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H8/300H Super Low Power Series

Switching SCI Pin Assignment

Introduction

The H8/38099 is provided with a 3-channel serial communication interface (SCI3) as a peripheral function. The pins of the SCI3_1 (channel 1 of the SCI3 module) can be assigned to either port 4 or port F. This application note describes how to change the SCI3_1 pin assignment from port 4 to port F.

Target Device

H8/38099

Contents

1. Specifications

1. The SCI3_1 pin functions assigned to port 4 are changed to port F using the port function switching function of the H8/38099.
2. The H8/38099 sends and receives serial data in clock synchronous mode.

2. Description of Functions Used

2.1 I/O Ports (Port 4/Port F Pin Configuration)

Port F has input/output pins covering an external interrupt input pin, SCI3_1 input/output pins, and a timer G input pin. Port 4 has input/output pins covering SCI3_1 input/output pins and the timer F input/output pins. The pin configuration of port F and port 4 is shown in figure 1. Set port F as SCI3_1 pins using the port function control register and the serial port control register.

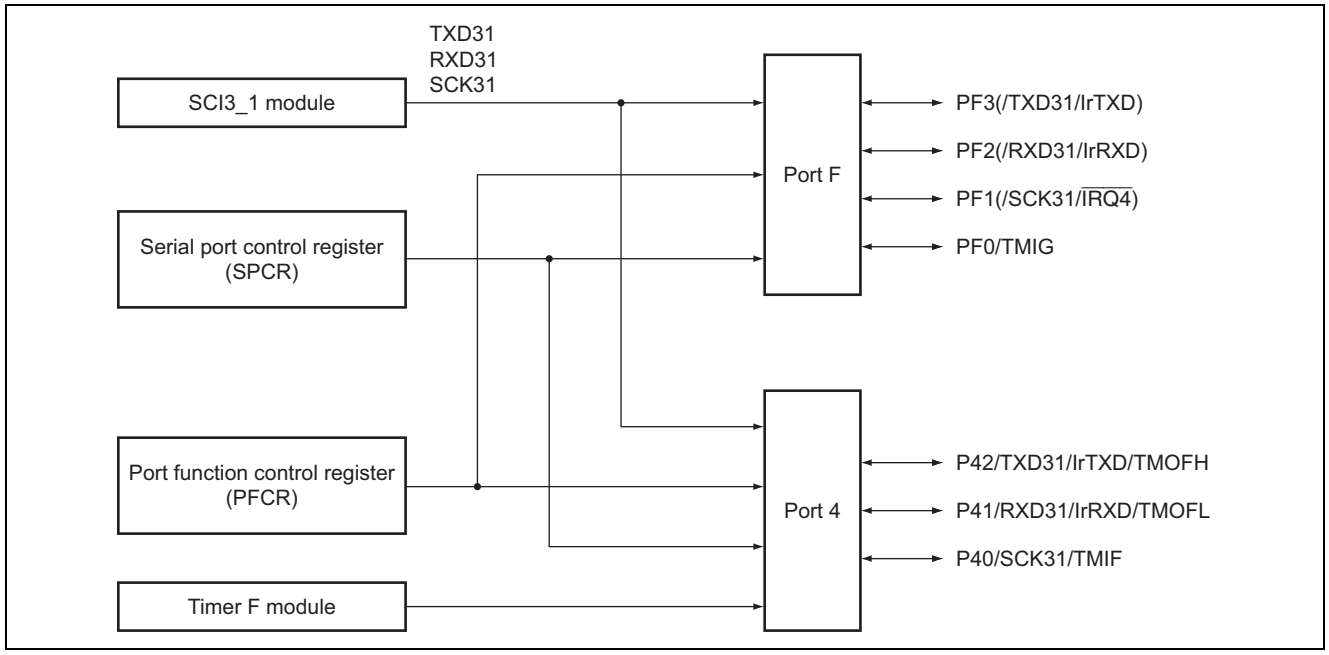


Figure 1 Functional Block Diagram

2.2 Functions Used

2.2.1 Description of Functions

In this sample task, the H8/38099 switches SCI3_1 pins from P42 to P40 (default) to PF3 to PF1 using the port function switching function to send/receive serial data in clock synchronous mode.

2.2.2 I/O Port Function (Switching Port Function)

- Port Function Control Register (PFCR)
  PFCR is an 8-bit read/write register that switches pins and controls the assignment of the SCI3_1 and SCI3_2 pins.

2.2.3 Serial Communication Interface (SCI3)

- Receive Shift Register 3_1 (RSR3_1)
  RSR3_1 is a shift register for reception that is used for converting the serial data input from the RXD31 pin to parallel data. When one frame of data is received, it is automatically transferred to RDR3_1. This register cannot be accessed directly from the CPU.

- Receive Data Register 3_1 (RDR3_1)
  RDR3_1 is an 8-bit register for storing received data. When one frame of data is received, it is transferred from RSR3_1 to this register and RSR3_1 becomes ready to receive the next data. This double buffer structure of RSR3_1 and RDR3_1 allows continuous data reception. RDR3_1 should be read only once after confirming that the RDRF31 bit in SSR3_1 is set to 1. RDR3_1 cannot be written from the CPU. The initial value of RDR3_1 is H'00. RDR3_1 is initialized to H'00 by a reset or on entering standby mode, watch mode, or module standby mode.

- Transmit Shift Register 3_1 (TSR3_1)
  TSR3_1 is a shift register used to send serial data. The data written to TDR3_1 is automatically transferred to TSR3_1, and is then output from the TXD31 pin sequentially from the LSB to send serial data. However, when no data is written in TDR3_1 (TDRE31 is set to 1), no data is transferred from TDR3_1 to TSR3_1. This register cannot be accessed directly from the CPU.

- Transmit Data Register 3_1 (TDR3_1)
  TDR3_1 is an 8-bit register for storing transmit data. When TSR3_1 is detected to be empty, the transmit data written to TDR3_1 is transferred to TSR3_1 and transmission starts. This double buffer structure of TSR3_1 and TDR3_1 allows continuous data transmission. When the next transmit data has been written to TDR3_1 when the transmission of one frame of data ends, the data is transferred to TSR3_1 to continue data transmission. To ensure serial transmission, transmit data should be written to TDR3_1 only once after confirming that the TDRE31 bit in SSR3_1 is set to 1. The initial value of TDR3_1 is H'FF. TDR3_1 is initialized to H'FF by a reset or on entering standby mode, watch mode, or module standby mode.

- Serial Mode Register 3_1 (SMR3_1)
  SMR3_1 is a register that selects a serial data communication format and the clock source of the on-chip baud rate generator. SMR3_1 is initialized to H'00 by a reset or on entering standby mode, watch mode, or module standby mode.

- Serial Control Register 3_1 (SCR3_1)
  SCR3_1 is a register that controls data transmission/reception and interrupts and selects a transmission/reception clock source. SCI3_1 is initialized to H'00 by a reset or on entering standby mode, watch mode, or module standby mode.

- Serial Status Register 3_1 (SSR3_1)
  SSR3_1 consists of the SCI3_1 status flags and stores the received multiprocessor bit and multiprocessor bit for transmission. TDRE31, RDRF31, OER31, PER31, and FER31 can be written to only for clearing. SSR3_1 is initialized to H'84 by a reset or on entering standby mode, watch mode, or module standby mode.

- Bit Rate Register 3_1 (BRR3_1)
  BRR3_1 is an 8-bit read/write register that sets a bit rate. The initial value of BRR3_1 is H'FF. In this sample task, N (see below) is set to 24 to produce a 100-kbps transfer clock.

$$N \text{ (setting value of BRR3\_1)} = \frac{\phi}{4 \times 2^{2n} \times B} - 1$$

B: Bit rate
N: Setting value of BRR3_1 in the baud rate generator ($0 \leq N \leq 255$)
ϕ: Operating frequency (Hz)
n: Input clock number of the baud rate generator (n = 0, 2, 3)
(For the relationship between n and clock, see table 1.)

Table 1 SMR3_1 Setting

		SMR3_1 Setting Value	
n	**Clock**	**CKS1**	**CKS0**
0	ϕ	0	0
0	$\phi_W/2$*	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

Note: * In sub-active mode or sub-sleep mode, SCI3_1, SCI3_2, and SCI3_3 are available for use only when the CPU operating clock is $\phi_W/2$.

- Serial Port Control Register (SPCR)
  SPCR switches the pin functions of the TXD32 and TXD31/IrTXD pins and specifies whether to invert the input/output data on the RXD32 pin, RXD31/IrRXD pin, TXD32 pin, and TXD31/IrTXD pin.

- IrDA Control Register (IrCR)
  IrCR controls the operation of the IrDA function of SCI3_1.

2.2.4 Watchdog Timer Function

The H8/38099 has an 8-bit internal watchdog timer (WDT). After a reset, the watchdog timer is turned on. The inside of the H8/38099 is reset when the WDT counter overflows because of the CPU being unable to rewrite the counter value due to a system runaway or other reasons. In this sample task, the watchdog timer function is deactivated because it is not used.

- Timer control/status register WD1 (TCSRWD1)
  Timer control/status register WD1 (TCSRWD1) controls writing to TCSRWD1 itself and to TCWD. TCSRWD1 also controls the operation of the watchdog timer and indicates its operating status. To rewrite this register, use the MOV instruction. Bit manipulation instructions cannot be used to change its setting.

2.3 Assignment of Functions

Table 2 lists the assignment of functions of this sample task. With the functions assigned as shown in table 1, the SCI3_1 pins are switched from port 4 to port F and transmission/reception of serial data is performed in clock synchronous mode.

Table 2 Assignment of Functions

Function	Description
PFCR	Controls SCI3_1 pin assignment.
TDR3_1	An 8-bit register to store transmit data.
RDR3_1	An 8-bit register to store received data.
SMR3_1	Sets clock synchronous mode and selects ϕ as the baud rate generator clock source.
SCR3_1	Enables transmission and reception and selects an internal clock as the clock source.
SSR3_1	Status flags that indicate the operating states of SCI3_1.
BRR3_1	Sets the bit rate (100 kbps).
SPCR	Specifies the pin as the TXD31/IrTXD pin and to output data without inverting it. Specifies to use the data input from the RXD31 pin without inverting it.
IrCR	Specifies the TXD31/IrTXD and RXD31/IrRXD pins as the TXD31 and RXD31 pins, respectively.
SCK31	SCI3_1 clock output pin (selected from the multiplexed functions on the PF3 pin).
TXD31	SCI3_1 transmit data output pin (selected from the multiplexed functions on the PF2 pin).
RXD31	SCI3_1 receive data input pin (selected from the multiplexed functions on the PF1 pin).
TCSRWD	Stops the watchdog timer.

3. Principles of Operation

3.1 Switching the Port Function

This section describes how to switch the port function. Writing 1 to the SC31S bit in the port function control register (PFCR) sets the SCI3_1 pins from port 4 (default) to port F.

Table 3 shows the relationship between the setting values of the registers required to specify a pin function of PF3 and the corresponding pin functions. The PF3 pin is set as the TXD31 output pin by setting the following registers.

Table 3 PF3 Pin Function

Register Name	PFCR	SPCR	IrCR	PCRF	
Bit Name	**SC31S**	**SPC31**	**IrE**	**PCRF3**	**PF3 Pin Function**
Setting Value	0	X	X	0	General input (PF3)
				1	General output (PF3)
	1	0		0	General input (PF3)
				1	General output (PF3)
		1	0	X	TXD31 output
			1		IrTXD output

Legend:
X: Don't care

Table 4 shows the relationship between the setting values of the registers required to specify a pin function of PF2 and the corresponding pin functions. The PF2 pin is set as the RXD31 input pin by setting the following registers.

Table 4 PF2 Pin Function

Register Name	PFCR	SCR3_1	IrCR	PCRF	
Bit Name	**SC31S**	**RE_31**	**IrE**	**PCRF2**	**PF2 Pin Function**
Setting Value	0	X	X	0	General input (PF2)
				1	General output (PF2)
	1	0		0	General input (PF2)
				1	General output (PF2)
		1	0	X	RXD31 input
			1		IrRXD input

Legend:
X: Don't care

Table 5 shows the relationship between the setting values of the registers required to specify a pin function of PF1 and the corresponding pin functions. The PF1 pin is set as the SCK31 pin by setting the following registers.

Table 5 PF1 Pin Function

Register Name	PMR9	PMRF	PFCR	SMR3_1	SCR3_1		PCRF	
Bit Name	**IRQ4**	**IRQ4**	**SC31S**	**COM**	**CKE1**	**CKE0**	**PCRF1**	**PF1 Pin Function**
Setting Value	0	1	X	X	X	X	X	$\overline{\text{IRQ4}}$ input pin
	Other than above		0	X	X	X	0	General input pin (PF1)
							1	General output pin (PF1)
			1	0	0	0	0	General input pin (PF1)
							1	General output pin (PF1)
						1	X	SCK31 output pin
					1	0		SCK31 input pin
				1	0			SCK31 output pin
					1			SCK31 input pin

Legend:
X: Don't care

3.2 Transmission/Reception of Serial Data in Clock Synchronous Mode

For details of transmission/reception of serial data in clock synchronous mode, see section 17.5, “Operation in Clock Synchronous Mode”, in the H8/38099 Group Hardware Manual.

4. Description of Software

4.1 Modules

Table 6 lists the modules of this sample task.

Table 6 Modules

Module Name	Label Name	Function
Main routine	main	Sets port switching for the SCI3_1 pins and makes initial settings of SCI3_1.
SCI3_1	t_r31	Sends/receives serial data in clock synchronous mode.

4.2 Arguments

No argument is used in this sample task.

4.3 Internal Registers Used

This section describes the internal registers used in this sample task.

- Port Function Control Register (PFCR) Address: H'FFFFCB

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
0	SC31S	1	0	R/W	SCI3_1 Pin Assignment Select 0: TXD31 is assigned to P42. RXD31 is assigned to P41. SCK31 is assigned to P40. 1: TXD31 is assigned to PF3. RXD31 is assigned to PF2. SCK31 is assigned to PF1.

- Receive Data Register 3_1 (RDR3_1) Address: H'FFFF9D

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	RDR7	0	—	R	RDR3_1 is an 8-bit register for storing received data. When one frame of data is received, it is transferred from RSR3_1 to this register and RSR3_1 becomes ready to receive the next data. This double buffer structure of RSR3_1 and RDR3_1 allows continuous data reception. RDR3_1 should be read only once after confirming that the RDRF31 bit in SSR3_1 is set to 1. RDR3_1 cannot be written from the CPU. The initial value of RDR3_1 is H'00. RDR3_1 is initialized to H'00 by a reset or on entering standby mode, watch mode, or module standby mode.
6	RDR6	0	—	R	
5	RDR5	0	—	R	
4	RDR4	0	—	R	
3	RDR3	0	—	R	
2	RDR2	0	—	R	
1	RDR1	0	—	R	
0	RDR0	0	—	R	

- Transmit Data Register 3_1 (TDR3_1) Address: H'FFFFB5

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	TDR7	1	0	W	TDR3_1 is an 8-bit register for storing transmit data. When TSR3_1 is detected to be empty, the transmit data written to TDR3_1 is transferred to TSR3_1 and transmission starts. This double buffer structure of TSR3_1 and TDR3_1 allows continuous data transmission. When the next transmit data has been written to TDR3_1 when the transmission of one frame of data ends, the data is transferred to TSR3_1 to continue data transmission. To ensure serial transmission, transmit data should be written to TDR3_1 only once after confirming that the TDRE31 bit in SSR3_1 is set to 1. The initial value of TDR3_1 is H'FF. TDR3_1 is initialized to H'FF by a reset or on entering standby mode, watch mode, or module standby mode.
6	TDR6	1	1	W	
5	TDR5	1	0	W	
4	TDR4	1	0	W	
3	TDR3	1	0	W	
2	TDR2	1	0	W	
1	TDR1	1	0	W	
0	TDR0	1	1	W	

- Serial Mode Register 3_1 (SMR3_1) Address: H'FFFF98

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	COM	0	1	R/W	Communication Mode 0: Operates in asynchronous mode. 1: Operates in clock synchronous mode.
1	CKS1	0	0	R/W	Clock Select 1, 0 Select the clock source of the on-chip baud rate generator. 00: ϕ clock (n = 0) 01: ϕ_W/2 clock (n = 0) 10: ϕ/16 clock (n = 2) 11: ϕ/64 clock (n = 3) When ϕ_W/2 is selected, SCI3 is available in sub-active mode or sub-sleep mode only when the CPU operating clock is ϕ_W/2.
0	CKS0	0	0	R/W	

- Serial Control Register 3_1 (SCR3_1) Address: H'FFFF9A

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
5	TE	0	0/1	R/W	Transmit Enable When this bit is set to 1, data transmission is enabled. When TE = 0, the TDRE31 bit in SSR3_1 is fixed to 1. When transmit data is written to TDR3_1 with TE set to 1, the TDRE31 bit in SSR3_1 is cleared to 0 and transmission of serial data starts. Before setting TE to 1, be sure to set SMR3_1 and SPC31 in SPCR to determine the transmission format.
4	RE	0	0/1	R/W	Receive Enable When this bit is set to 1, data reception is enabled. In this state, when a start bit (in asynchronous mode) or a synchronization clock input (in clock synchronous mode) is detected, reception of serial data starts. Before setting RE to 1, be sure to set SMR3_1 to determine the reception format. Note that, even if RE is cleared to 0, the RDRF31, FER31, PER31, and OER31 flags in SSR3_1 are not affected and remain unchanged.
1	CKE1	0	0	R/W	Clock Enable 1, 0
0	CKE0	0	0	R/W	Select a clock source. Clock synchronous mode: 00: Internal clock (SCK31 becomes a clock output pin) 01: Reserved 10: External clock (SCK31 becomes a clock input pin) 11: Reserved

- Serial Status Register 3_1 (SSR3_1) Address: H'FFFF9C

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	TDRE31	1	0/1	R/(W)*	Transmit Data Register Empty Indicates whether any transmit data is in TDR. [Setting conditions] • TE = 0 in SCR3_1 • Data is transferred from TDR3_1 to TSR3_1 [Clearing conditions] • Writing 0 to this bit after reading 1 from it • Transmit data is written to TDR3_1
6	RDRF31	0	0/1	R/(W)*	Receive Data Register Full Indicates whether received data is stored in RDR3_1. [Setting condition] • Data is received normally and transferred from RSR3_1 to RDR3_1 [Clearing conditions] • Writing 0 to this bit after reading 1 from it • Received data is read from RDR3_1 When an error is detected during data reception or RE in SCR3_1 is cleared to 0, RDR3_1 and RDRF31 are not affected and remain unchanged. Note that, when data reception is completed with RDRF31 set to 1, an overrun error (OER31) occurs and the receive data will be lost.
5	OER31	0	0/1	R/(W)*	Overrun Error [Setting condition] • Overrun error occurs during data reception [Clearing condition] • Writing 0 to this bit after reading 1 from it When RE in SCR3_1 is cleared to 0, OER31 is not affected and remains unchanged. When an overrun error occurs, the data received before the overrun error is retained in RDR3_1 and the data received thereafter will be lost. As long as OER31 is 1, data can no longer be received. In clock synchronous mode, data transmission can no longer be continued, either.
2	TEND31	1	1	R	Transmit End [Setting conditions] • TE = 0 in SCR3_1 • TDRE31 = 1 when the last bit of a transmit character is transmitted [Clearing conditions] • Writing 0 to TDRE31 after reading 1 from it • When transmit data is written to TDR3_1

Note: * Only writing 0 to clear the flag is allowed.

- Bit Rate Register 3_1 (BRR3_1) Address: H'FFFF99

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	BRR7	1	0	R/W	BRR3_1 is an 8-bit register that sets the bit rate.
6	BRR6	1	0	R/W	In this sample task, this register is set to 24 to use
5	BRR5	1	0	R/W	a 100-kbps transfer clock.
4	BRR4	1	1	R/W	
3	BRR3	1	1	R/W	
2	BRR2	1	0	R/W	
1	BRR1	1	0	R/W	
0	BRR0	1	0	R/W	

- Serial Port Control Register (SPCR) Address: H'FFFF91

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
4	SPC31	0	1	R/W	P42/TXD31/IrTXD/TMOFH (PF3/TXD31/IrTXD) Pin Switching Selects whether to use the P42/TXD31/IrTXD/TMOFH (PF3/TXD31/IrTXD) pin as the P42/TMOFH (PF3) pin or TXD31/IrTXD pin. 0: Used as the P42 (PF3) input/output pin or TMOFH output pin. 1: Used as the TXD31/IrTXD output pin. This bit must be set to 1 before setting the TE bit in SCR3_1.

- IrDA Control Register (IrCR) Address: H'FFFFA7

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	IrE	0	0	R/W	IrDA Enable Sets the SCI3_1 input/output pins to normal SCI or IrDA. 0: TXD31/IrTXD and RXD31/IrRXD pins function as the TXD31 and RXD31 pins, respectively. 1: TXD31/IrTXD and RXD31/IrRXD pins function as the IrTXD and IrRXD pins, respectively.

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFFFB1

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	B6WI	1	1	R/W	Bit 6 Write Disable Writing to bit 6 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
6	TCWE	0	0	R/W	Timer Counter W Write Enable Writing to TCWD is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 7.
5	B4WI	1	*	R/W	Bit 4 Write Disable Writing to bit 4 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	0	*	R/W	Timer Control/Status Register W Write Enable Writing to bits 2 and 0 of this register is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 5.
3	B2WI	1	*	R/W	Bit 2 Write Disable Writing to bit 2 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
2	WDON	1	*	R/W	Watchdog Timer On Setting this bit to 1 causes TCWD to start counting up. Clearing it to 0 causes TCWD to stop counting up. [Setting conditions] • A reset is made. • 0 is written to B2WI and 1 is written to WDON while TCSRWE is 1. [Clearing condition] • 0 is written to B2WI and WDON while TCSRWE is 1.
1	B0WI	1	1	R/W	Bit 0 Write Disable Writing to bit 0 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
0	WRST	0	0	R/W	Watchdog Timer Reset [Setting condition] • TCWD overflows and an internal reset signal is generated. [Clearing conditions] • A reset is made with the $\overline{\text{RES}}$ pin. • 0 is written to B0WI and WRST while TCSRWE is 1.

Note: * These bits are manipulated so as to stop the watchdog timer. See the flowchart for the main routine.

4.4 RAM Usage

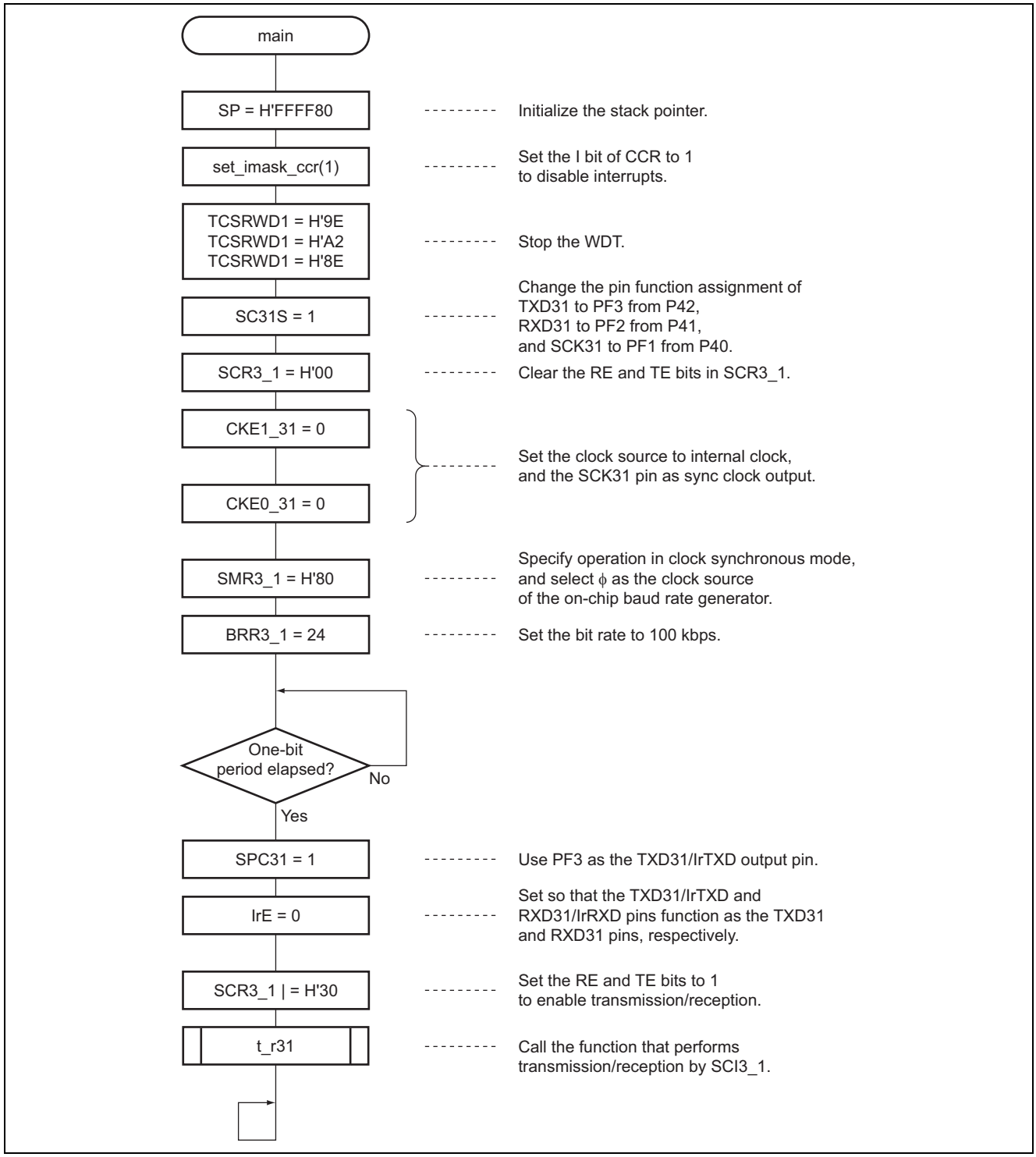
Table 7 shows the RAM usage in this sample task.

Table 7 RAM Usage

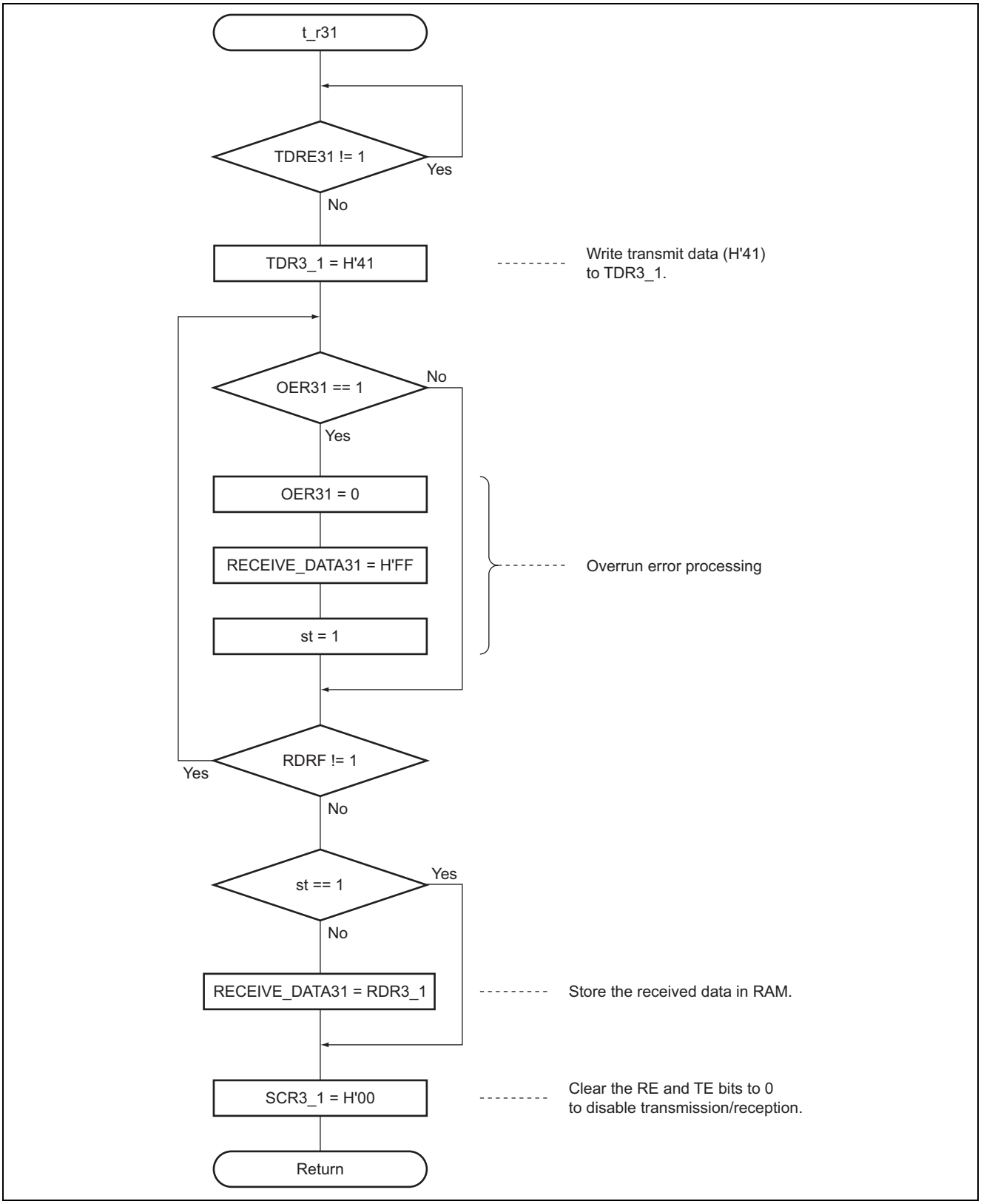
Type	Label Name	Description	Used In
unsigned char	RECEIVE_DATA31	Stores the data received by SCI3_1.	t_r31
unsigned char	st	A flag that is referenced to see when an overrun error has occurred in SCI3_1. 0: No overrun error occurred. 1: An overrun error occurred.	main t_r31

5. Flowcharts

5.1 main Function



5.2 t_r31 Function



6. Link Address Specifications

Section Name	Address
CV1	H'000000
P	H'000800
B	H'FFF380

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
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