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M16C/62P Group

Stop Mode Set-Up

1. Abstract

Setting and operation for entering stop mode are described here. Figure 1 shows the set-up procedure. A reference program is an example when using the INT0 interrupt for a return factor from stop mode.

2. Introduction

This application note is applied to the M16C/62P group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M16C/62P Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.



3. Set-up

- (1) Enables the interrupt used for returning from stop mode.
- (2) Sets the interrupt enable flag(I flag) to "1".
- (3) Clearing the protection and setting all clock stop control bit to "1" stops oscillation and causes the processor to go into stop mode

Interrupt control register	
TBilC(i=3 to 5) [Address 004516 to 004716]	
BCNIC [Address 004A16]	
KUPIC [Address 004D16] SiTIC(i=0 to 2) [Address 005116, 005316, 004F1	
SiRIC(i=0 to 2) [Address 005216, 005416, 00501	- INTIC(I=3) IA00fess 0044161
TAilC(i=0 to 4) [Address 005516 to 005916] TBilC(i=0 to 2) [Address 005A16 to 005C16]	(j=3, 4) [Address 004816, 004916] INTilC(i=0 to 2) [Address 005D16 to 005F16]
Interrupt priority level select bit Make sure that the interrupt priority	Interrupt priority level select bit Make sure that the interrupt priority level of the
level of the interrupt which is used to cancel the wait mode is higher than	
the processor interrupt priority(IPL) of	
the routine where the WAIT instruction is executed.	Reserved bit Must always be set to "0"
	•
(2) Interrupt enable flag (I flag) ◄"1"	-
(z) interrupt enable hag (r hag)	
	•
(3) Canceling protect	
Protect register PRCR [Address 000A16]	
Enables writing to system clock cont	trol registers 0 and 1
(addresses 000616 and 000716) 1 : Write-enabled	
	:
(3) Setting operation clock after returning from sto (When operating with XIN after returning)	p mode (When operating with XCIN after returning)
b7 b0 System clock control register CM0 [Address 000616]	b7 b0 System clock control register 0 1 1 CM0 [Address 000616]
Main clock (XIN-XOUT) stop bit	Port XC select bit
On	XCIN-XCOUT generation
System clock select bit XIN, XOUT	System clock select bit XCIN, XCOUT
As this register becomes setting mentioned above when operating with XIN (count source of BCLK is XIN), the user does not need to set it again.	As this register becomes setting mentioned above when operating with XCIN (count source of BCLK is XCIN), the user does not need to set it again. When operating with XIN, set port XC select bit to "1" before setting system clock select bit to "1". The both bits cannot be set at the same time.
	•
3) All clocks off (stop mode)	
3) All clocks off (stop mode)	
System clock control register CM1 [Address 000716]	
All clock stop control bit 1 : All clocks off (stop mode)	
Reserved bit	
Must always be set to "0"	
	stop control bit to "1".
nsert at least four NOPs after the instruction that sets the all clock	
nsert at least four NOPs after the instruction that sets the all clock	•



1. The exa	mple of	f reference	e program				
•************** ,	********	*******	******	******			
; ; M16C/62	M16C/62P Program Collection						
, ; FILE NAM	FILE NAME : rjj05b0696_src.a30 CPU : M16C/62P Group						
; CPU							
; FUNCTIO							
; HISTORY	HISTORY : 2004.12.24 Ver 1.00 Copyright(C)2004, Renesas Technology Corp.						
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; Copyrigh	t(C)2004	, Renesas S	Solutions Cor	р.			
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• •	***************************************						
, .**************** ,							
; Inclu	Ide	***	***				
, .LIS	т	off		;Stops outputting lines to the assembler list file			
.INC	LUDE	sfr62p.inc		;Reads the file that defined SFR			
.LIS	т	on		;Starts outputting lines to the assembler list file			
;							
; Svm	Symbol definition						
,	******	****	*****	******			
,							
RAM_TOP		.equ	00400h	;Start address of RAM			
RAM_END		.equ	013ffh	;End address of RAM			
ROM_TOP		.equ	0f4000h	;Start address of ROM			
VECT_TOP		.equ	0ffe00h	;Start address of vect_top			
FIXED_VECT_TOP .equ Offfdch			;Start address of fixed_vect_top				
SB_BASE		.equ	00380h	;Base address of sb			
, .************** ,	*******	*****	*****	*****			
•	ram area						
,				****************************			
;======== ; Start							
;=====================================			===========				
,	.secti	on prograr	n,code	;Declares section name and section type			
	.org		ROM_TOF	;Declares start address			
	.sb		SB_BASE	;			
;							



	ldc	#RAM END+1.isr	;Sets interrupt stack pointer
	ldc	#SB_BASE,sb	;Sets sb register
;		_ ,	
	mov.b	#03h,prcr	;Removes protect
			;Set processor mode registers 0 and 1
	MOV.W	#0800h,pm0	;Single-chip mode
			;No expansion, No wait
	mov.w	#2008h,cm0	;Xcin-Xcout High
			;Xin-Xout High, Main clock is No divison
	mov.b	#0,prcr	;Protects all registers
;			
	ldintb	#VECT_TOP	;Sets interrupt table register
;			
	MOV.W	#0,r0	;Clears WORKRAM area
	MOV.W	#((RAM_END+1)-	RAM_TOP)/2,r3
	mov.w	#RAM_TOP,a1	
	sstr.w		
, 			
; Main p	orogram		
;==========			
MAIN:			
,	fclr	:	Clear interrupt anable flag
	ICII	i	;Clear interrupt enable flag ;M16C-85-0202(Japanese) countermeasure
,			;M16C-85-0202(Japanese) countermeasure ;M16C-85-0204(English) countermeasure
, -			
,	mov.b	#00000011b.int0id	;Interrupt control register
;			;Interrupt priority level select bit
;			;(011:Level 3, interrupt disabled)
,		+	;Interrupt request bit (0:interrupt not requested)
	mov.w	#00400h,r0	;Dummy read
	fset	i	;Set interrupt enable flag
	mov.b	#0000001b,prcr	;Removes protect
	mov.b	#00001000b,cm0	;Xcin-Xcout(High)
	bset	0,cm1	;Stop mode
	jmp.b	MAIN_A	;TN-16C-124A/JA(Japanese) countermeasure
;			;TN-16C-124A/EA(English) countermeasure
,			;M16C-84-0202(Japanese) countermeasure
;			;M16C-84-0204(English) countermeasure
MAIN_A:			
	nop		
,	mov.b	#00000000b.prcr	;Protects all registers



MAIN_B:

	jmp	MAIN_B	
;			
;			
;====	Interrupt program		
, :====	Interrupt program		
, INT0 <u>.</u>	_INT:		
;			
;	;/	INT0 interrupt routine	/
;			
	reit		
,==== ;	Dummy interrupt pro	======================================	
;====			
DUM	reit		
	Ten		
, •*****	******	*****	***********
;	Setting of variable v	ector table	
•****	•		*****
;			
	.section ve	ect,romdata	
	.org	VECT_TOP +	(4 * 4)
;			
	.lword	DUMMY	;INT3 interrupt vector
	.lword	DUMMY	;TB5 interrupt vector
	.lword	DUMMY	;TB4 interrupt vector
			;UART1 bus collision detection interrupt vector
	.lword	DUMMY	;TB3 interrupt vector
		51000/	;UART0 bus collision detection interrupt vector
	.lword	DUMMY	;SI/04/INT5 interrupt vector
	.lword	DUMMY	;SI/03/INT4 interrupt vector
	.lword	DUMMY	;UART2 bus collision detection interrupt vector
	.lword .lword	DUMMY DUMMY	;DMA0 interrupt vector
	.lword	DUMMY	;DMA1 interrupt vector ;KEY interrupt vector
	.lword	DUMMY	;A-D interrupt vector
	.lword	DUMMY	;UART2 transmit/NACK interrupt vector
	.lword	DUMMY	;UART2 receive/ACK interrupt vector
	.lword	DUMMY	;UART0 transmit/NACK interrupt vector
	.lword	DUMMY	;UART0 receive/ACK interrupt vector
	.lword	DUMMY	;UART1 transmit/NACK interrupt vector
	.lword	DUMMY	;UART1 receive/ACK interrupt vector
	.lword	DUMMY	;TA0 interrupt vector
	.lword	DUMMY	;TA1 interrupt vector



.lword	DUMMY	;TA2 interrupt vector	
.lword	DUMMY	,TA3 interrupt vector	
.lword	DUMMY	TA4 interrupt vector	
.lword	DUMMY	;TB0 interrupt vector	
.lword	DUMMY	;TB1 interrupt vector	
.lword	DUMMY	TB2 interrupt vector	
.lword	INT0_INT	;INT0 interrupt vector	
.lword	DUMMY	;INT1 interrupt vector	
.lword	DUMMY	;INT2 interrupt vector	
•*************************************	*****	**********	
; Setting of fixed vector			
.*************************************	******	***************	
;			
.section f_vect,	.section f_vect,romdata		
.org	FIXED_VECT_T	OP	
;			
.lword	DUMMY	;Undefined instruction interrupt vector	
.lword	DUMMY	;Overflow (INTO instruction) interrupt vector	
.lword	DUMMY	;BRK instruction interrupt vector	
.lword	DUMMY	;Address match interrupt vector	
.lword	DUMMY	;Single-step interrupt vector	
.lword	DUMMY	;Watchdog timer interrupt vector	
		;Oscillation stop and Re-oscillation detection interrupt	
		;vector	
		;Voltage down detection interrupt vector	
.lword	DUMMY	;DBC interrupt vector	
.lword	DUMMY	;NMI interrupt vector	
.lword	START	;Sets start vector	
;			
.end			



5. Referense

Hardware manual

M16C/62P group version (M16C/62P,M16C/62PT) Hardware Manual Rev.2.30 (Use the latest on the web-site: http://www.renesas.com)

6. Web-site and contact for support

Renesas web-site http://www.renesas.com/

Contact for Renesas technical support E-mail: support_apl@renesas.com



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