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# H8/300L Series

## SSB Communication via Serial Communication Interface (H8/3644)

### Introduction

As shown in figure 1.1, IC1 and IC2, which are connected by a serial clock (SCL) and a serial data (SDA) line, are controlled using an SSB communication function.

### Target Device

H8/3644

### Contents

## 1. Specifications

1. As shown in figure 1.1, IC1 and IC2, which are connected by a serial clock (SCL) and a serial data (SDA) line, are controlled using an SSB communication function.
2. The length of the transmit data is 16 bits. The data is transmitted according to the 6.4-µs transfer clock.
3. After the end of 16-bit transferred data, a tail mark is added and transmitted. In this sample task, the hold tail is selected as a tail mark.

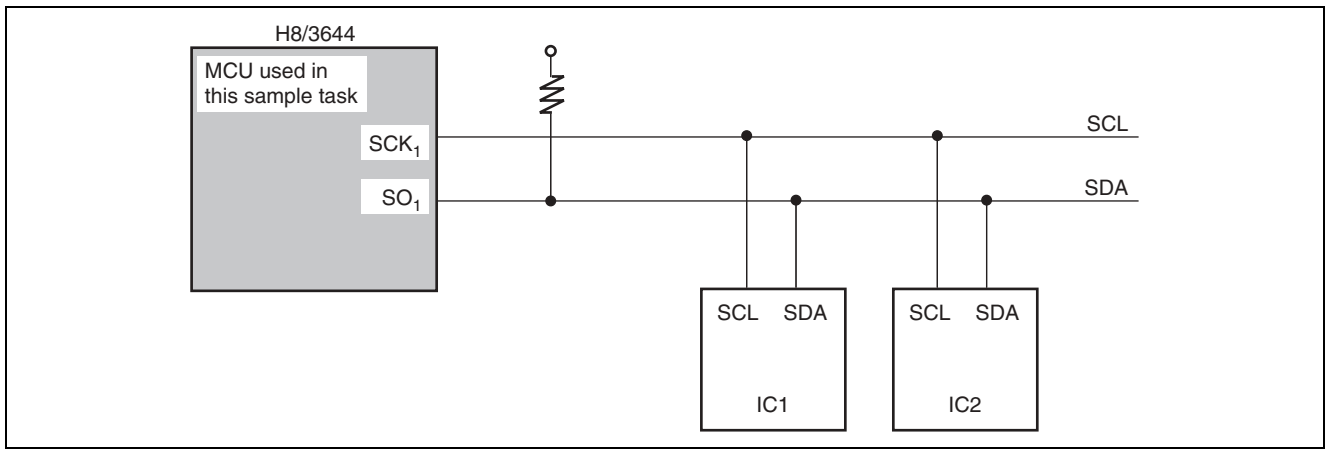



**Figure 1.1 Example of SSB Connection**

## 2. Description of Functions

1. In this sample task, SSB communication is performed via the serial communication interface (SCI). Figure 2.1 shows a block diagram of the SSB communication, and the following is the description for the block diagram:
   - The SSB communication method is configured with two lines, SCL and SDA, to control multiple ICs connected.
   - In SSB mode, a tail mark is added and transmitted after an 8-bit or 16-bit data transfer. The hold or latch tail can be selected for the tail mark.
   - The system clock frequency (ϕ) used as the basic clock for the CPU or peripheral-function operation is 5-MHz; this clock is obtained by dividing the 10-MHz OSC clock by 2.
   - The prescaler S (PSS) is a 13-bit counter, to which ϕ is input. The PSS counts up on each cycle.
   - The serial control register 1 (SCR1) is an 8-bit readable/writable register that selects operating mode, transfer clock source, and prescaler division ratio.
   - The serial control/status register 1 (SCSR1) is an 8-bit counter that indicates operation status, error status, etc.
   - The serial data register U (SDRU) is an 8-bit readable/writable register that functions as a data register for the upper 8 bits in 16-bit data transfer. Data written to SDRU is output to SDRL with the LSB first. Then, data is in turn input from the $SI_1$ pin with the LSB first, and data is shifted from the MSB to the LSB. SDRU should be read or written to after data transmission or reception is complete. If it is read or written to during data transmission or reception, data may not be guaranteed.
   - The serial data register L (SDRL) is an 8-bit readable/writable register that functions as a data register in 8-bit data transfer and as a data register for the lower 8 bits in 16-bit data transfer. In 8-bit data transfer, data written to SDRL is output from the $SO_1$ pin with the LSB first. Then, data is in turn input from the $SI_1$ pin with the LSB first, and data is shifted from the MSB to the LSB. In 16-bit data transfer, operation is the same as that in 8-bit data transfer except that data is input from SDRU. SDRL should be read or written to after data transmission or reception is complete. If it is read or written to during data transmission or reception, data may not be guaranteed.
   - The transfer clock can be selected from eight internal clocks. External clocks cannot be selected because this LSI provides clock output. The transfer rate can be selected with CKS2 to CKS0 in SCR1, however, the transfer clock cycle should be set as 2 µs or more because the transfer rate is also used for a tail mark.

— The SCI1 transfer format is shown in figure 2.2. Data is transferred with the LSB first that transmits data from its lowest bit. After 8-bit or 16-bit data transfer, a tail mark is added.

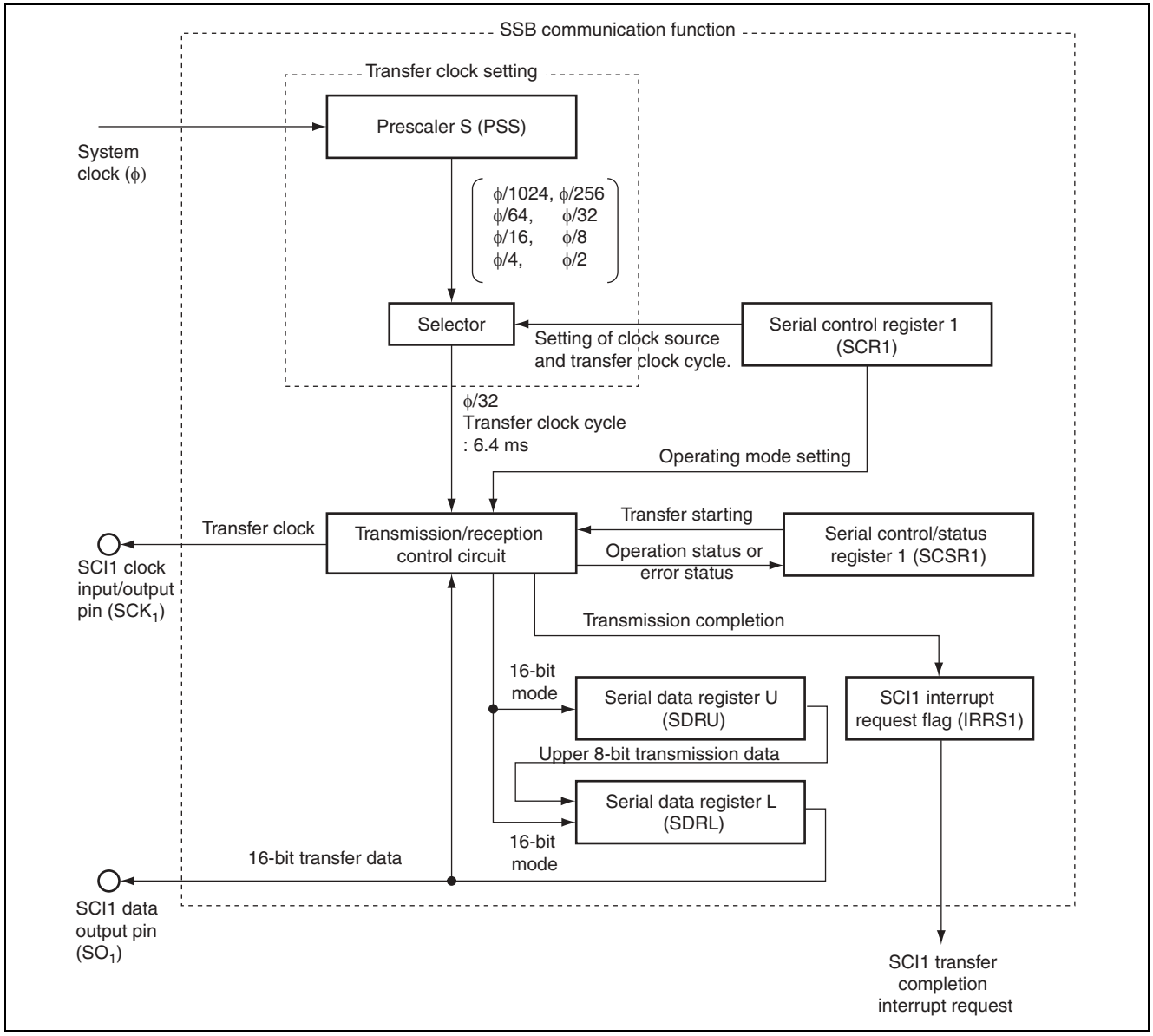



**Figure 2.1 Block Diagram of SSB Communication Function**

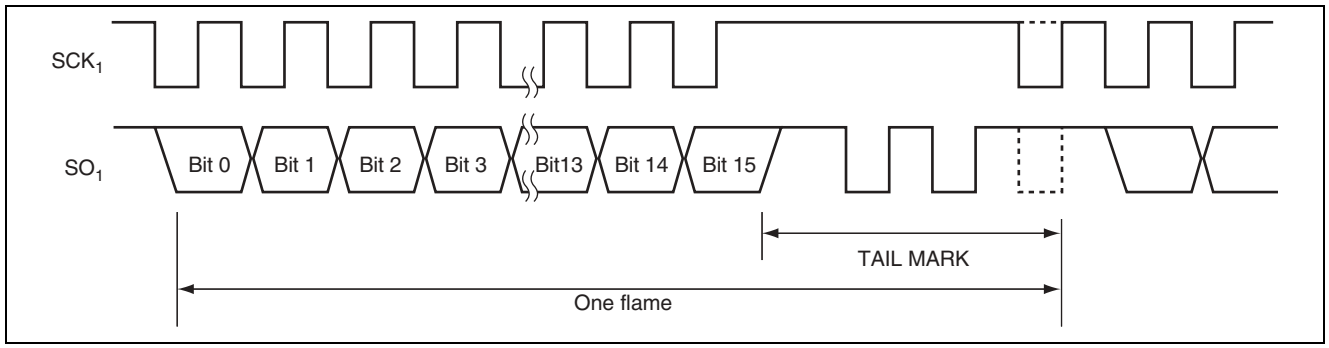



**Figure 2.2 Transfer Format (When SNC1 = 0, SNC0 = 1 and MRKON = 1)**

— The hold or latch tail can be selected for a tail mark. Figure 2.3 shows output waveforms of the hold and latch tails. Time t in figure 2.3 indicates the period determined by the transfer clock that is set with CKS2 to CKS0 in SCR1.

— One of the SCI1 interrupt sources is transfer completion. When the SCI1 transfer completes, IRRS1 in IRR2 is set to 1. SCI1 interrupt requests can be enabled or disabled with IENS1 in IENR2.

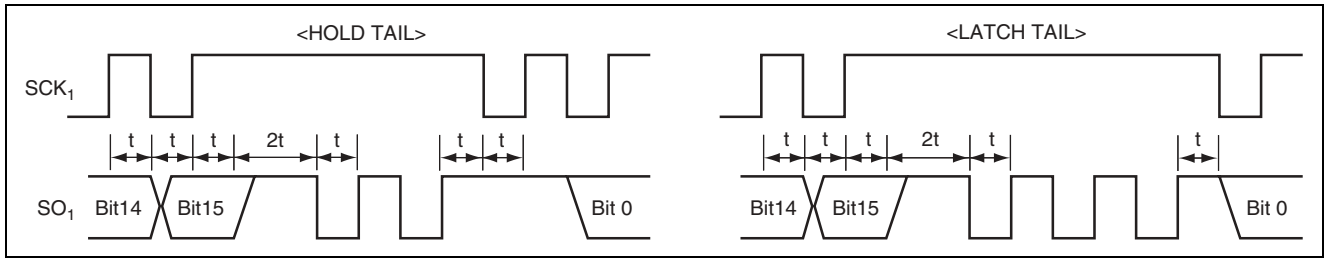



**Figure 2.3 Hold and Latch Tail Output Waveforms**

2. Table 2.1 shows the allocation of functions used in this sample task. Functions are allocated as shown in table 1 to perform SSB communication.

**Table 2.1 Function Allocation**

| Function | Function Allocation |
|---|---|
| PSS | 13-bit counter to which the system clock is input. |
| SCR1 | Operating mode, transfer clock source and prescaler division ratio are set. |
| SCSR1 | Operation status or error status is indicated. |
| SDRU | Data register for the upper 8 bits of 16-bit transmit data |
| SDRL | Data register for the lower 8 bits of 16-bit transmit data |
| SCK1 | Transfer clock output pin of SCI1 |
| SO1 | Transmit data output pin of SCI1 |
| IRRS1 | SCI1 transfer completion is indicated. |
| IENS1 | Enabling/disabling of SCI1 interrupt requests is controlled. |
| PMR3 | $P3_2/SO_1$ and $P3_0/SCK_1$ pin functions are set. |
| PMR7 | Turning on/off of the $P3_2/SO_1$ pin output buffer PMOS is controlled. |

## 3. Principle of Operation

1. Figure 3.1 shows the principle of operation. SSB communication is performed with the hardware and software processing shown in the figure.

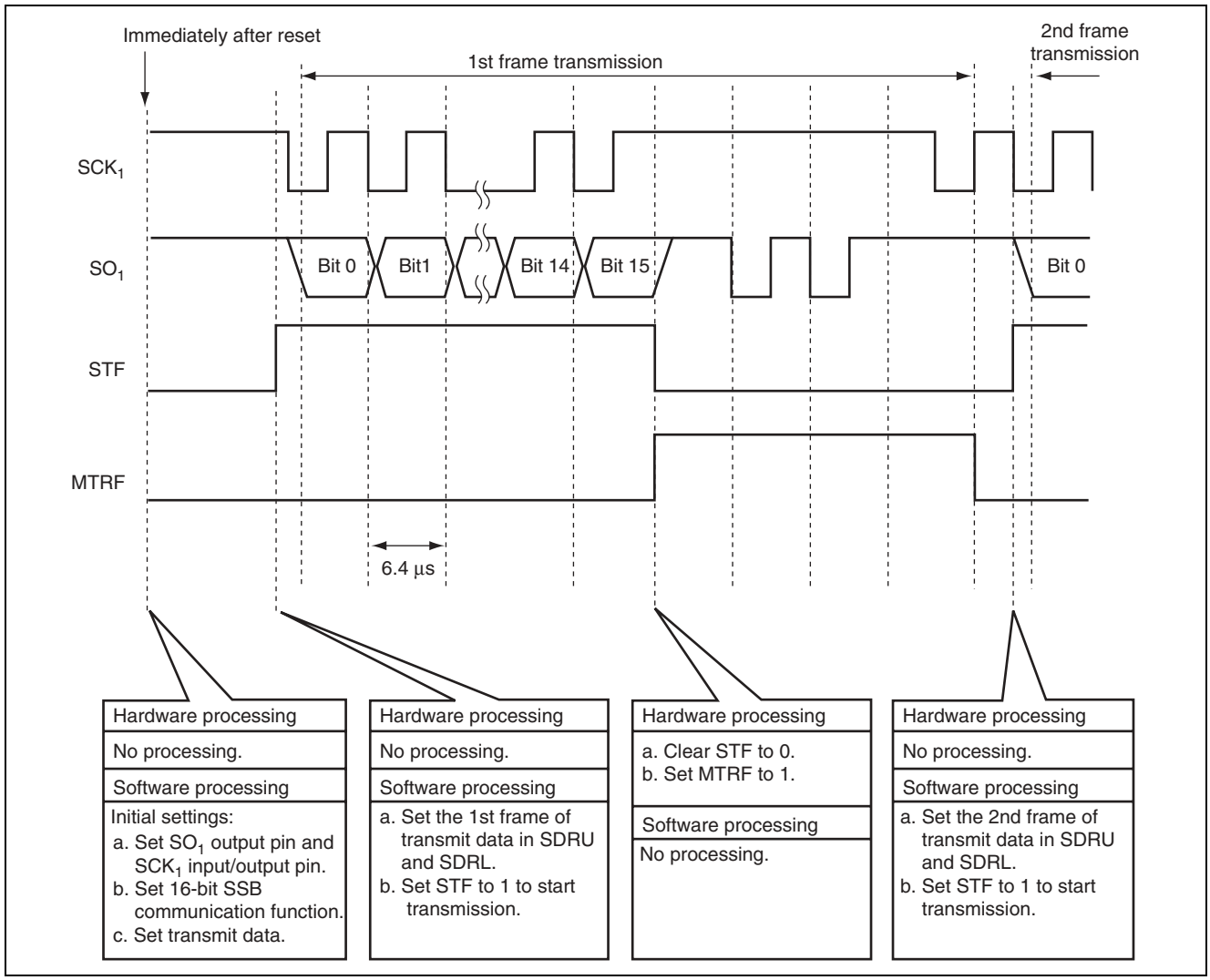



**Figure 3.1 Principle of Operation of SSB Communication**

# 4. Description of Software

## 4.1 Module

Table 4.1 describes the module used in this sample task.

**Table 4.1 Description of Module**

| Module | Label | Function |
|---|---|---|
| Main routine | main | Initializes the stack pointer, sets transfer data, sets SSB communication mode, enables interrupts, and terminates when 4 frames of 16-bit data have been transmitted. |

## 4.2 Arguments

Table 4.2 describes the arguments used in this sample task.

**Table 4.2 Description of Modules**

| Argument | Function | Used in | Data Length | Input/ Output |
|---|---|---|---|---|
| STD0H to STD3H | Upper 8 bits of 16-bit transmit data are stored | Main routine | 1 byte | Input |
| SRD0L to SRD3L | Lower 8 bits of 16-bit transmit data are stored | Main routine | 1 byte | Input |

## 4.3 Internal Registers

The internal registers used in this sample task are described in table 4.3.

**Table 4.3 Description of Internal Registers**

| Register | | Function | Address | Setting |
|---|---|---|---|---|
| SCR1 | SNC1<br>SNC0 | Serial Control Register 1 (Operating Mode Select 1, 0)<br>When SNC1 = 0 and SNC0 = 0, operating mode is set to 16-bit mode. | H'FFA0<br>Bit 7<br>Bit 6 | SNC1 = 0<br>SNC0 = 0 |
| | MRKON | Serial Control Register 1 (Tail Mark Control)<br>When MRKON = 1, a tail mark is output. | H'FFA0<br>Bit 5 | 1 |
| | LATCH | Serial Control Register 1 (Latch Tail Select)<br>When LATCH = 0, the hold tail is output as a tail mark. | H'FFA0<br>Bit 4 | 0 |
| | CKS3 | Serial Control Register 1 (Clock Source Select 3)<br>When CKS3 = 0, prescaler S is set for the clock source and the $SKC_1$ pin is set to output. | H'FFA0<br>Bit 3 | 0 |
| | CKS2<br>CKS1<br>CKS0 | Serial Control Register 1 (Clock Source Select 2, 1, 0)<br>When CKS2 = 0, CKS1 = 1 and CKS0 = 1, prescaler division ratio is set to 32 and the transfer clock cycle is set to 6.4 μs. | H'FFA0<br>Bit 2<br>Bit 1<br>Bit 0 | CKS2 = 0<br>CKS1 = 1<br>CKS0 = 1 |
| SCSR1 | SOL | Serial Control/Status Register 1 (Expansion Data Bit)<br>When SOL = 0, the $SO_1$ pin output level is changed to low.<br>When SOL = 1, the $SO_1$ pin output level is changed to high. | H'FFA1<br>Bit 6 | 1 |
| | MTRF | Serial Control/Status Register 1 (Tail Mark Flag)<br>When MTRF = 0, indicates that transfer wait state is entered or 8-bit/16-bit data transfer is in progress.<br>When MTRF = 1, indicates that a tail mark is being transmitted. | H'FFA1<br>Bit 1 | 0 |

| Register | | Function | Address | Setting |
|---|---|---|---|---|
| SCSR1 | STF | Serial Control/Status Register 1 (Start Flag)<br>When STF = 0, transfer operation is complete.<br>When STF = 1, transfer operation starts. | H'FFA1<br>Bit 0 | 0 |
| SDRU | | Serial Data Register U<br>Stores upper 8 bits of transmit data during 16-bit transfer | H'FFA2 | — |
| SDRL | | Serial Data Register L<br>Stores lower 8 bits of transmit data during 16-bit transfer | H'FFA3 | — |
| IENR2 | IENS1 | Interrupt Enable Register 2 (SCI1 Interrupt Enable)<br>When IENS1 = 0, SCI1 interrupt requests are disabled.<br>When IENS1 = 1, SCI1 interrupt requests are enabled. | H'FFF5<br>Bit 4 | 0 |
| IRR2 | IRRS1 | Interrupt Request Register 2 (SCI1 Interrupt Request Flag)<br>When IRRS1 = 0, SCI1 interrupt requests are not requested.<br>When IRRS1 = 1, SCI1 interrupt requests are requested. | H'FFF8<br>Bit 4 | 0 |
| PMR3 | SO1 | Port Mode Register 3 ($P3_2$/$SO_1$ Pin Function Switch)<br>When SO1 = 1, this pin functions as $SO_1$ output pin. | H'FFFD<br>Bit 2 | 1 |
| | SCK1 | Port Mode Register 3 ($P3_0$/$SCK_1$ Pin Function Switch)<br>When SCK1 = 1, this pin functions as $SCK_1$ input/output pin. | H'FFFD<br>Bit 0 | 1 |
| PMR7 | POF1 | Port Mode Register 7 ($P3_2$/$SO_1$ Pin PMOS Control)<br>When POF1 = 1, NMOS open drain output is selected. | H'FFFF<br>Bit 0 | 1 |

## 4.4 Description of RAM

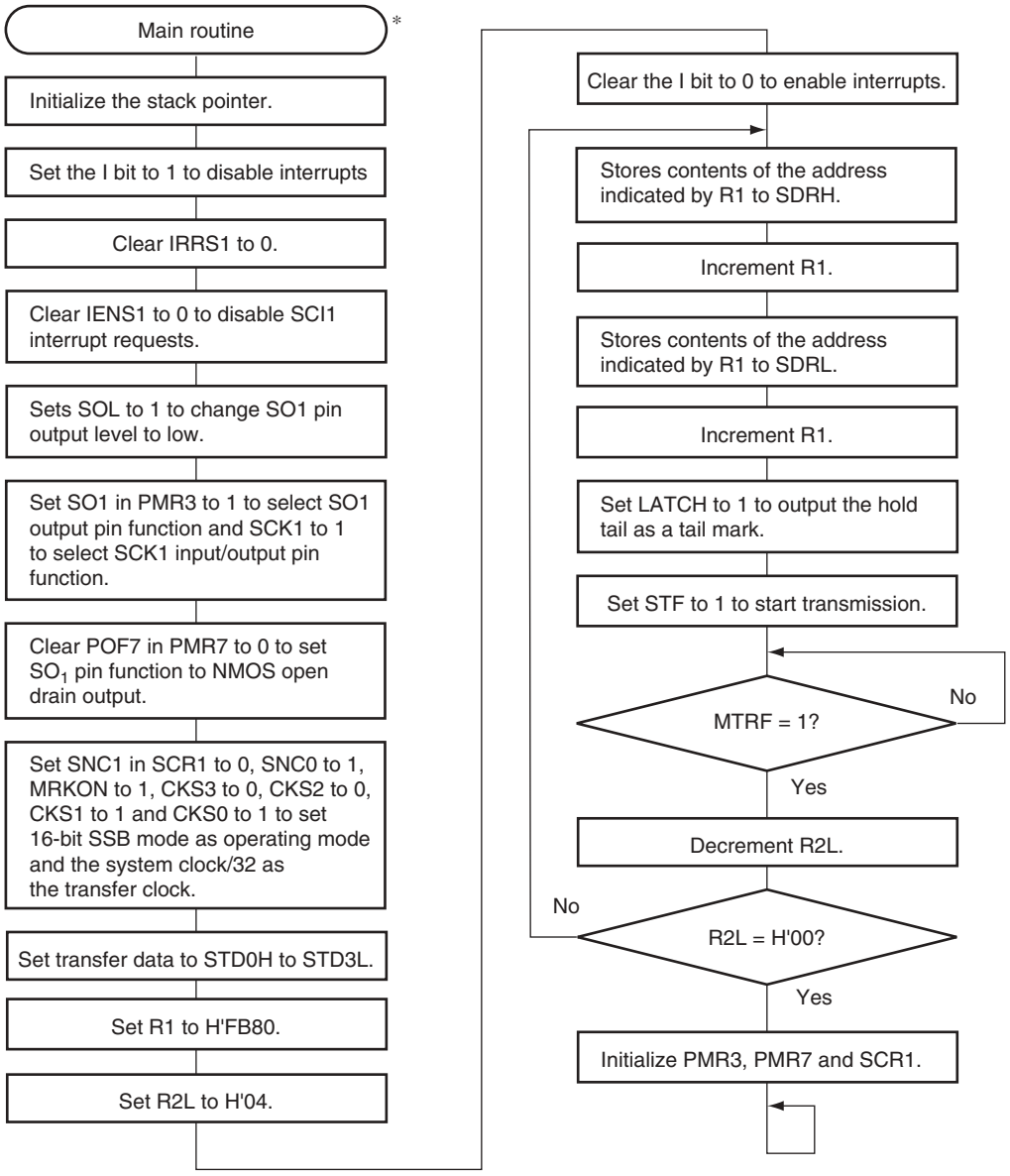
Table 4.4 describes the RAM used in this sample task.

**Table 4.4 Description of RAM**

| Label | Function | Address | Used in |
|---|---|---|---|
| STD0H | Stores the upper 8 bits of 16-bit transmit data in the 1st frame | H'FB80 | Main routine |
| STD0L | Stores the lower 8 bits of 16-bit transmit data in the 1st frame | H'FB81 | Main routine |
| STD1H | Stores the upper 8 bits of 16-bit transmit data in the 2nd frame | H'FB82 | Main routine |
| STD1L | Stores the lower 8 bits of 16-bit transmit data in the 2nd frame | H'FB83 | Main routine |
| STD2H | Stores the upper 8 bits of 16-bit transmit data in the 3rd frame | H'FB84 | Main routine |
| STD2L | Stores the lower 8 bits of 16-bit transmit data in the 3rd frame | H'FB85 | Main routine |
| STD3H | Stores the upper 8 bits of 16-bit transmit data in the 4th frame | H'FB86 | Main routine |
| STD3L | Stores the lower 8 bits of 16-bit transmit data in the 4th frame | H'FB87 | Main routine |

## 5. Flowchart

1. Main routine




Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

## 6. Program Listing

```
;*****************************************************************************************
;*                                                                                       *
;*     H8/300L Series -H8/3644,H8/3657-                                                  *
;*     Application Note                                                                  *
;*                                                                                       *
;*     'SSB Communications'                                                              *
;*                                                                                       *
;*     Function                                                                          *
;*     : Serial Communication Interface                                                  *
;*       SSB Communication                                                               *
;*                                                                                       *
;*     External Clock : 10MHz                                                            *
;*     Internal Clock :  5MHz                                                            *
;*     Sub Clock      : 32.768kHz                                                        *
;*                                                                                       *
;*****************************************************************************************
;
          .cpu         300L
;
;*****************************************************************************************
;*  Symbol Defnition                                                                     *
;*****************************************************************************************
;
SCR1      .equ         H'FFA0        ;Serial Control Register 1
SNC1      .bequ        7,SCR1        ;Select the Operation Mode 1
SNC0      .bequ        6,SCR1        ;Select the Operation Mode 0
MRKON     .bequ        5,SCR1        ;TAIL MARK Control
LTCH      .bequ        4,SCR1        ;LATCH TAIL Select
CKS3      .bequ        3,SCR1        ;Clock Source Select 3
CKS2      .bequ        2,SCR1        ;Clock Select 2
CKS1      .bequ        1,SCR1        ;Clock Select 1
CKS0      .bequ        0,SCR1        ;Clock Select 0
SCSR1     .equ         H'FFA1        ;Serial Control Status Register 1
SOL       .bequ        6,SCSR1       ;Extended Data Bit
ORER      .bequ        5,SCSR1       ;Overrun Error Flag
MTRF      .bequ        1,SCSR1       ;TAIL MARK Transmit Flag
STF       .bequ        0,SCSR1       ;Start Flag
SDRU      .equ         H'FFA2        ;Serial Data Register U
SDRL      .equ         H'FFA3        ;Serial Data Register L
IENR2     .equ         H'FFF5        ;Interrupt Enable Register 2
IENS1     .bequ        4,IENR2       ;SCI1 Interrupt Enable
IRR2      .equ         H'FFF8        ;Interrupt Request Register 2
IRRS1     .bequ        4,IRR2        ;SCI1 Interrupt Request Flag
PMR3      .equ         H'FFFD        ;Port Mode Register 3
SO1       .bequ        2,PMR3        ;P32/SO1 Pin Function Switch
SI1       .bequ        1,PMR3        ;P31/SI1 Pin Function Switch
SCK1      .bequ        0,PMR3        ;P30/SCK1 Pin Function Switch
PMR7      .equ         H'FFFF        ;Port Mode Register 7
POF1      .bequ        0,PMR7        ;P32/SO1 Pin Function Switch
;
```

```
;*************************************************************************************
;*  RAM Allocation                                                                   *
;*************************************************************************************
;
STACK       .equ        H'FF80        ;Stack Pointer
STD0H       .equ        H'FB80        ;Serial Transmitting Data 0 Upper
STD0L       .equ        H'FB81        ;Serial Transmitting Data 0 Lower
STD1H       .equ        H'FB82        ;Serial Transmitting Data 1 Upper
STD1L       .equ        H'FB83        ;Serial Transmitting Data 1 Lower
STD2H       .equ        H'FB84        ;Serial Transmitting Data 2 Upper
STD2L       .equ        H'FB85        ;Serial Transmitting Data 2 Lower
STD3H       .equ        H'FB86        ;Serial Transmitting Data 3 Upper
STD3L       .equ        H'FB87        ;Serial Transmitting Data 3 Lower
;*
;*************************************************************************************
;*  Vector Address                                                                   *
;*************************************************************************************
;
            .org        H'0000
            .data.w     MAIN          ;Reset Interrupt
;
            .org        H'0008
            .data.w     MAIN          ;IRQ0 Interrupt
            .data.w     MAIN          ;IRQ1 Interrupt
            .data.w     MAIN          ;IRQ2 Interrupt
            .data.w     MAIN          ;IRQ3 Interrupt
            .data.w     MAIN          ;INT0 - INT7 Interrupt
;
            .org        H'0014
            .data.w     MAIN          ;Timer A Interrupt
            .data.w     MAIN          ;Timer B1 Interrupt
;
            .org        H'0020
            .data.w     MAIN          ;Timer X Interrupt
            .data.w     MAIN          ;Timer V Interrupt
;
            .org        H'0026
            .data.w     MAIN          ;SCI1 Interrupt
;
            .org        H'002A
            .data.w     MAIN          ;SCI3 Interrupt
            .data.w     MAIN          ;A/D Converter Interrupt
            .data.w     MAIN          ;SLEEP Instruction Executed Interrupt
;
```

```
;*************************************************************************************
;*  Main Program                                                                     *
;*************************************************************************************
;
          .org          H'1000
;
MAIN      .equ          $
          MOV.W         #STACK,SP     ;Initialize Stack Pointer
          ORC           #H'80,CCR     ;Interrupt Disable
;
          BCLR          IRRS1         ;Clear IRRS1
          BCLR          IENS1         ;SCI1 Interrupt Disable
;
          BSET          SOL           ;Initialize SO1 Terminal Output Level
          MOV.B         #H'05,R0L
          MOV.B         R0L,@PMR3     ;Initialize SO1 CKS1 Terminal Function
          BSET          POF1          ;Initialize SO1 Terminal NMOS Open-Drain Output
;
          MOV.B         #H'63,R0L
          MOV.B         R0L,@SCR1     ;Initialize SSB Communication Function
;
          MOV.W         #H'0001,R0
          MOV.B         R0H,@STD0H     ;Set Serial Transmitting Data 1 Upper
          MOV.B         R0L,@STD0L     ;Set Serial Transmitting Data 1 Lower
          MOV.W         #H'0011,R0
          MOV.B         R0H,@STD1H     ;Set Serial Transmitting Data 2 Upper
          MOV.B         R0L,@STD1L     ;Set Serial Transmitting Data 2 Lower
          MOV.W         #H'0111,R0
          MOV.B         R0H,@STD2H     ;Set Serial Transmitting Data 3 Upper
          MOV.B         R0L,@STD2L     ;Set Serial Transmitting Data 3 Lower
          MOV.W         #H'1111,R0
          MOV.B         R0H,@STD3H     ;Set Serial Transmitting Data 4 Upper
          MOV.B         R0L,@STD3L     ;Set Serial Transmitting Data 4 Lower
;
          MOV.W         #H'FB80,R1     ;Initialize Serial Transmitting Data Address
          MOV.B         #H'04,R2L      ;Initialize Serial Transmitting Data Counter
;
MAIN1     .equ          $
          MOV.B         @R1,R0H        ;Load Serial Transmitting Data Upper
          MOV.B         R0H,@SDRU      ;Set Serial Transmitting Data Upper
          ADDS          #1,R1          ;Increment Serial Transmitting Data Address
;
          MOV.B         @R1,R0L        ;Load Serial Transmitting Data Lower
          MOV.B         R0L,@SDRL      ;Set Serial Transmitting Data Lower
          ADDS          #1,R1          ;Increment Serial Transmitting Data Address
;
          BCLR          LTCH           ;Set HOLD TAIL
;
          BSET          STF            ;Start Transmitting
;
```

```
MAIN2     .equ        $
          BTST        MTRF          ;MTRF = "1" ?
          BEQ         MAIN2         ;No.
;
          DEC         R2L           ;Decrement Serial Transmitting Data Counter
          BNE         MAIN1         ;Serial Transmitting Data Counter = H'00 ? No.
;
          MOV.B       #H'00,R0L
          MOV.B       R0L,@PMR3     ;Initialize SO1 & SCK1 Terminal Function
          BCLR        POF1          ;Initialize SO1 Terminal Function
          MOV.B       R0L,@SCR1     ;Initialize SCI1 Function
;
MAIN9     .equ        $
          BRA         MAIN9
;
          .end
```

## Revision Record

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Dec.19.03 | — | First edition issued |
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