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H8SX Family

Single-Master Mode Communications Using I²C Bus Interface 2 (IIC2)

Introduction

This application note describes the usage of the I²C bus interface 2 (IIC2) module in the single-master mode.

Target Device

H8SX/1664

Contents

1. Specification

- Figure 1 shows the connections for communications using the I²C bus interface 2 in single-master mode. The slave addresses and settings for the SAR_0 registers of the individual devices are listed in table 1.
- The single-master system in this sample task consists of one master device and one slave device.
- The I²C bus transfer rate is 93.75 kbits/s (kHz).

The following describes the procedures for the operation of this sample task.

1. The I²C bus interface single master transfer starts on the input of the low trigger to the $\overline{\text{IRQ0}}$ pin of the master.
2. The master transmits 4 bytes of data, which have been prepared in the on-chip ROM in advance, to the on-chip RAM on the slave side.
3. The slave device returns the 4 bytes of data received in step 2 from its on-chip RAM to the on-chip RAM on the master side.
4. The master device performs processing for random reading of the EEPROM. This includes the issuance of a new start condition and reception of the single byte of data read out from the slave.
5. The master compares the received data in its on-chip RAM with the data transmitted from its on-chip ROM, and confirms whether the two match.
6. Based on the results of this comparison, the master outputs levels on the P31 and P30 pins that indicate the result of operations.

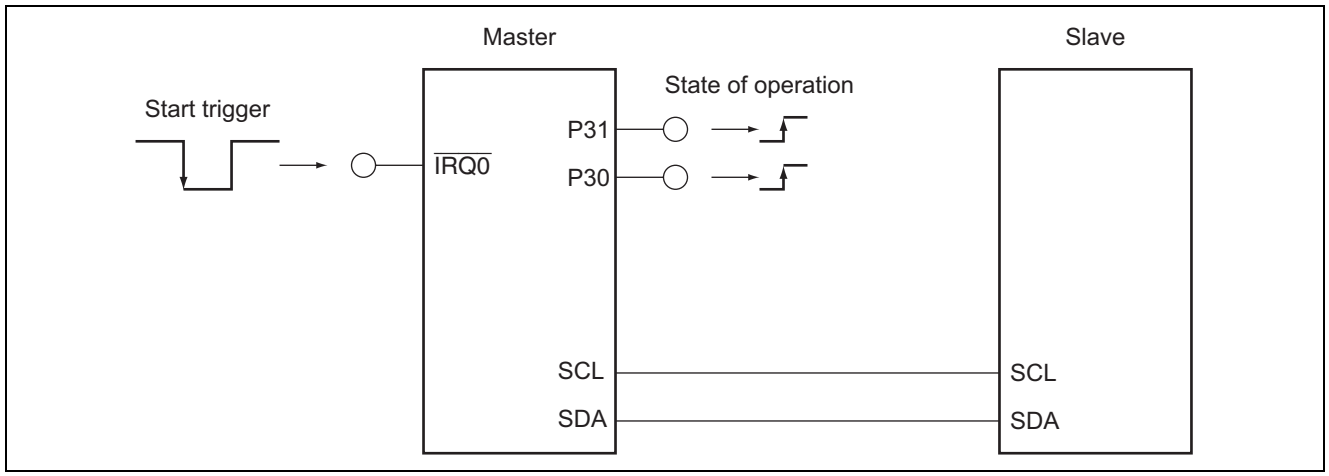


Figure 1 Connections for I²C Bus Interface 2 Single-Master Mode Communication

Table 1 Slave Addresses

Device	Slave Address	SAR_0 Setting
Master	1	H'02
Slave	3	H'06

2. Applicable Conditions

Table 2 Applicable Conditions

Items	Description	
Operating frequency	Input clock	: 12 MHz
	System clock (Iϕ)	: 24 MHz (input clock frequency × 2)
	Peripheral mode clock (Pϕ)	: 24 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 24 MHz (input clock frequency × 2)
Mode of operation	Mode 7 (MD2 = 1, MD1 = 1, MD0 = 1)	

3. Description of Functions Used

3.1 Description of I²C Bus Interface 2 (IIC2)

An I²C bus interface 2 is used in single-master operation to demonstrate bi-directional communications between in master mode and slave mode.

3.2 Master Side $\overline{\text{IRQ0}}$ Pin

The trigger to start master transmission and master reception is input to the $\overline{\text{IRQ0}}$ pin on the master side. $\overline{\text{IRQ0}}$ starts the processing of the I²C bus interface communications on the input of a falling edge on the $\overline{\text{IRQ0}}$ pin.

The master judges whether or not the $\overline{\text{IRQ0}}$ pin has received the start trigger by polling the IRQ status flag. The IRQ interrupt is not used.

3.3 Master Side P31 and P30 Pins

As indicated in table 3, the pins P31 and P30 on the master side indicate the state of I²C bus interface communications (reset state or result of operations).

Table 3 Output Values of Master Side Pins and State of Operations

P31	P30	State of Operation
0	0	Reset
0	1	Data match
1	0	Data mismatch

4. Principles of Operation

4.1 Timing of Operations in Master Transmit Mode

Figure 2 shows the timing of operations of the I²C bus interface 2 in master transmit mode. Table 4 describes processing by hardware and software at the numbered points in figure 2.

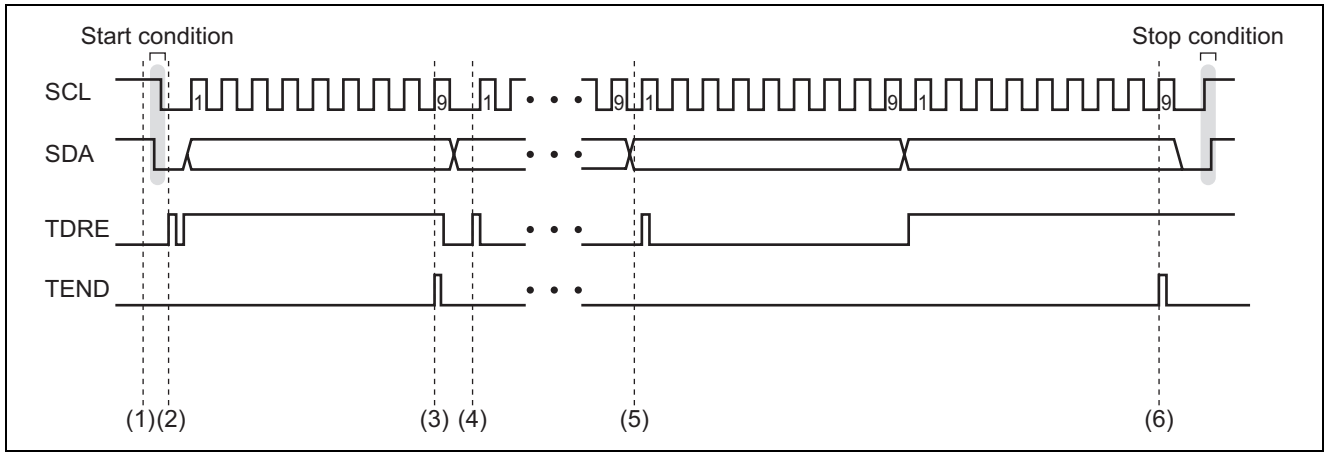


Figure 2 Timing of Operations in Master Transmit Mode

Table 4 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	a. Set the TIE bit to 1, enabling the data empty interrupt. Set the TDRE bit to 1 for interrupt generation. b. Issue the start condition.
(2)	a. Generation of transmit-data empty interrupt The start condition is detected and the TDRE is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDRT, then transmit this data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit data empty interrupts. c. Set the TEIE to 1, enabling the transmit-end interrupt. When the TEND bit is set to 1, the interrupt will be generated.
(3)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Write the data for transmission to ICDRT and transmit the data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 1, enabling the data-empty interrupt. When the TDRE bit is set to 1, the interrupt will be generated. c. Set the TEIE bit to 0, disabling the transmit-end interrupt.
(4)	a. Generation of transmit-data empty interrupt Data are transferred from ICDRT to ICDRS, and ICDRT becomes empty. Then, the TDRE bit is set to 1.	a. Write the data for transmission to ICDRT, then transmit the data. Writing to ICDRT clears the TDRE and TEND flags.

	Hardware Processing	Software Processing
(5)	a. Generation of transmit-data empty interrupt Data are transferred from ICDRT to ICDRS, and ICDRT becomes empty. Then, the TDRE bit is set to 1.	a. Write the last transmit data to ICDRT, then transmit the data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit-data empty interrupt. c. Set the TEIE bit to 1, enabling the transmit-end interrupt. When the TEND bit is set to 1, the interrupt will be generated.
(6)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Clear the TEND flag by software. b. Confirm that the SCL signal is at the low level and then issue the stop condition.

4.2 Timing of Operations in Master Receive Mode

Figures 3 and 4 show the timing of operations of the I²C bus interface 2 in master receive mode. Tables 5 and 6 describe processing by hardware and software at the numbered points in figures 3 and 4.

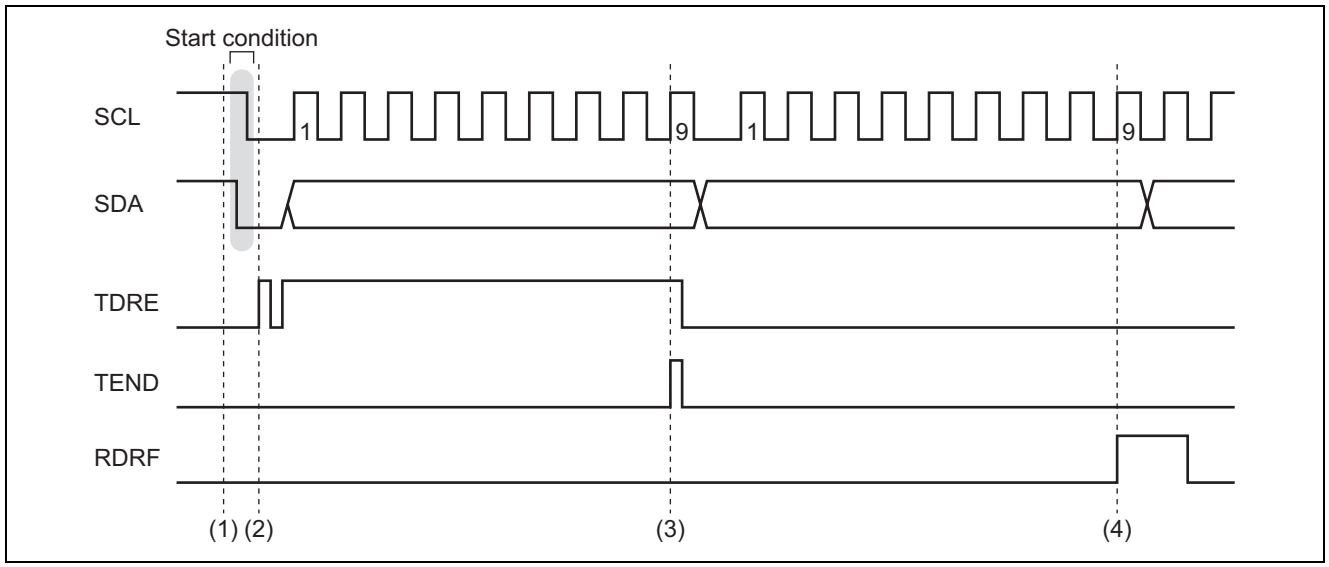


Figure 3 Timing of Operations in Master Receive Mode 1

Table 5 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	a. Set the TIE bit to 1, enabling the data empty interrupts. When the TDRE bit is set to 1, an interrupt is generated. b. Issue the start condition.
(2)	a. Generation of transmit-data empty interrupt Start condition is detected and the TDRE is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDRT, then transmit this data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit-data empty interrupt. c. Set the TEIE bit to 1, enabling the transmit-end interrupt. When the TEND bit is set to 1, the interrupt will be generated.
(3)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Set the TEIE bit to 0, disabling the transmit-end interrupt. b. Set the RIE bit to 1, enabling the receive-data full interrupt. c. Set the RCVD bit to 1, disabling the next receive operation. d. Clear the TEND flag by software. e. Set the TRS bit to 0, selecting receive mode. f. Clear the TDRE flag by software. g. Set the ACKBT bit to 0, so that 0 is output at the timing of acknowledgement output. h. Execute a dummy read of ICDRR. Reading from ICDRR clears the RDRF bit.
(4)	a. Generation of receive-data interrupt Receiving frame data is completed. On the rising edge of the ninth cycle of SCL, the RDRF bit is set to 1.	a. First byte of data for reception is read from ICDRR and saved in RAM. Reading from ICDRR clears the RDRF bit.

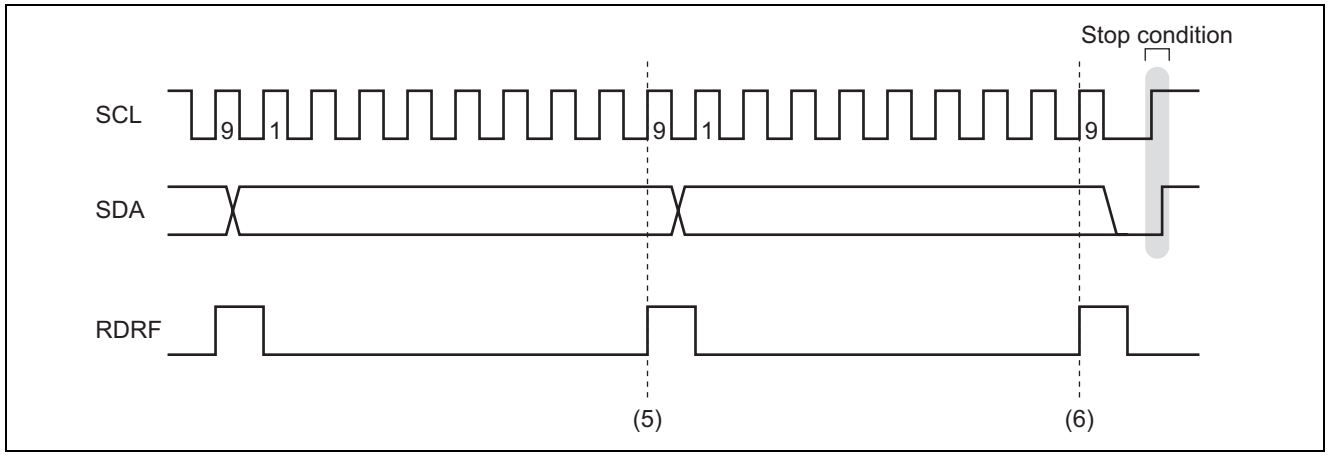


Figure 4 Timing of Operations in Master Receive Mode 2

Table 6 Description of Processing

	Hardware Processing	Software Processing
(5)	a. Generation of receive-data interrupt Receiving frame data is completed. On the rising edge of the ninth cycle of SCL, the RDRF bit is set to 1.	a. Set the ACKBT bit to 1, so that 1 is output at the timing of acknowledge output. b. Data for reception is read from ICDRR and saved in RAM. Reading from ICDRR clears the RDRF bit.
(6)	a. Generation of receive-data interrupt Receiving frame data is completed. On the rising edge of the ninth cycle of SCL, the RDRF bit is set to 1.	a. Last byte of data for reception is read from ICDRR and saved in RAM. Reading from ICDRR clears the RDRF bit. b. Set the RIE bit to 0, disabling the receive-data full interrupt. c. Confirm that the SCL signal is at the low level and then issue the stop condition.

4.3 Random Read Waveform and Interrupt Timing

Figure 5 shows the timing of operations for the I²C bus interface 2 in master transmit mode. Table 7 describes processing by hardware and software at the numbered points in figure 5.

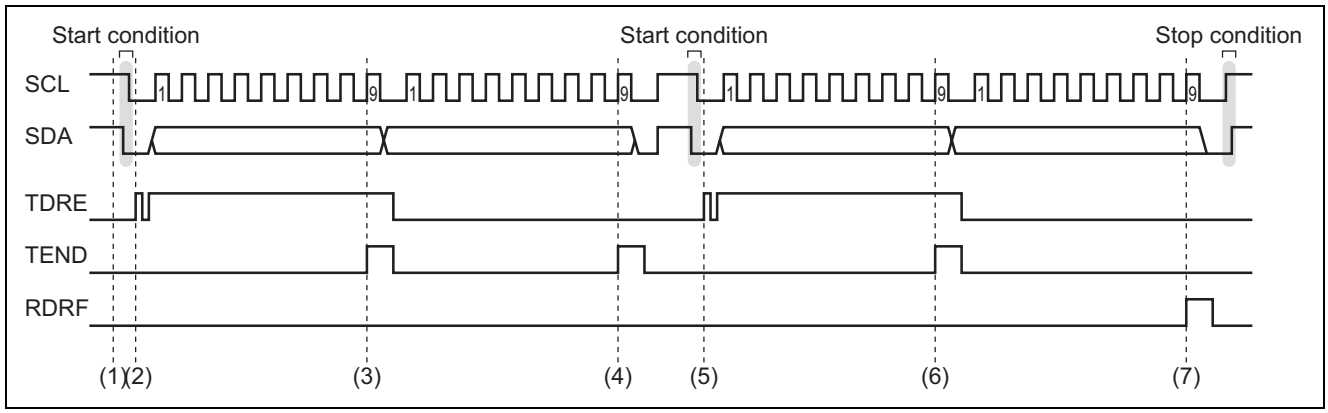


Figure 5 Timing of Operations in Master Transmit Mode

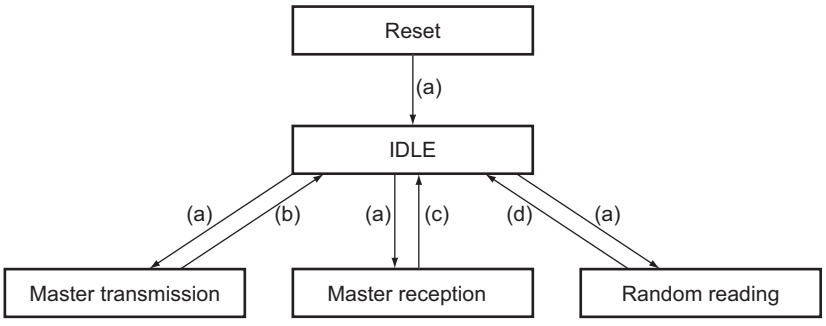
Table 7 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	a. Set the TIE bit to 1, enabling the data empty interrupts. When the TDRE bit is set to 1, an interrupt is generated. b. Issue the start condition.
(2)	a. Transmit-data empty interrupt generation Start condition is detected and the TDRE bit is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDRT, then transmit this data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit-data empty interrupt. c. Set the TEIE bit to 1, enabling the transmit-end interrupt. When the TEND bit is set to 1, the interrupt will be generated.
(3)	a. Generation of transmit-end interrupt On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Write the memory address to ICDRT and transmit the data. Writing to ICDRT clears the TDRE and TEND flags.
(4)	a. Transmit-end interrupt generation On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Set the TIE bit to 1, enabling the data-empty interrupt. Set the TDRE bit to 1 to generate the interrupt. b. Set the TEIE bit to 0, disabling the transmit-end interrupt. c. Clear the TEND flag software. d. Confirm that the SCL signal is at the low level and then issue the start condition.

	Hardware Processing	Software Processing
(5)	a. Transmit-data empty interrupt generation Start condition is detected and the TDRE bit is set to 1.	a. Write the slave-side address and data-direction bit (R/$\overline{W}$) to ICDRT, then transmit this data. Writing to ICDRT clears the TDRE and TEND flags. b. Set the TIE bit to 0, disabling the transmit-data empty interrupt. c. Set the TEIE bit to 1, enabling the transmit-end interrupt. The interrupt will be generated when the TEND bit is 1.
(6)	a. Transmit-end interrupt generation On the rising edge of the ninth cycle of SCL, the TEND bit is set to 1.	a. Set the TEIE bit to 0, disabling the transmit-end interrupt. b. Set the RIE bit to 1, enabling the receive-data full interrupt. c. Set the RCVD bit to 1, disabling next receive operation. d. Clear the TEND flag by software. e. Set the TRS bit to 0: Selects receive mode. f. Clear the TDRE flag by software. g. Set the ACKBT bit to 1: Outputs 1 at the timing of acknowledge output in receive mode. h. Execute a dummy read of ICDRR; this clears RDRF.
(7)	a. Receive-data interrupt generation After the reception of first frame data is completed, and on the rising edge of the ninth cycle of SCL, the RDRF bit is set to 1.	a. Read the final byte of received data from ICDRR and store the data in RAM. Reading ICDRR clears RDRF. b. Set the RIE bit to 0, disabling the receive-data full interrupt. c. Clear the TEND flag by software. d. Confirm that the SCL signal is at the low level and then issue the stop condition.

4.4 State Transition Diagram

Figure 6 is a state-transition diagram for this sample task. In this sample task, the idle mode is selected as the default.



(a) Transition initiated by software instruction
(b) Transition on completion of transmission or an error in communications
(c) Transition on completion of reception or an error in communications
(d) Transition on on completion of reception or an error in communications

Figure 6 State Transition Diagram

5. Description of Software

5.1 Operating Environment

Table 8 Operating Environment

Item	Detail
Development tool	High-performance Embedded Workshop Ver.4.02.00
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
H8SX compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)
Evaluation board	Master: H8SX/1663 evaluation board
	Slave: H8SX/1663 evaluation board

Table 9 Setting of Sections

Address	Section	Description
H'001000	P	Program area
	C	Data table
H'FF2000	B	Non-initialized data area (RAM area)

Table 10 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Task “Reset”	0	H'000000	init
IICI0 interrupt	116	H'0001D0	iici0_int

5.2 List of Functions

Table 11 List of Functions: main.c File

Function Name	Description
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from module stop mode, and calls the main function.
main	Main routine Selects master mode operation, judges the state of the $\overline{\text{IRQ0}}$ pin, and handles master-transmission/reception processing.

Table 12 List of Functions: iic.c File

Function Name	Description
iic_init	I²C bus interface initialization routine
mtrs_start	Sets I²C bus interface master transmission. Issues the start condition.
mrcv_start	Sets I²C bus interface master reception. Issues the start condition.
mrandrd_start	Sets random reading. Issues the start condition.
iici0_int	Handler for I²C bus interface interrupts. According to the state of operations, the functions for receiving the stop condition, master transmission, master reception, and random reading are called from this function.
receive_stop_condition	Detects the stop condition.
master_transfer	When the state of operation of this sample task is master transmission, this function for master transmission processing is called from the I²C bus interface interrupt handler. One byte of data is transferred per call of this function.
master_receive	When the state of operation of this sample task is master reception, this function for master reception processing is called from the I²C bus interface interrupt handler. One byte of data is received per call of this function.
master_randomread	When the state of operation of this sample task is random-reading, this function for random reading is called from the I²C bus interface interrupt. The function transmits the specified address and receives one byte of data from that address.

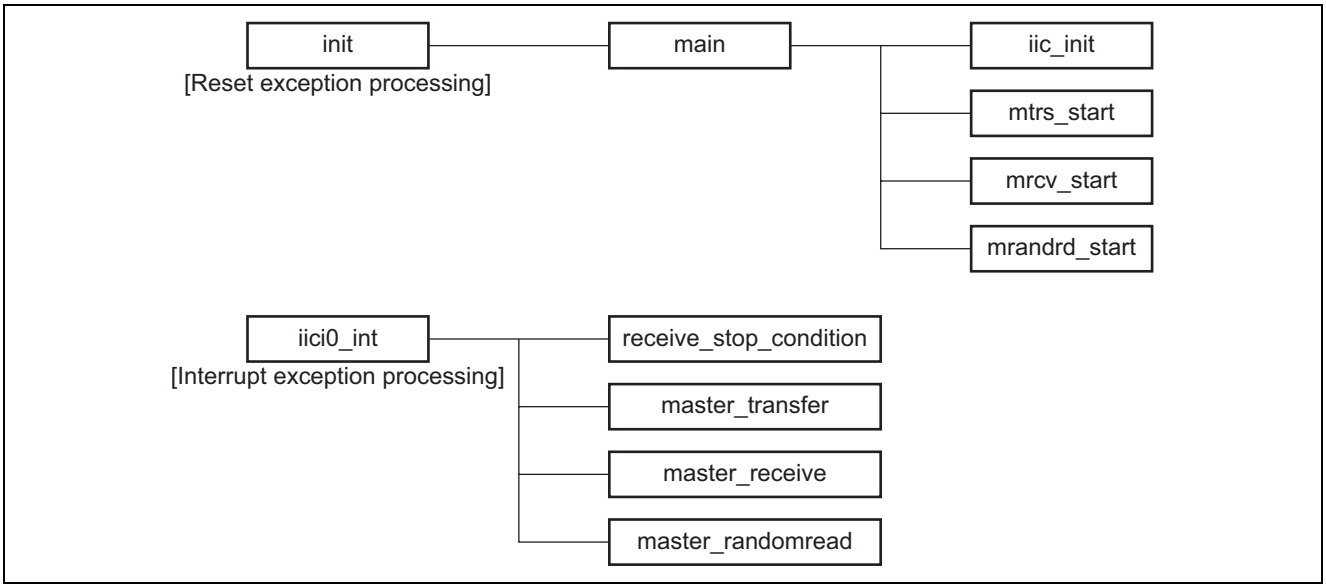


Figure 7 Hierarchy of Calls in the User Program

5.3 RAM Usage

Table 13 Description of RAM Usage

Type	Variable Name	Description	Used in
unsigned char	iic_mode	Sets state of processing by this sample task.	main iic_init mtrs_start mrcv_start mrandrd_start iici0_int receive_stop_condition
unsigned short	mt_cnt	Counter used for master transmission	iic_init mtrs_start master_transfer
unsigned short	mr_cnt	Counter used for master reception	iic_init mrcv_start receive_stop_condition master_receive
unsigned char	randrd_cnt	Counter used for random reading	iic_init mrandrd_start master_randomread
unsigned short	mt_num	Number of bytes for master transmission	mtrs_start master_transfer
unsigned short	mr_num	Number of bytes for master reception	mrcv_start receive_stop_condition master_receive
unsigned char	*mt_data	Pointer to data for transmission	mtrs_start mrandrd_start master_transfer master_randomread
unsigned char	*mr_data	Pointer to data for reception	mrcv_start mrandrd_start receive_stop_condition master_receive
unsigned char	MemAddress	Memory area used to set the address of the data for random reading from the EEPROM area	mrandrd_start
unsigned char	MRcv_dt[4]	Master-side receive area	main

5.4 Constant

Table 14 Constant

Type	Variable Name	Setting	Description	Used in
unsigned char	MTrs_dt[4]	H'81, H'01, H'02, H'03	Data for master transmission	main

5.5 Macro Constants

Table 15 Macro Constants

Variable Name	Setting	Description	Used in
DTNUM	4	Number of data for transmission/reception	main
SLAVE_ADDR	H'02	Slave address	iic_init
MT_ID	H'06	Slave address +R/$\overline{W}$(0) bit for master transmission Slave-side slave address + 0 (transmission to the slave)	master_transfer master_randomread
MR_ID	H'07	Slave address +R/$\overline{W}$(1) bit for master reception Slave-side slave address + 1 (reception from the slave)	master_receive master_randomread
MODE_MR_RAND	5	State of processing of this sample task: Random-read mode	mrandrd_start iici0_int receive_stop_condition
MODE_MT	4	State of processing of this sample task: Master transmission	mtrs_start iici0_int
MODE_MR	3	State of processing of this sample task: Master reception	mrcv_start iici0_int receive_stop_condition
MODE_IDLE	0	State of processing of this sample task: Idle	main iic_init mtrs_start mrcv_start randrd_start receive_stop_condition

5.6 Functions of File main.c

5.6.1 init Function

1. Functional overview
   Initialization routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 16). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
10	MDS2	Undefined*	R	
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by pins MD3 to MD0.

Table 16 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock signal, which is provided to the CPU, DMAC, and DTC.
8	ICK0	1	R/W	001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Adress: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

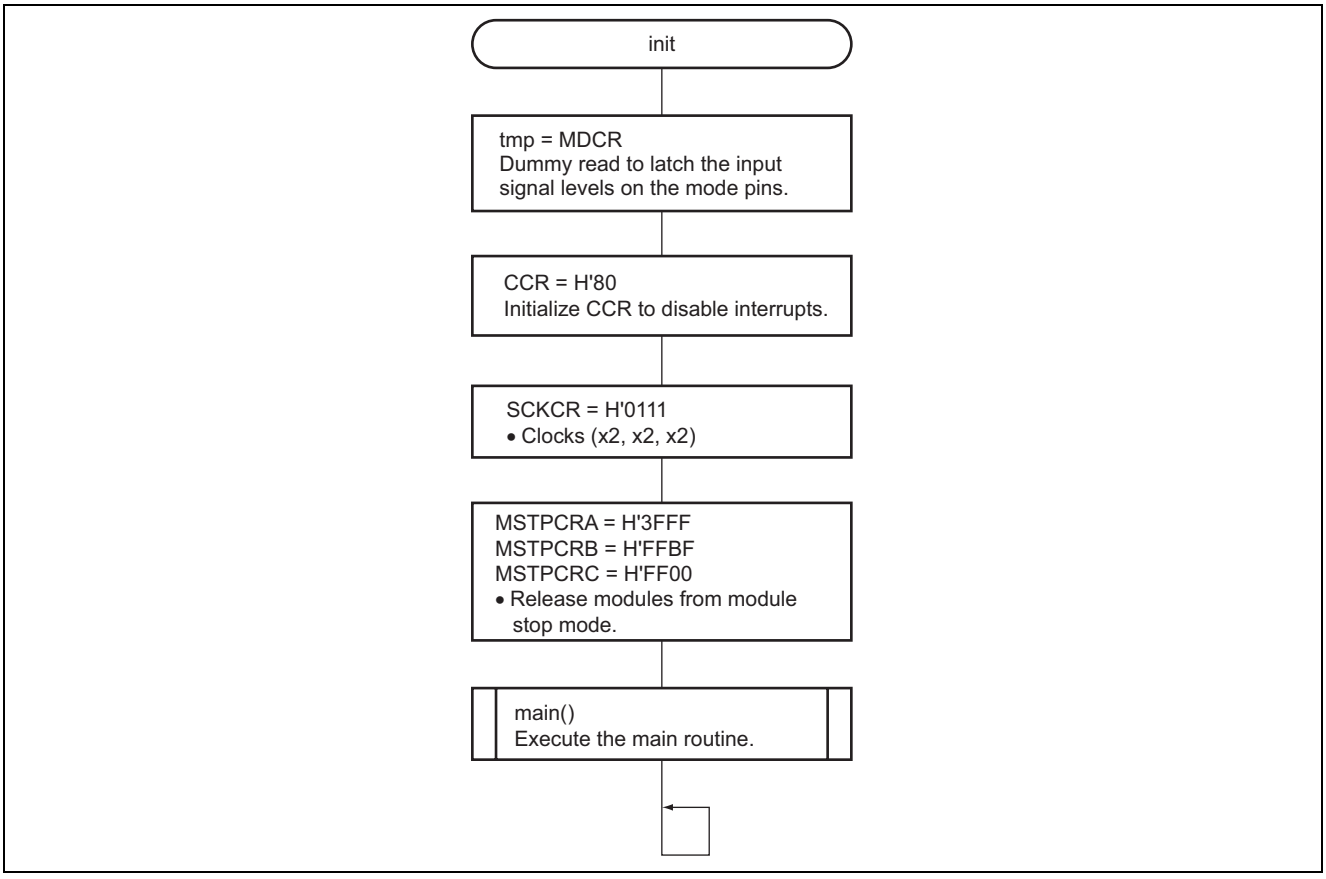
- Module stop control register B (MSTPCRB) Number of bits: 16 Adress: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I²C bus interface_1 (IIC_1)
6	MSTPB6	0	R/W	I²C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.6.2 main Function

1. Functional overview

- On falling edges of the $\overline{\text{IRQ0}}$ signal, this function performs 4-byte master transmission, 4-byte master reception and 1-byte random reading.
- Compares the master-transmission data with the master-reception data, and outputs an indicator of the results of comparison to pins P31 and P30.

2. Argument
   None

3. Return value
   None

4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

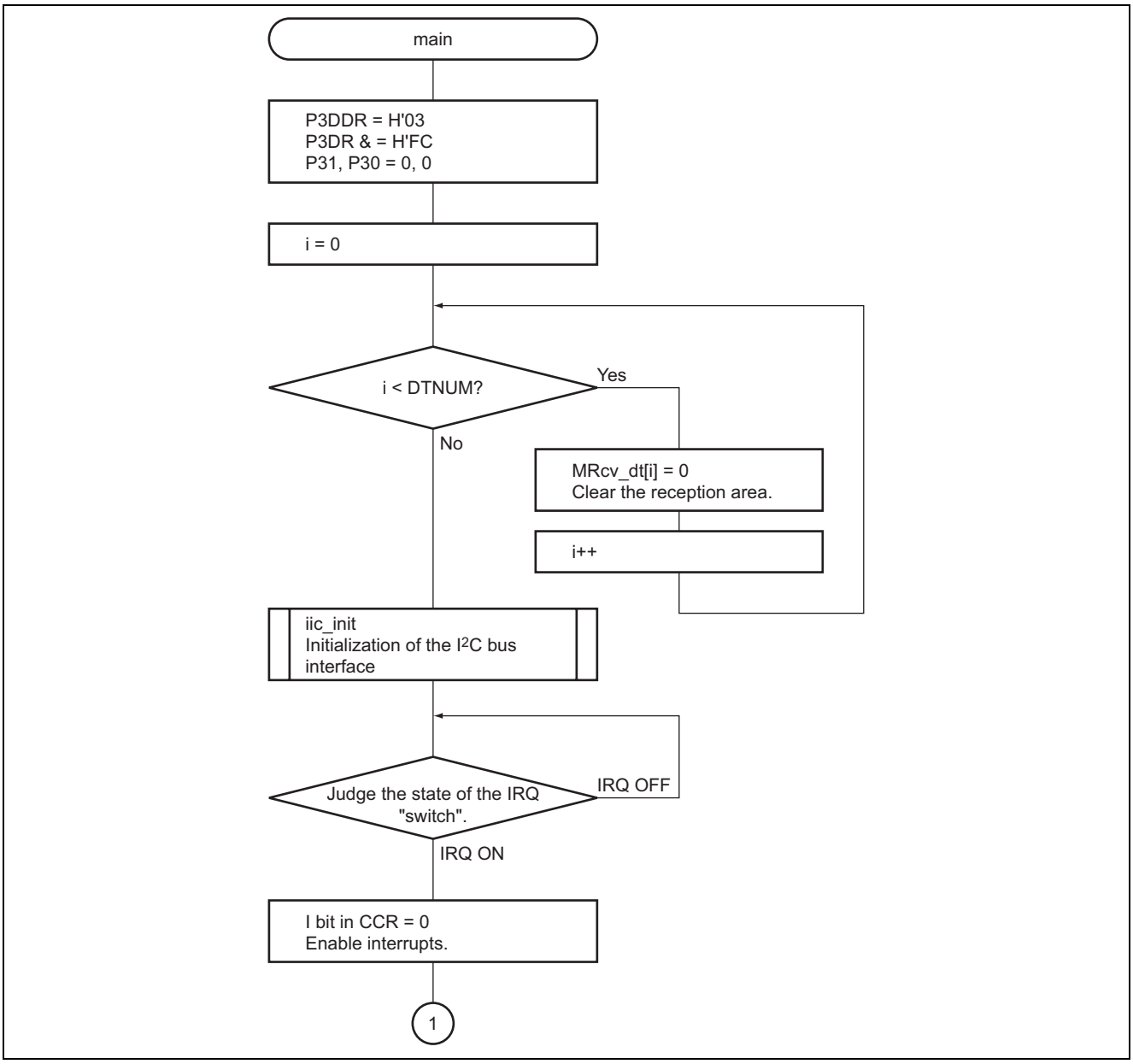
- Port 3 data direction register (P3DDR) Number of bits: 8 Address: H'FFFB82

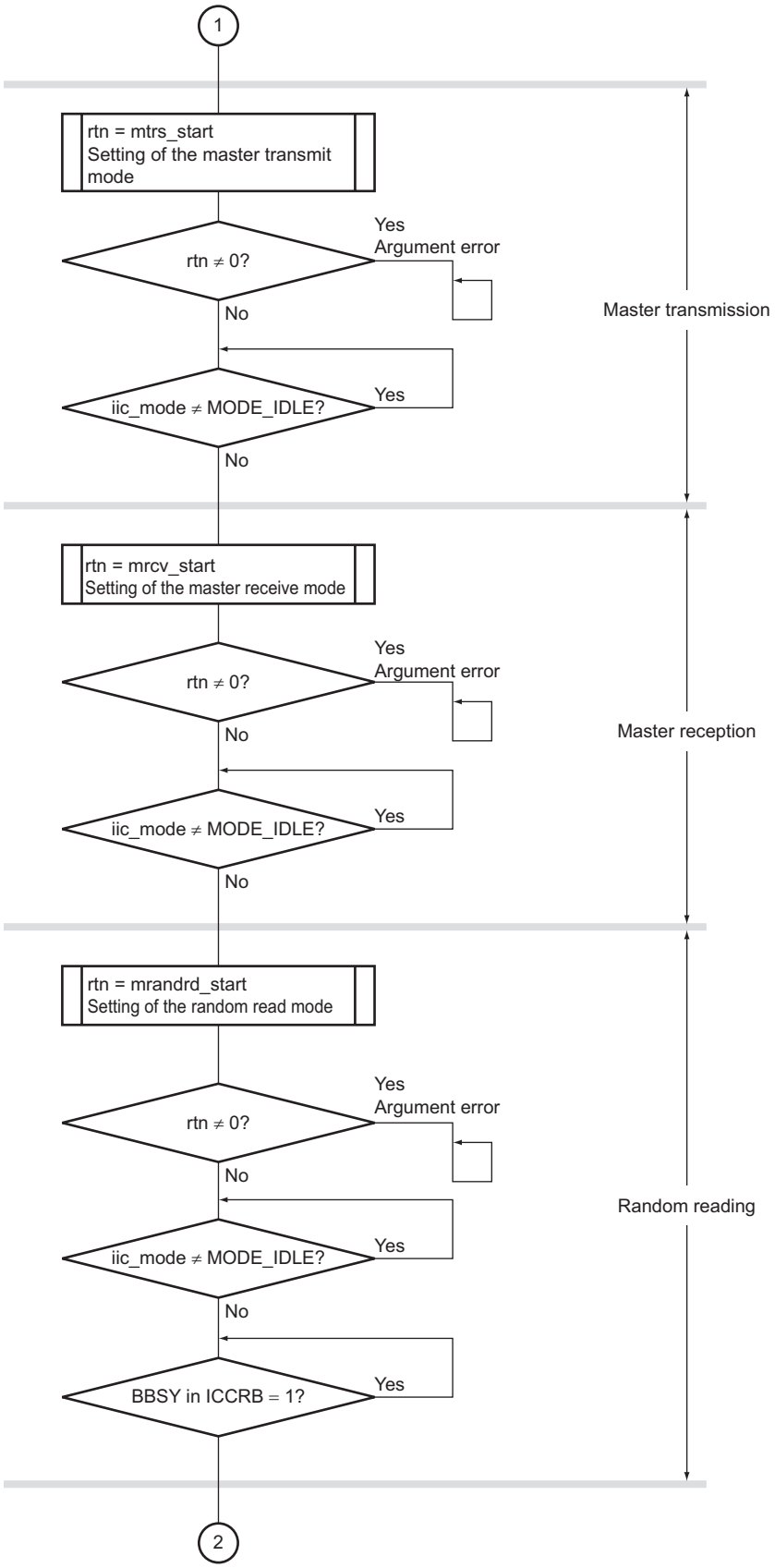
Bit	Bit Name	Setting	R/W	Description
1	P31DDR	1	R/W	0: Sets the P31 pin as an input pin. 1: Sets the P31 pin as an output pin.
0	P30DDR	1	R/W	0: Sets the P30 pin as an input pin. 1: Sets the P30 pin as an output pin.

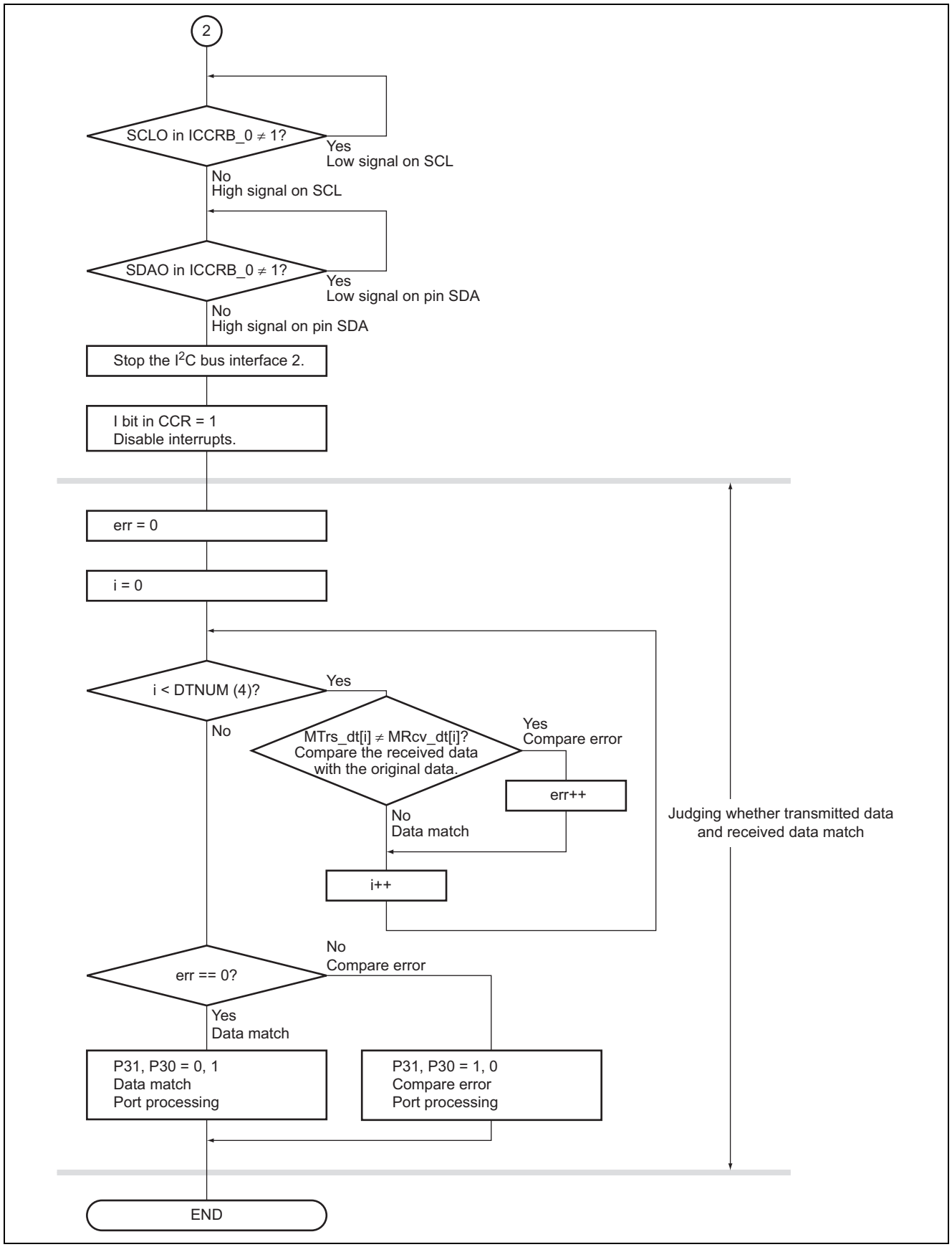
- Port 3 data register (P3DR) Number of bits: 8 Address: H'FFFF52

Bit	Bit Name	Setting	R/W	Description
1	P31DR	0/1	R/W	0: P31 pin is set to the low level. 1: P31 pin is set to the high level.
0	P30DR	0/1	R/W	0: P30 pin is set to the low level. 1: P30 pin is set to the high level.

5. Flowchart


main
P3DDR = H'03
P3DR & = H'FC
P31, P30 = 0, 0
i = 0
i < DTNUM?
Yes
No
MRcv_dt[i] = 0
Clear the reception area.
i++
iic_init
Initialization of the I²C bus interface
Judge the state of the IRQ "switch".
IRQ OFF
IRQ ON
I bit in CCR = 0
Enable interrupts.
1


1
rtn = mtrs_start
Setting of the master transmit mode
rtn ≠ 0?
Yes
Argument error
No
iic_mode ≠ MODE_IDLE?
Yes
No
Master transmission
rtn = mrcv_start
Setting of the master receive mode
rtn ≠ 0?
Yes
Argument error
No
iic_mode ≠ MODE_IDLE?
Yes
No
Master reception
rtn = mrandrd_start
Setting of the random read mode
rtn ≠ 0?
Yes
Argument error
No
iic_mode ≠ MODE_IDLE?
Yes
No
BBSY in ICCRB = 1?
Yes
Random reading
2


2
SCLO in ICCRB_0 ≠ 1?
Yes
Low signal on SCL
No
High signal on SCL
SDAO in ICCRB_0 ≠ 1?
Yes
Low signal on pin SDA
No
High signal on pin SDA
Stop the I²C bus interface 2.
I bit in CCR = 1
Disable interrupts.
err = 0
i = 0
i < DTNUM (4)?
Yes
No
MTrs_dt[i] ≠ MRcv_dt[i]?
Compare the received data with the original data.
Yes
Compare error
err++
No
Data match
i++
Judging whether transmitted data and received data match
err == 0?
No
Compare error
Yes
Data match
P31, P30 = 0, 1
Data match
Port processing
P31, P30 = 1, 0
Compare error
Port processing
END

5.7 Functions of File iic.c

5.7.1 iic_init Function

1. Functional overview
   I²C bus interface initialization routine
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Port 1 input buffer control register (P1ICR) Number of bits: 8 Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Description
7	P17ICR	1	R/W	0: Disables the input buffer of P17 (SCL0) pin. 1: Enables the input buffer of P17 (SCL0) pin.
6	P16ICR	1	R/W	0: Disables the input buffer of P16 (SDA0) pin. 1: Enables the input buffer of P16 (SDA0) pin.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
7	ICE	1	R/W	I²C Bus Interface Enable 0: Disables the IIC2 module. 1: Enables transfer via the IIC2 module (pins SCL and SDA are driving the bus).
6	RCVD	0	R/W	Reception Disable Enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables the next reception. 1: Disables the next reception.
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	00: Slave receive mode
3	CKS3	1	R/W	Transfer Clock Select 3 to 0
2	CKS2	1	R/W	1111: Transfer rate is 93.75 kbits/s with Pϕ = 24 MHz.
1	CKS1	1	R/W	
0	CKS0	1	R/W	

- I²C bus mode register_0 (ICMR_0) Number of bits: 8 Address: H'FFFEB2

Bit	Bit Name	Setting	R/W	Description
6	WAIT	0	R/W	Wait Insertion Bit This bit selects whether to insert a wait on completion of data transfer other than the acknowledge bit. When WAIT is set to 1, after the falling edge of the clock cycle for the final data bit, the low period is extended for two cycles of the transfer clock. When WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted. The setting of this bit is invalid in slave mode. Note that in usage with WAIT set to 1, when the slave device pulls SCL to the low level after the low period of SDA in the eighth and ninth clock cycles has extended for at least two cycles of the transfer clock, the high period of the ninth cycle of the transfer clock may be shortened. In such cases, the WAIT setting in this situation should be changed to 0. Except under this condition, however, there is no problem with usage.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1. 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).
6	TEIE	0	R/W	Transmit End Interrupt Enable Enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Disables the transmit end interrupt request (TEI). 1: Enables the transmit end interrupt request (TEI).
5	RIE	1	R/W	Receive Interrupt Enable Enables or disables the receive data full interrupt request (RXI) when a received data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Disables the receive data full interrupt request (RXI). 1: Enables the receive data full interrupt request (RXI).
4	NAKIE	1	R/W	NACK Receive Interrupt Enable Enables or disables the NACK receive interrupt request (NAKI) when the NACKF and AL bits in ICSR are set to 1. NAKI can be canceled by clearing the NACKF, AL, or NAKIE bit to 0. 0: Disables the NACK receive interrupt request (NAKI). 1: Enables the NACK receive interrupt request (NAKI).
3	STIE	1	R/W	Stop Condition Detection Interrupt Enable 0: Disables the stop condition detection interrupt request (STPI). 1: Enables the stop condition detection interrupt request (STPI).
2	ACKE	1	R/W	Acknowledge Bit Judgment Select 0: The value of the acknowledge bit is ignored, and continuous transfer is performed. 1: When the acknowledge bit is 1, continuous transfer is interrupted.
0	ACKBT	0	R/W	Transmit Acknowledge Specifies the bit to be sent at the acknowledge timing in receive mode. 0: 0 is output at acknowledge timing. 1: 1 is output at acknowledge timing.

- I²C bus status register_0 (ICSR_0) Number of bits: 8 Address: H'FFFEB4

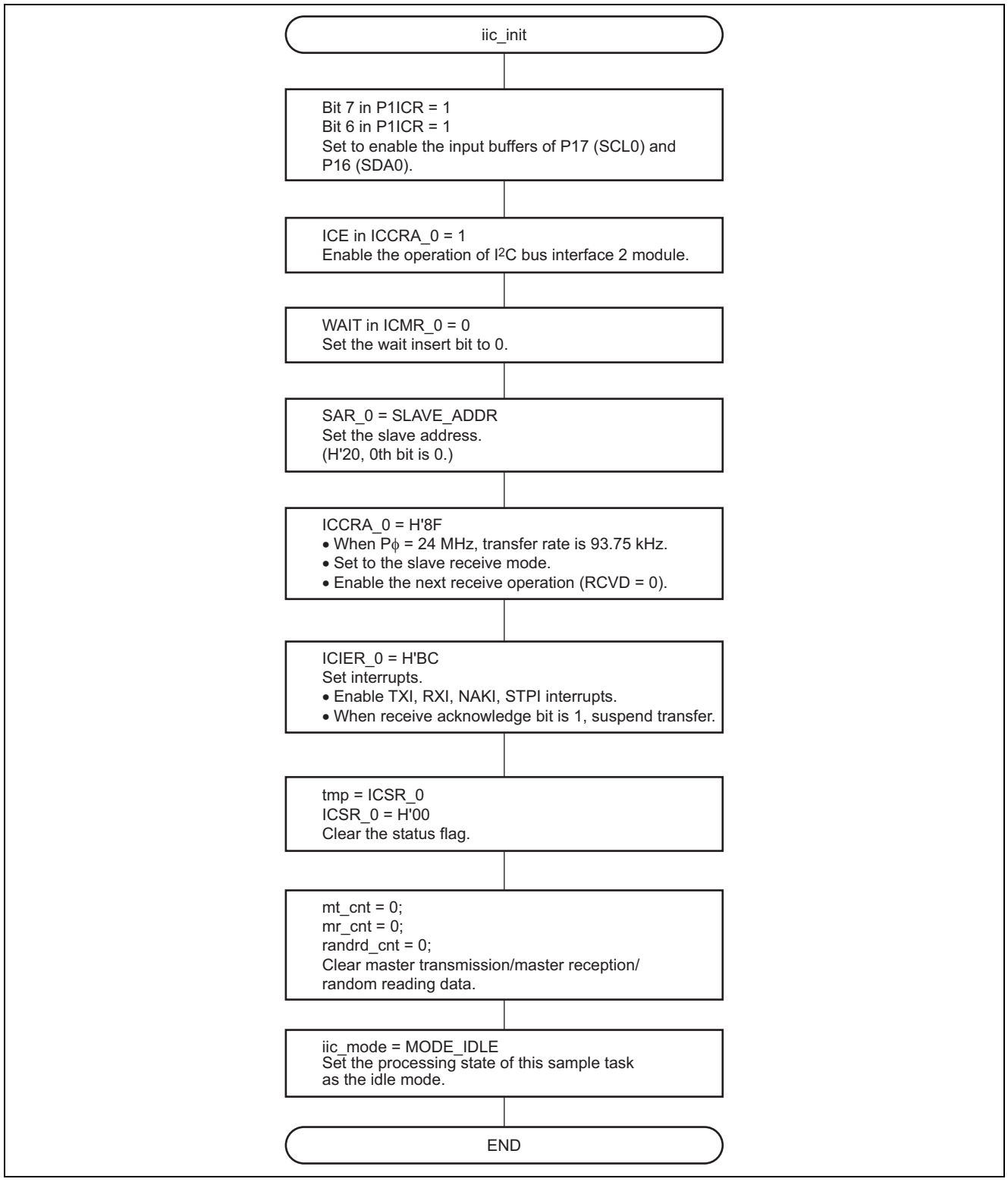
Bit	Bit Name	Setting	R/W	Description
7	TDRE	0	R/W	Transmit Data Register Empty [Setting conditions] • Transferring of data from ICDRT to ICDRS and having ICDRT empty • Setting of TRS • Issuing of a start condition (including retransmission) • Transition from the receive mode to the transmit mode has been made in the slave mode [Clearing conditions] • Writing of 0 in TDRE after reading TDRE as 1 • Writing of data in ICDRT
6	TEND	0	R/W	Transmit End [Setting condition] • Rising of the ninth clock of SCL while the TDRE flag is 1 [Clearing conditions] • Writing 0 in TEND after reading TEND as 1 • Writing of data in ICDRT
5	RDRF	0	R/W	Receive Data Register Full [Setting condition] • Transferring of received data from ICDRS to ICDRR [Clearing conditions] • Writing of 0 in RDRF after reading RDRF as 1 • Reading of data from ICDRR
4	NACKF	0	R/W	No Acknowledge Detection Flag [Setting condition] • Detection of no acknowledge from the receive device in transmission while the ACKE bit in ICIER is 1 [Clearing condition] • Writing of 0 in NACKF after reading NACKF as 1
3	STOP	0	R/W	Stop Condition Detection Flag [Setting conditions] • Detection of a stop condition after completion of frame transfer in master mode • Detection of a stop condition after match of the first-byte address after general call and detection of start condition and address set in SAR in slave mode [Clearing condition] • Writing of 0 in STOP after reading STOP as 1

Bit	Bit Name	Setting	R/W	Description
2	AL	0	R/W	Arbitration Lost Flag Indicates that arbitration was lost in the master mode. When two or more master devices attempt to seize the bus at nearly the same time, if the I²C bus interface detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been taken by another master. [Setting conditions] • Different values for the internal SDA signal and SDA pin on a rising edge of SCL in master transmit mode • The SDA pin being at the high level in master mode while a start condition is detected [Clearing condition] • Writing of 0 in AL after reading AL as 1
1	AAS	0	R/W	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 when the first frame following a start condition matches bits SVA6 to SVA0 in SAR. [Setting conditions] • Detection of the slave address in slave receive mode • Detection of the general call address in the slave receive mode [Clearing condition] • Writing of 0 in AAS after reading AAS as 1

- Slave address register_0 (SAR_0) Number of bits: 8 Address: H'FFFEB5
  The slave address is set in the SAR bits. An interface in slave mode responds as the slave device when the 7 higher-order bits of SAR match the 7 higher-order bits of the first frame received after a start condition.

Bit	Bit Name	Setting	R/W	Description
7 to1	SVA6 to SVA0	SLAVE_ADDR	R/W	Slave Address 6 to 0 Unique address setting (address differing from the addresses of other slave devices connected to the I²C bus) for the device
0	–		R/W	Reserved This bit is readable/writable. 0 should be written in writing.

5. Flowchart


iic_init
Bit 7 in P1ICR = 1
Bit 6 in P1ICR = 1
Set to enable the input buffers of P17 (SCL0) and P16 (SDA0).
ICE in ICCRA_0 = 1
Enable the operation of I²C bus interface 2 module.
WAIT in ICMR_0 = 0
Set the wait insert bit to 0.
SAR_0 = SLAVE_ADDR
Set the slave address.
(H'20, 0th bit is 0.)
ICCRA_0 = H'8F
• When Pϕ = 24 MHz, transfer rate is 93.75 kHz.
• Set to the slave receive mode.
• Enable the next receive operation (RCVD = 0).
ICIER_0 = H'BC
Set interrupts.
• Enable TXI, RXI, NAKI, STPI interrupts.
• When receive acknowledge bit is 1, suspend transfer.
tmp = ICSR_0
ICSR_0 = H'00
Clear the status flag.
mt_cnt = 0;
mr_cnt = 0;
randrd_cnt = 0;
Clear master transmission/master reception/ random reading data.
iic_mode = MODE_IDLE
Set the processing state of this sample task as the idle mode.
END

5.7.2 mtrs_start Function

1. Functional overview

This function sets up the task for I²C bus interface master transmission and issues the start condition.

2. Argument

Type	Name of Variable	Description
const unsigned char	*dtadd	First address of data for transmission
unsigned short	dtnum	Number of data to be transmitted

3. Return value

Type	Description
unsigned char	0: Starts normal transmission. 1: Transmission in progress 2: Bus busy 3: Argument error

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
5	MST	1	R/W	Master/ Slave Select
4	TRS	1	R/W	11: Master transmit mode

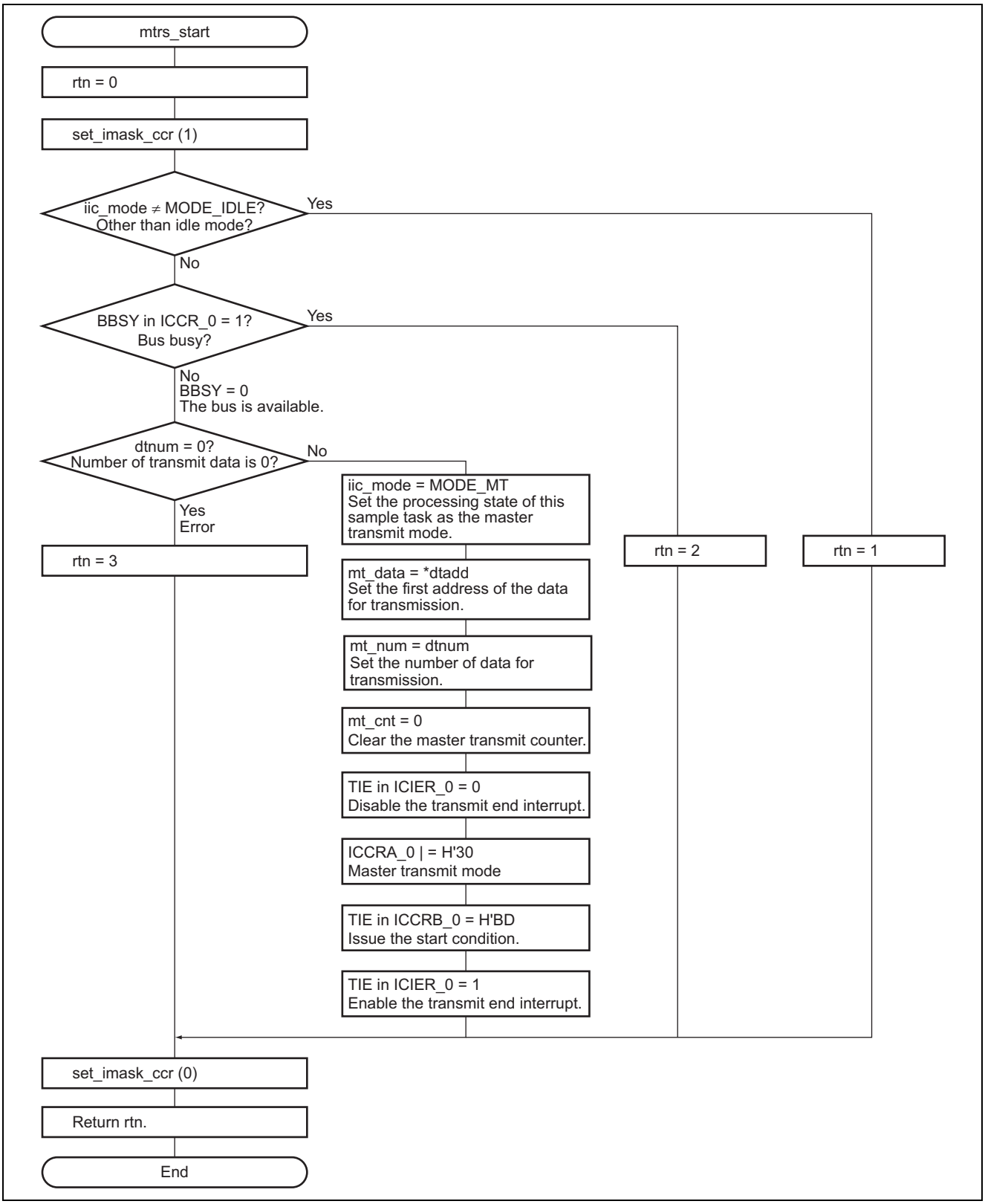
- I²C bus control register B_0 (ICCRB_0) Number of bits: 8 Address: H'FFFEB1

Bit	Bit Name	Setting	R/W	Description
7	BBSY	1	R/W	Bus Busy The BBSY flag can be read to check whether the I²C bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions. A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0. Using a MOV instruction to write 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Using a MOV instruction to write 0 in BBSY and SCP issues a stop condition.
6	SCP	0	R/W	Start Condition/Stop Condition Prohibit Bit Controls the issuing of start and stop conditions in master mode. Writing 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Writing 0 in BBSY and SCP issues a stop condition. This bit is always read as 1. Writing of 1 has no effect.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1. 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).

5. Flowchart


mtrs_start
rtn = 0
set_imask_ccr (1)
iic_mode ≠ MODE_IDLE?
Other than idle mode?
Yes
No
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
BBSY = 0
The bus is available.
dtnum = 0?
Number of transmit data is 0?
No
Yes
Error
rtn = 3
iic_mode = MODE_MT
Set the processing state of this sample task as the master transmit mode.
mt_data = *dtadd
Set the first address of the data for transmission.
mt_num = dtnum
Set the number of data for transmission.
mt_cnt = 0
Clear the master transmit counter.
TIE in ICIER_0 = 0
Disable the transmit end interrupt.
ICCRA_0 | = H'30
Master transmit mode
TIE in ICCRB_0 = H'BD
Issue the start condition.
TIE in ICIER_0 = 1
Enable the transmit end interrupt.
rtn = 2
rtn = 1
set_imask_ccr (0)
Return rtn.
End

5.7.3 mrcv_start Function

1. Functional overview

This function sets up the task for I²C bus interface master reception and issues the start condition.

2. Argument

Type	Name of Variable	Description
const unsigned char	*dtadd	First address of received data
unsigned short	dtnum	Number of data to be received

3. Return value

Type	Description
unsigned char	0: Starts normal transmission. 1: Transmission in progress 2: Bus busy 3: Argument error

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
5	MST	1	R/W	Master/Slave Select
4	TRS	1	R/W	11: Master transmit mode

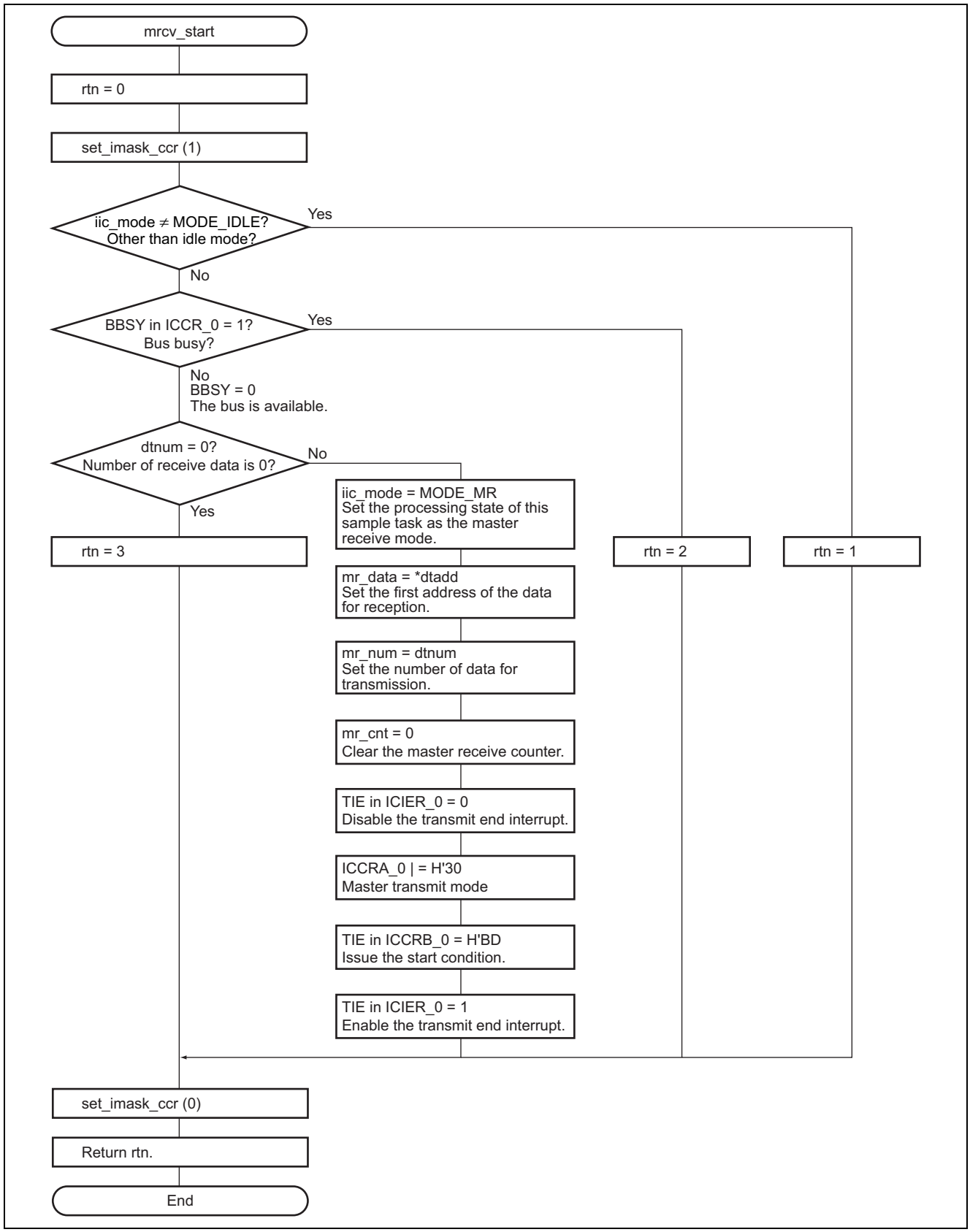
- I²C bus control register B_0 (ICCRB_0) Number of bits: 8 Address: H'FFFEB1

Bit	Bit Name	Setting	R/W	Description
7	BBSY	1	R/W	Bus Busy The BBSY flag can be read to check whether the I²C bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions. A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0. Using a MOV instruction to write 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Using a MOV instruction to write 0 in BBSY and SCP issues a stop condition.
6	SCP	0	R/W	Start Condition/Stop Condition Prohibit Bit Controls the issuing of start and stop conditions in master mode. Writing 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Writing 0 in BBSY and SCP issues a stop condition. This bit is always read as 1. Writing of 1 has no effect.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1. 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).

5. Flowchart


mrcv_start
rtn = 0
set_imask_ccr (1)
iic_mode ≠ MODE_IDLE?
Other than idle mode?
Yes
No
BBSY in ICCR_0 = 1?
Bus busy?
Yes
No
BBSY = 0
The bus is available.
dtnum = 0?
Number of receive data is 0?
No
Yes
rtn = 3
iic_mode = MODE_MR
Set the processing state of this sample task as the master receive mode.
mr_data = *dtadd
Set the first address of the data for reception.
mr_num = dtnum
Set the number of data for transmission.
mr_cnt = 0
Clear the master receive counter.
TIE in ICIER_0 = 0
Disable the transmit end interrupt.
ICCRA_0 | = H'30
Master transmit mode
TIE in ICCRB_0 = H'BD
Issue the start condition.
TIE in ICIER_0 = 1
Enable the transmit end interrupt.
rtn = 2
rtn = 1
set_imask_ccr (0)
Return rtn.
End

5.7.4 mrandrd_start Function

1. Functional overview
   This function sets up the task for random reading, including issuance of a start condition to initiate reading from the EEPROM.

2. Argument

Type	Name of Variable	Description
const unsigned char	*mrbuf	Location where the random-read data is to be stored
unsigned short	mtbuf	EEPROM memory address

3. Return value
   None

4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
5	MST	1	R/W	Master/Slave Select
4	TRS	1	R/W	11: Master transmit mode

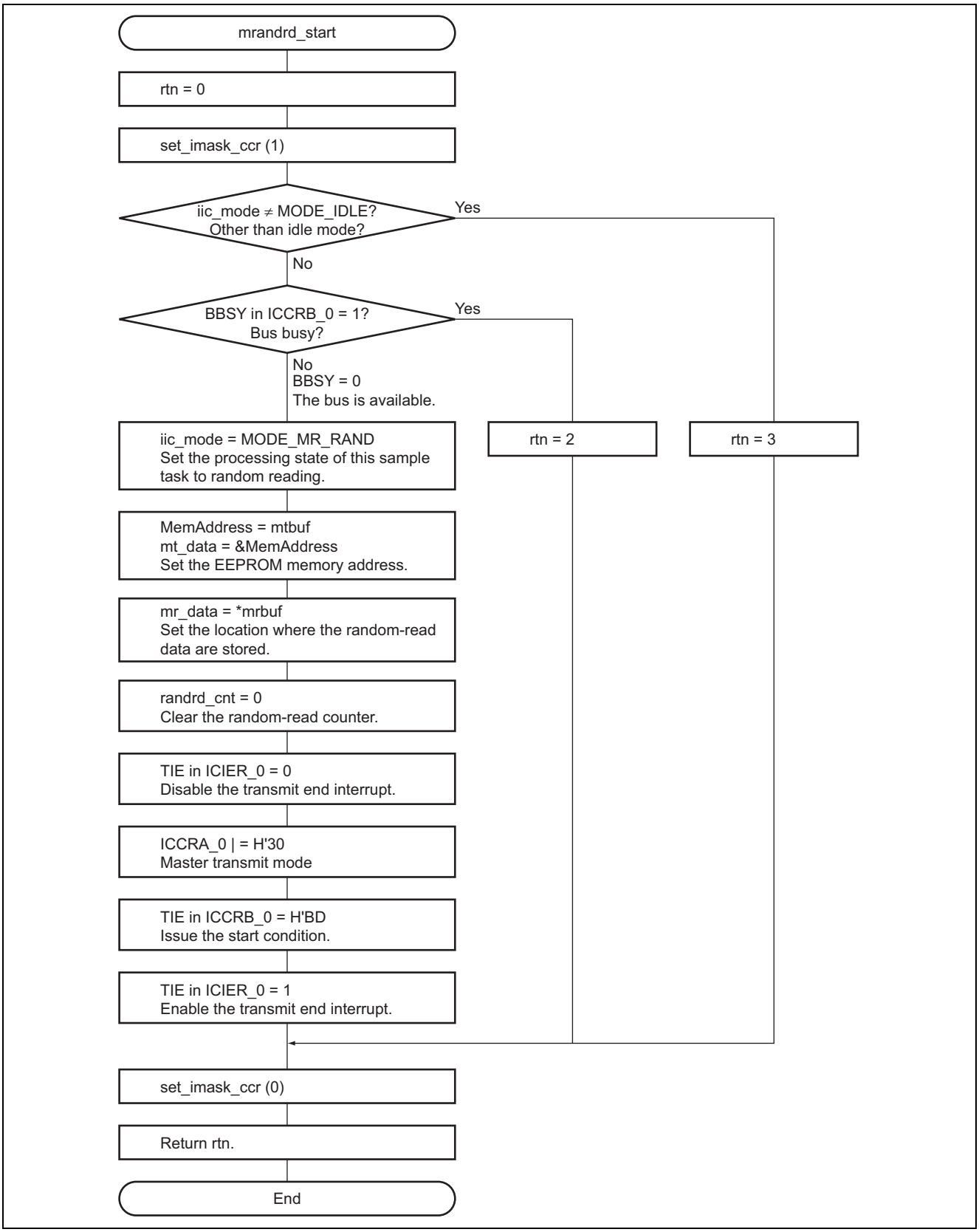
- I²C bus control register B_0 (ICCRB_0) Number of bits: 8 Address: H'FFFEB1

Bit	Bit Name	Setting	R/W	Description
7	BBSY	1	R/W	Bus Busy The BBSY flag can be read to check whether the I²C bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions. A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0. Using a MOV instruction to write 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Using a MOV instruction to write 0 in BBSY and SCP issues a stop condition.
6	SCP	0	R/W	Start Condition/Stop Condition Prohibit Bit Controls the issuing of start and stop conditions in master mode. Writing 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Writing 0 in BBSY and SCP issues a stop condition. This bit is always read as 1. Writing of 1 has no effect.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1. 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).

5. Flowchart


mrandrd_start
rtn = 0
set_imask_ccr (1)
iic_mode ≠ MODE_IDLE?
Other than idle mode?
Yes
No
BBSY in ICCRB_0 = 1?
Bus busy?
Yes
No
BBSY = 0
The bus is available.
iic_mode = MODE_MR_RAND
Set the processing state of this sample task to random reading.
rtn = 2
rtn = 3
MemAddress = mtbuf
mt_data = &MemAddress
Set the EEPROM memory address.
mr_data = *mrbuf
Set the location where the random-read data are stored.
randrd_cnt = 0
Clear the random-read counter.
TIE in ICIER_0 = 0
Disable the transmit end interrupt.
ICCRA_0 | = H'30
Master transmit mode
TIE in ICCRB_0 = H'BD
Issue the start condition.
TIE in ICIER_0 = 1
Enable the transmit end interrupt.
set_imask_ccr (0)
Return rtn.
End

5.7.5 iici0_int Function

1. Functional overview
   Handler for I²C bus interface interrupts. According to the state of operations, this function calls the functions for receiving the stop condition, master transmission and master reception, and random reading.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

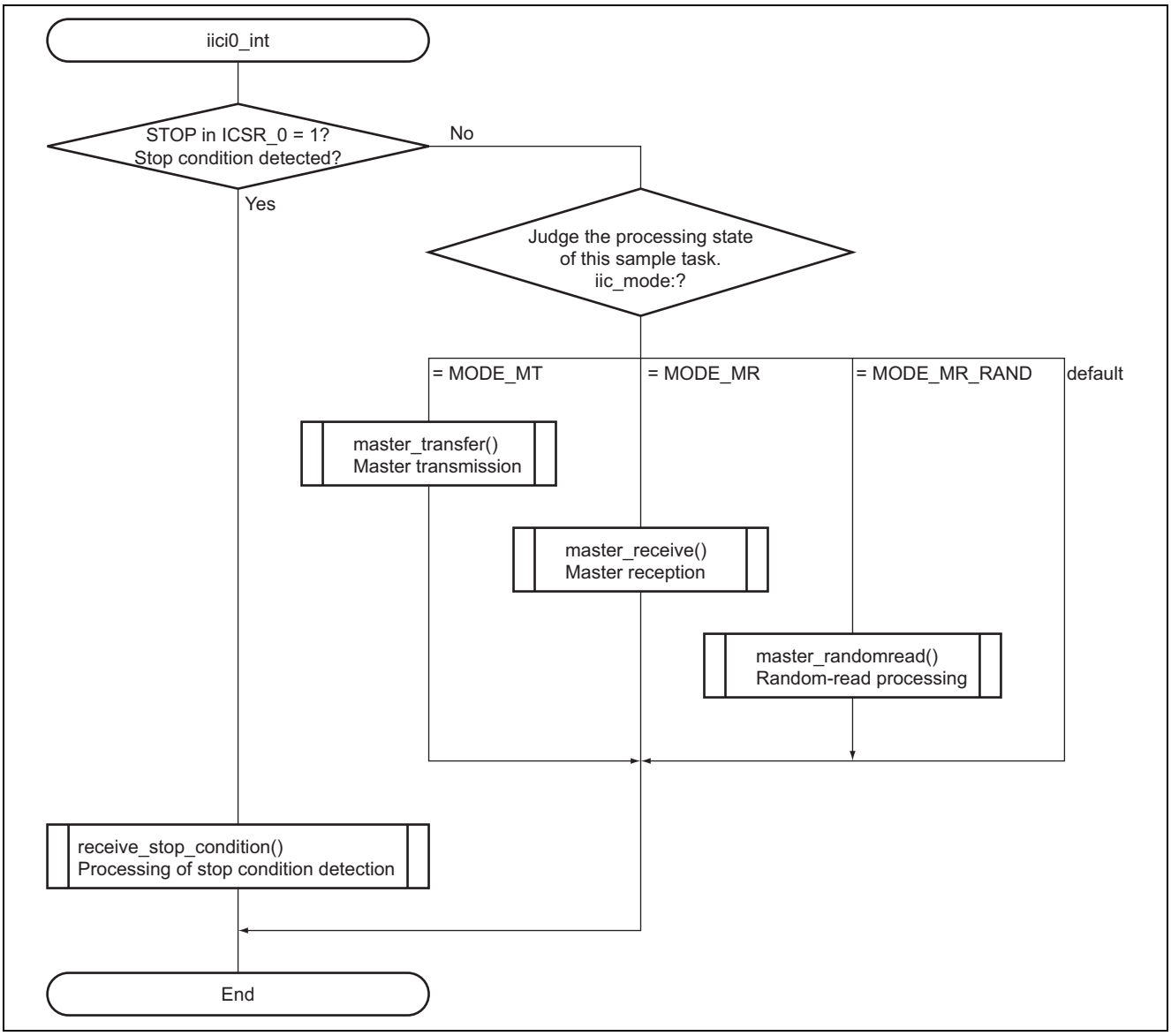
- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
4	TRS	Undefined	R/W	Master/Slave Select 0: Receive mode 1: Transmit mode

- I²C bus status register_0 (ICSR_0) Number of bits: 8 Address: H'FFFEB4

Bit	Bit Name	Setting	R/W	Description
3	STOP	Undefined	R/W	Stop Condition Detection Flag [Setting conditions] • Detection of a stop condition after completion of frame transfer in master mode • Detection of a stop condition after match of the first-byte address after general call and detection of start condition and address set in SAR in slave mode [Clearing condition] • Writing 0 in STOP after reading STOP as 1

5. Flowchart


iici0_int
STOP in ICSR_0 = 1?
Stop condition detected?
No
Yes
Judge the processing state
of this sample task.
iic_mode:?
= MODE_MT
= MODE_MR
= MODE_MR_RAND
default
master_transfer()
Master transmission
master_receive()
Master reception
master_randomread()
Random-read processing
receive_stop_condition()
Processing of stop condition detection
End

5.7.6 receive_stop_condition Function

1. Functional overview
   This function handles processing on detection of the stop condition.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
6	RCVD	0	R/W	Reception Disable Enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables the next reception. 1: Disables the next reception.
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	00: Slave receive mode

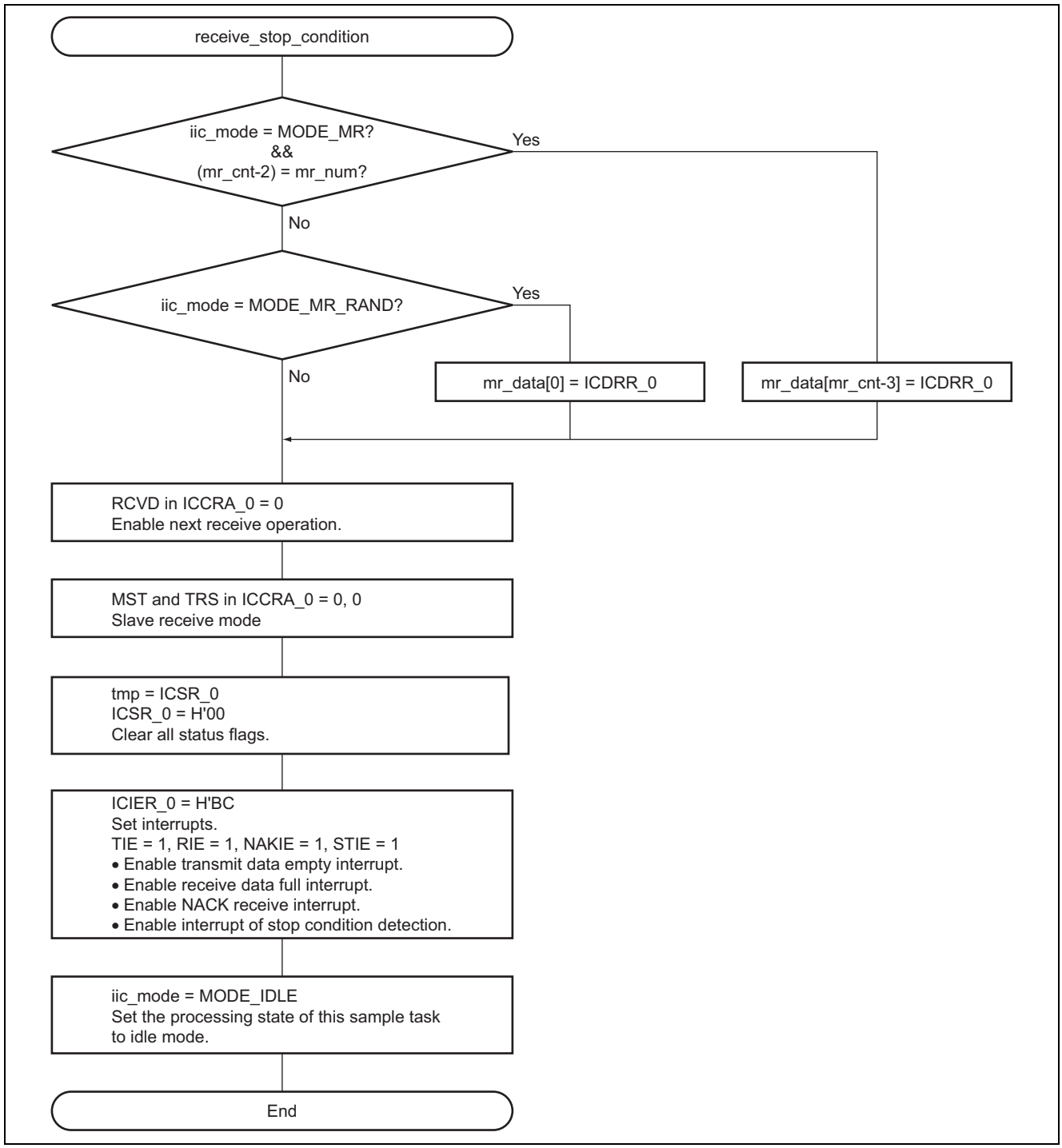
- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1. 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).
6	TEIE	0	R/W	Transmit End Interrupt Enable Enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Disables the transmit end interrupt request (TEI). 1: Enables the transmit end interrupt request (TEI).
5	RIE	1	R/W	Receive Interrupt Enable Enables or disables the receive data full interrupt request (RXI) when a received data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Disables the receive data full interrupt request (RXI). 1: Enables the receive data full interrupt request (RXI).
4	NAKIE	1	R/W	NACK Receive Interrupt Enable Enables or disables the NACK receive interrupt request (NAKI) when the NACKF and AL bits in ICSR are set to 1. NAKI can be canceled by clearing the NACKF, AL, or NAKIE bit to 0. 0: Disables the NACK receive interrupt request. 1: Enables the NACK receive interrupt request.
3	STIE	1	R/W	Stop Condition Detection Interrupt Enable 0: Disables the stop condition detection interrupt request (STPI). 1: Enables the stop condition detection interrupt request (STPI).
2	ACKE	1	R/W	Acknowledge Bit Judgment Select 0: The value of the acknowledge bit is ignored, and continuous transfer is performed. 1: When the acknowledge bit is 1, continuous transfer is interrupted.
0	ACKBT	0	R/W	Transmit Acknowledge Specifies the bit to be sent at the acknowledge timing in receive mode. 0: 0 is output at acknowledge timing. 1: 1 is output at acknowledge timing.

- I²C bus status register_0 (ICSR_0) Number of bits: 8 Address: H'FFFEB4

Bit	Bit Name	Setting	R/W	Description
7	TDRE	0	R/W	Transmit Data Register Empty [Setting conditions] • Transferring of data from ICDRT to ICDRS and having ICDRT empty • Setting of TRS • Issuing of a start condition (including retransmission) • Transition from the receive mode to the transmit mode has been made in the slave mode [Clearing conditions] • Writing of 0 in TDRE after reading it as 1 • Writing of data in ICDRT
4	NACKF	0	R/W	No Acknowledge Detection Flag [Setting condition] • Detection of no acknowledge from the receive device in transmission while the ACKE bit in ICIER is 1 [Clearing condition] • Writing of 0 in NACKF after reading it as 1
1	AAS	0	R/W	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 when the first frame following a start condition matches bits SVA6 to SVA0 in SAR. [Setting conditions] • Detection of the slave address in slave receive mode • Detection of the general call address in the slave receive mode [Clearing condition] • Writing of 0 in AAS after reading AAS as 1

5. Flowchart


receive_stop_condition
iic_mode = MODE_MR?
&&
(mr_cnt-2) = mr_num?
Yes
No
iic_mode = MODE_MR_RAND?
Yes
No
mr_data[0] = ICDRR_0
mr_data[mr_cnt-3] = ICDRR_0
RCVD in ICCRA_0 = 0
Enable next receive operation.
MST and TRS in ICCRA_0 = 0, 0
Slave receive mode
tmp = ICSR_0
ICSR_0 = H'00
Clear all status flags.
ICIER_0 = H'BC
Set interrupts.
TIE = 1, RIE = 1, NAKIE = 1, STIE = 1
• Enable transmit data empty interrupt.
• Enable receive data full interrupt.
• Enable NACK receive interrupt.
• Enable interrupt of stop condition detection.
iic_mode = MODE_IDLE
Set the processing state of this sample task
to idle mode.
End

5.7.7 master_transfer Function

1. Functional overview
   Master-transmission processing which is called from the I²C bus interface interrupt handler. In this case, the interrupt source will be the transmit data empty interrupt for each byte of transmitted data. When arbitration is lost, it places the interface in slave receive mode.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register B_0 (ICCRB_0) Number of bits: 8 Address: H'FFFEB1

Bit	Bit Name	Setting	R/W	Description
3	SCLO	1	R/W	Monitors level of signal output from SCL. When the SCLO bit is set to 1 in reading, the signal output from SCL is at high level. When the SCLO bit is set to 0 in reading, the signal output from SCL is at low level.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1. 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).
6	TEIE	0	R/W	Transmit End Interrupt Enable Enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Disables the transmit end interrupt request (TEI). 1: Enables the transmit end interrupt request (TEI).

- I²C bus status register_0 (ICSR_0) Number of bits: 8 Address: H'FFFEB4

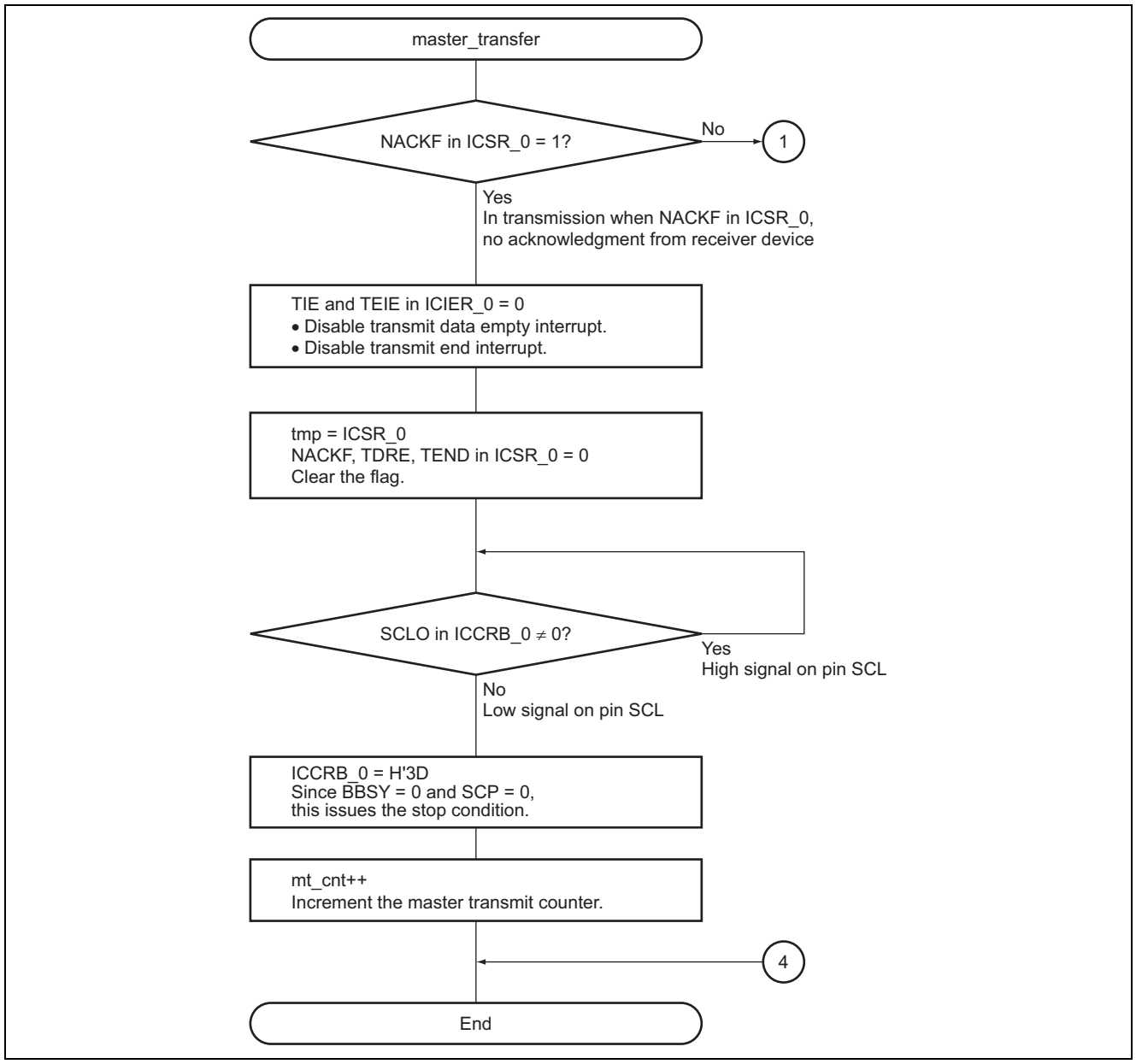
Bit	Bit Name	Setting	R/W	Description
7	TDRE	0	R/W	Transmit Data Register Empty [Setting conditions] • Transferring of data from ICDRT to ICDRS and having ICDRT empty • Setting of TRS • Issuing of a start condition (including retransmission) • Transition from the receive mode to the transmit mode has been made in the slave mode [Clearing conditions] • Writing of 0 in TDRE after reading it as 1 • Writing of data in ICDRT
6	TEND	0	R/W	Transmit End [Setting condition] • Rising of the ninth clock of SCL while the TDRE flag is 1 [Clearing conditions] • Writing 0 in TEND after reading TDRE as 1 • Writing of data in ICDRT

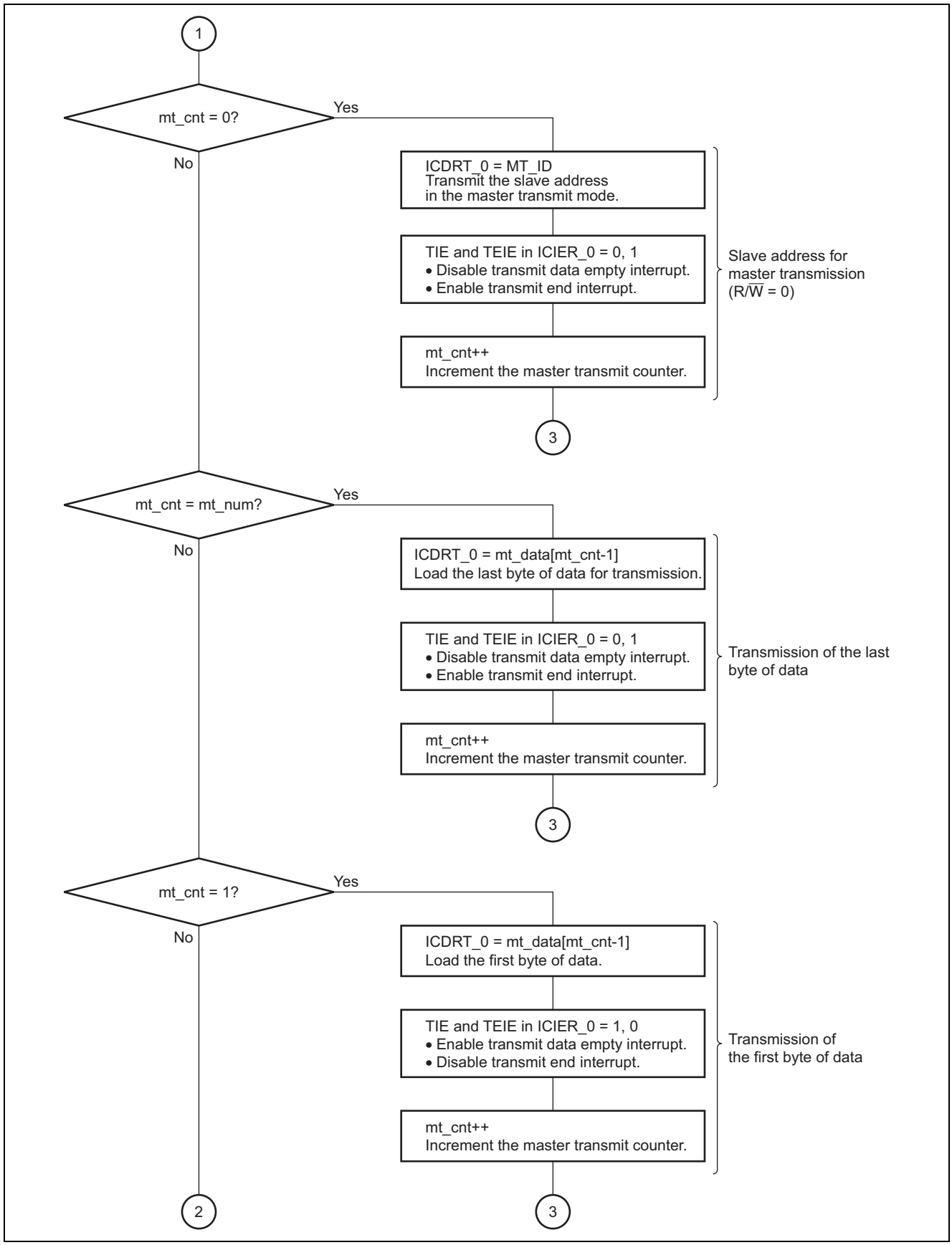
- I²C bus transmit data register_0 (ICDRT_0) Number of bits: 8 Address: H'FFFEB6

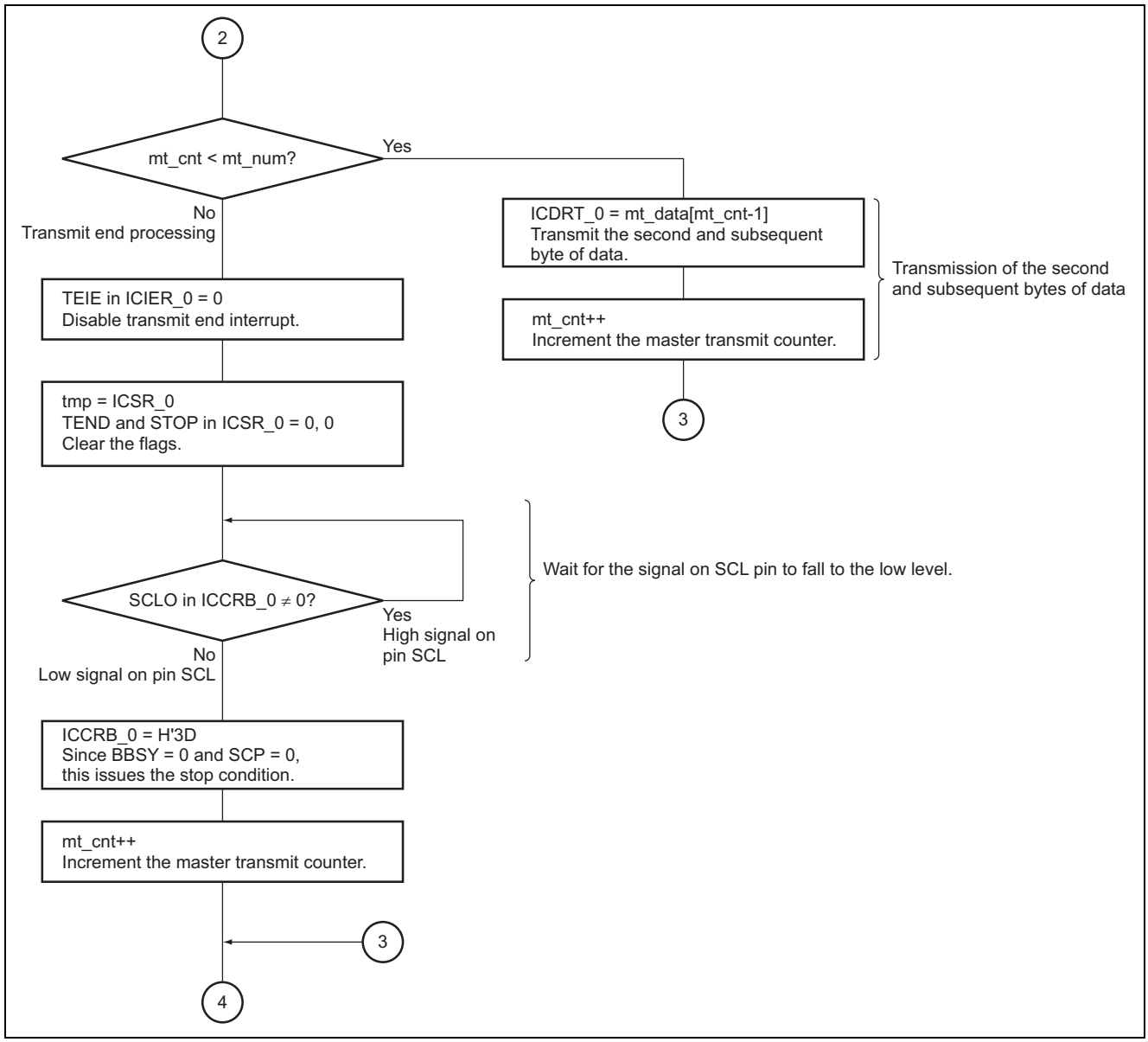
Function: ICDRT is an 8-bit readable/writable register that stores the transmit data. When ICDRT detects the space in the I²C bus shift register (ICDRS), it transfers the transmit data which is written in ICDRT to ICDRS and starts transferring data. When the next transfer data is written to ICDRT during transferring data of ICDRS, continuous transfer is possible. The initial value of ICDRT is H'FF.

Setting: S_Send[st_cnt]

5. Flowchart


master_transfer
NACKF in ICSR_0 = 1?
No
1
Yes
In transmission when NACKF in ICSR_0,
no acknowledgment from receiver device
TIE and TEIE in ICIER_0 = 0
• Disable transmit data empty interrupt.
• Disable transmit end interrupt.
tmp = ICSR_0
NACKF, TDRE, TEND in ICSR_0 = 0
Clear the flag.
SCLO in ICCRB_0 ≠ 0?
Yes
High signal on pin SCL
No
Low signal on pin SCL
ICCRB_0 = H'3D
Since BBSY = 0 and SCP = 0,
this issues the stop condition.
mt_cnt++
Increment the master transmit counter.
4
End


1
mt_cnt = 0?
Yes
No
ICDRT_0 = MT_ID
Transmit the slave address
in the master transmit mode.
TIE and TEIE in ICIER_0 = 0, 1
• Disable transmit data empty interrupt.
• Enable transmit end interrupt.
mt_cnt++
Increment the master transmit counter.
Slave address for
master transmission
(R/W = 0)
3
mt_cnt = mt_num?
Yes
No
ICDRT_0 = mt_data[mt_cnt-1]
Load the last byte of data for transmission.
TIE and TEIE in ICIER_0 = 0, 1
• Disable transmit data empty interrupt.
• Enable transmit end interrupt.
mt_cnt++
Increment the master transmit counter.
Transmission of the last
byte of data
3
mt_cnt = 1?
Yes
No
ICDRT_0 = mt_data[mt_cnt-1]
Load the first byte of data.
TIE and TEIE in ICIER_0 = 1, 0
• Enable transmit data empty interrupt.
• Disable transmit end interrupt.
mt_cnt++
Increment the master transmit counter.
Transmission of
the first byte of data
2
3


2
mt_cnt < mt_num?
Yes
No
Transmit end processing
ICDRT_0 = mt_data[mt_cnt-1]
Transmit the second and subsequent byte of data.
mt_cnt++
Increment the master transmit counter.
Transmission of the second and subsequent bytes of data
3
TEIE in ICIER_0 = 0
Disable transmit end interrupt.
tmp = ICSR_0
TEND and STOP in ICSR_0 = 0, 0
Clear the flags.
SCLO in ICCRB_0 ≠ 0?
Yes
High signal on pin SCL
Wait for the signal on SCL pin to fall to the low level.
No
Low signal on pin SCL
ICCRB_0 = H'3D
Since BBSY = 0 and SCP = 0, this issues the stop condition.
mt_cnt++
Increment the master transmit counter.
3
4

5.7.8 master_receive Function

1. Functional overview
   Master-reception processing which is called by the I²C bus interface interrupt handler. In this case, the interrupt source will be the receive data full interrupt for each byte of received data.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
6	RCVD	0	R/W	Reception Disable Enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables the next reception. 1: Disables the next reception.
4	TRS	Undefined	R/W	Master/Slave Select 0: Receive mode 1: Transmit mode

- I²C bus control register B_0 (ICCRB_0) Number of bits: 8 Address: H'FFFEB1

Bit	Bit Name	Setting	R/W	Description
7	BBSY	1	R/W	Bus Busy The BBSY flag can be read to check whether the I²C bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions. A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0. To issue a start condition, use a MOV instruction to write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, use a MOV instruction to write 0 in BBSY and 0 in SCP.
6	SCP	0	R/W	Start Condition/Stop Condition Prohibit Bit Controls the issuing of start and stop conditions in master mode. Writing 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Writing 0 in BBSY and SCP issues a stop condition. This bit is always read as 1. Writing of 1 has no effect.
3	SCLO	1	R/W	Monitors level of signal output from SCL. When the SCLO bit is set to 1 in reading, the signal output from SCL is at high level. When the SCLO bit is set to 0 in reading, the signal output from SCL is at low level.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).
6	TEIE	0	R/W	Transmit End Interrupt Enable Enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Disables the transmit end interrupt request (TEI). 1: Enables the transmit end interrupt request (TEI).
5	RIE	1	R/W	Receive Interrupt Enable Enables or disables the receive data full interrupt request (RXI) when a received data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Disables the receive data full interrupt request (RXI). 1: Enables the receive data full interrupt request (RXI).
0	ACKBT	0	R/W	Transmit Acknowledge Specifies the bit to be sent at the acknowledge timing in receive mode. 0: 0 is output at acknowledge timing. 1: 1 is output at acknowledge timing.

- I²C bus status register_0 (ICSR_0) Number of bits: 8 Address: H'FFFEB4

Bit	Bit Name	Setting	R/W	Description
6	TEND	0	R/W	Transmit End [Setting condition] • Rising of the ninth clock of SCL while the TDRE flag is 1 [Clearing conditions] • Writing of 0 in TEND after reading it as 1 • Writing of data in ICDRT
4	NACKF	0	R/W	No Acknowledge Detection Flag [Setting condition] • Detection of no acknowledge from the receive device in transmission while the ACKE bit in ICIER is 1 [Clearing condition] • Writing of 0 in NACKF after reading it as 1

- I²C bus transmit data register_0 (ICDRT_0) Number of bits: 8 Address: H'FFFEB6

Function: ICDRT is an 8-bit readable/writable register that stores the transmit data. When ICDRT detects the space in the I²C bus shift register (ICDRS), it transfers the transmit data which is written in ICDRT to ICDRS and starts transferring data. When the next transfer data is written to ICDRT during transferring data of ICDRS, continuous transfer is possible. The initial value of ICDRT is H'FF.

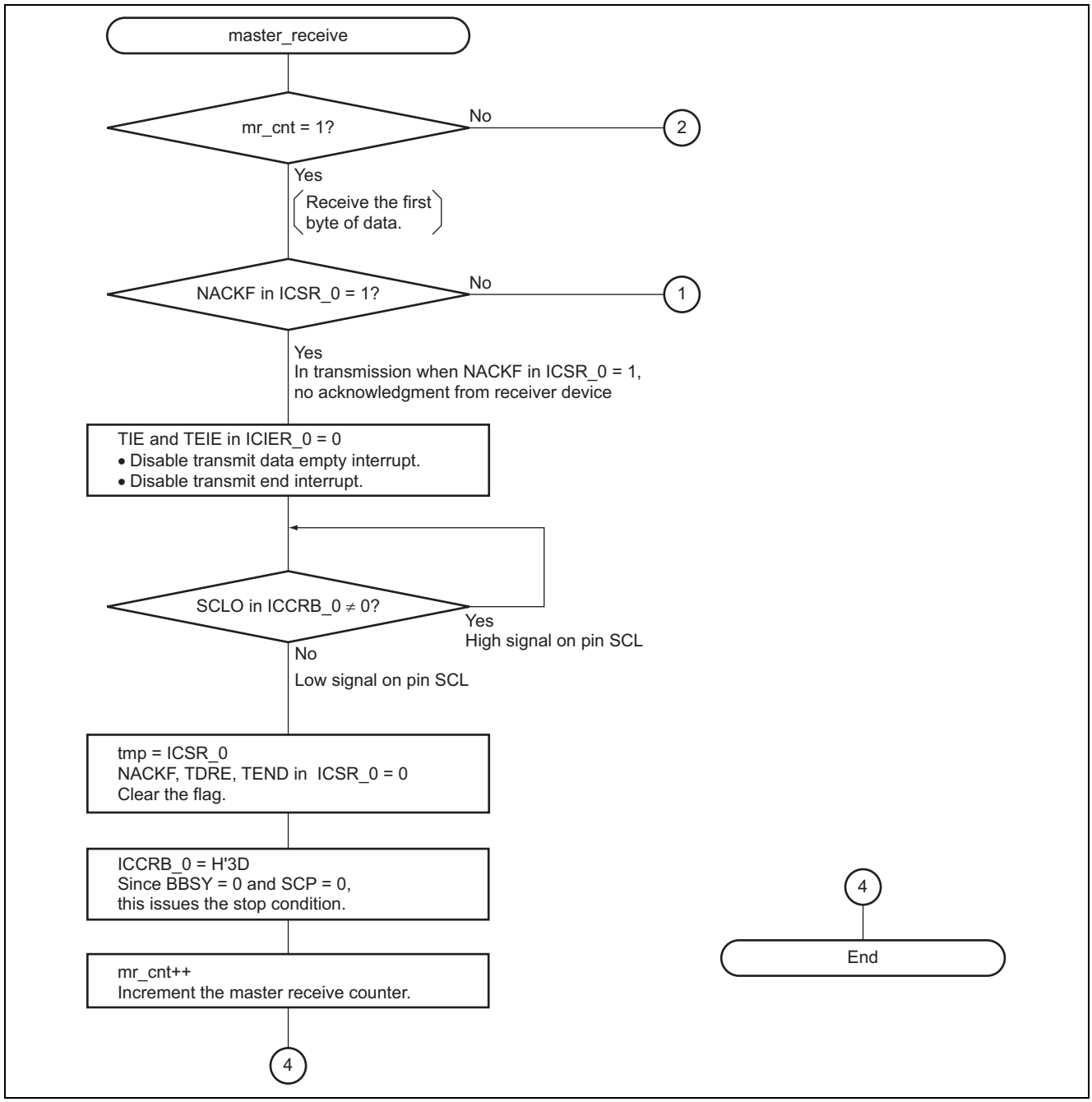
Setting: S_Send[st_cnt]

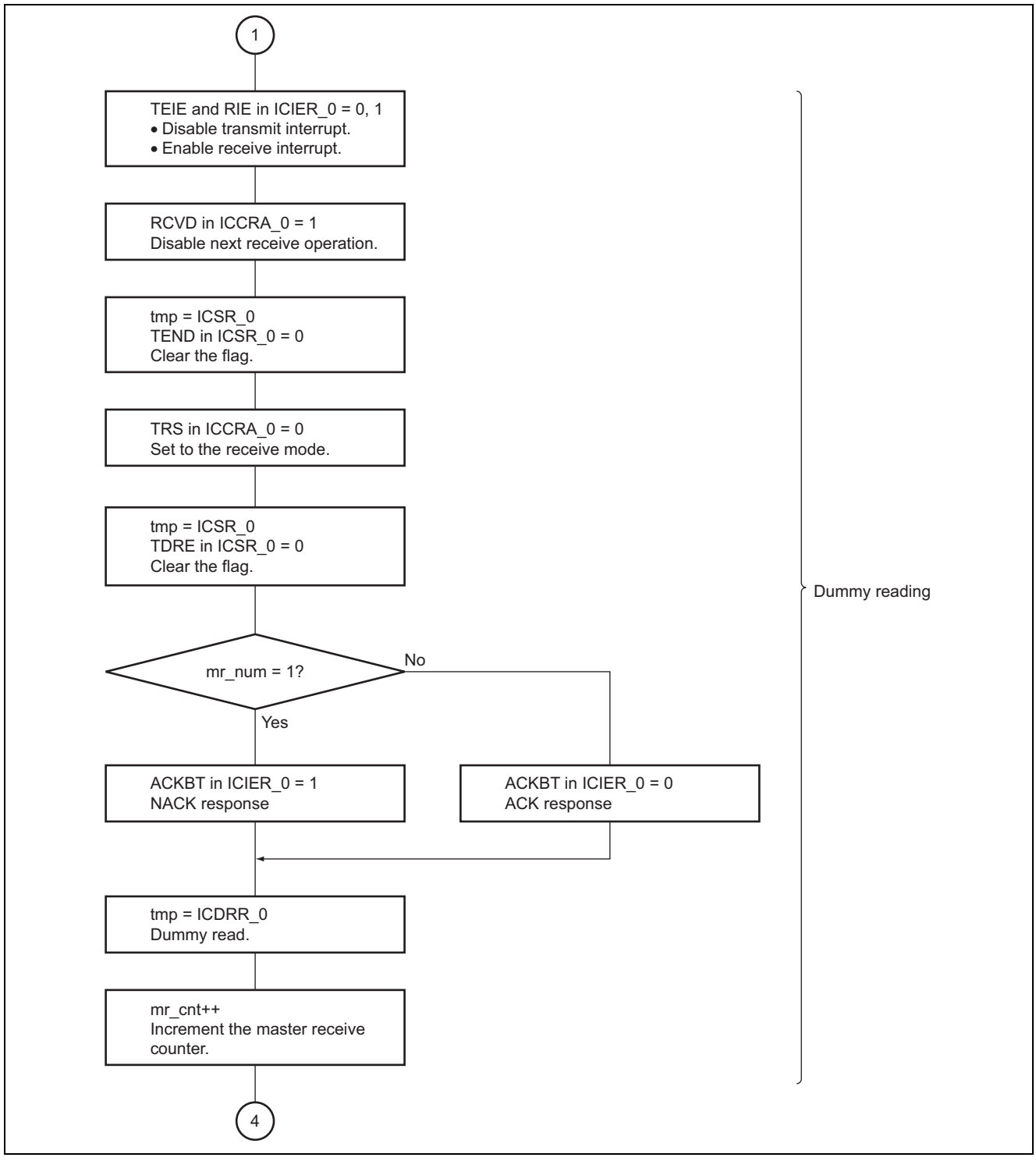
- I²C bus receive data register_0 (ICDRR_0) Number of bits: 8 Address: H'FFFEB7

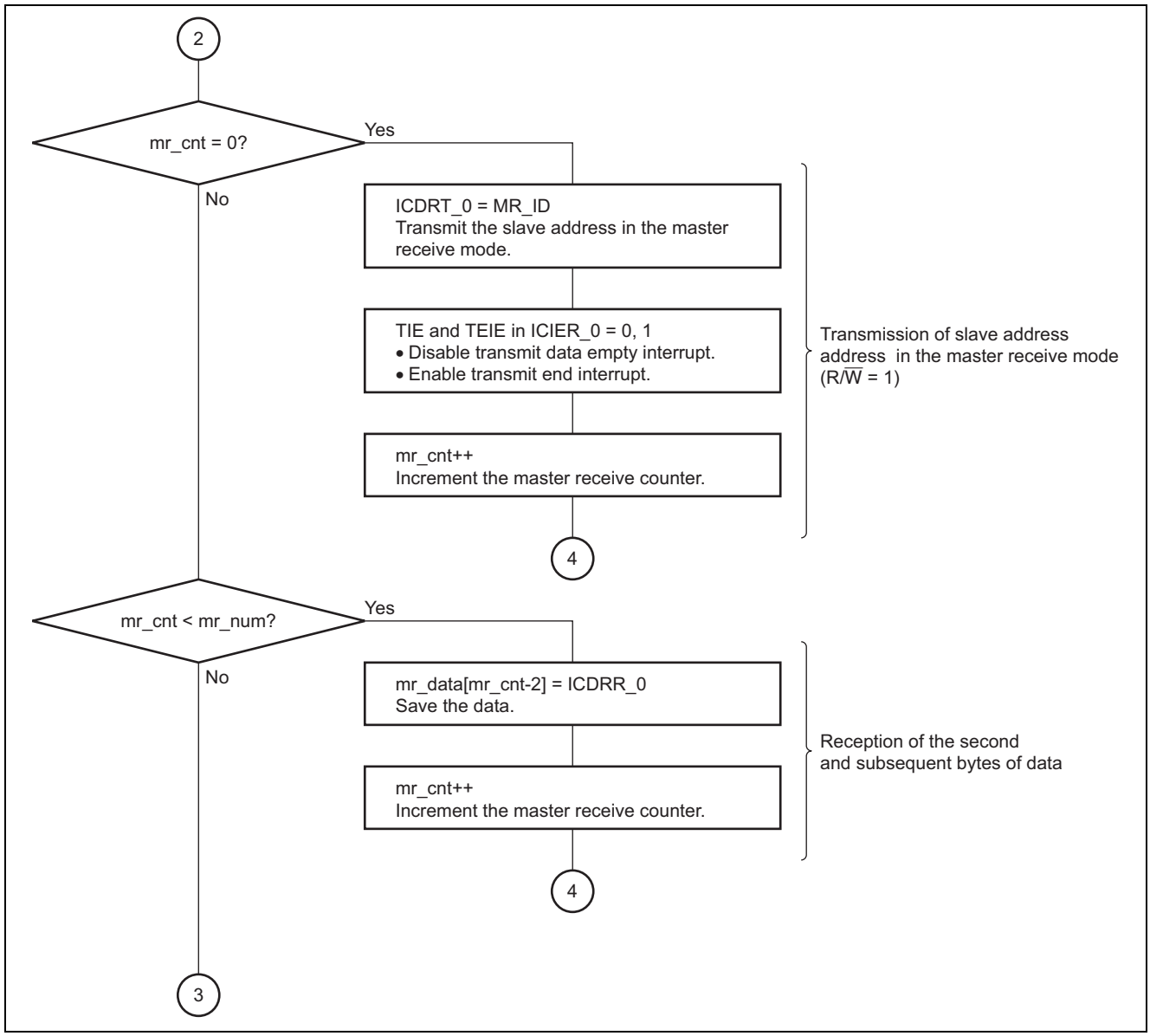
Function: ICDRR is an 8-bit register that stores the receive data. When data of one byte is received, ICDRR transfers the received data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, therefore the CPU cannot be written to this register. The initial value of ICDRR is H'FF.

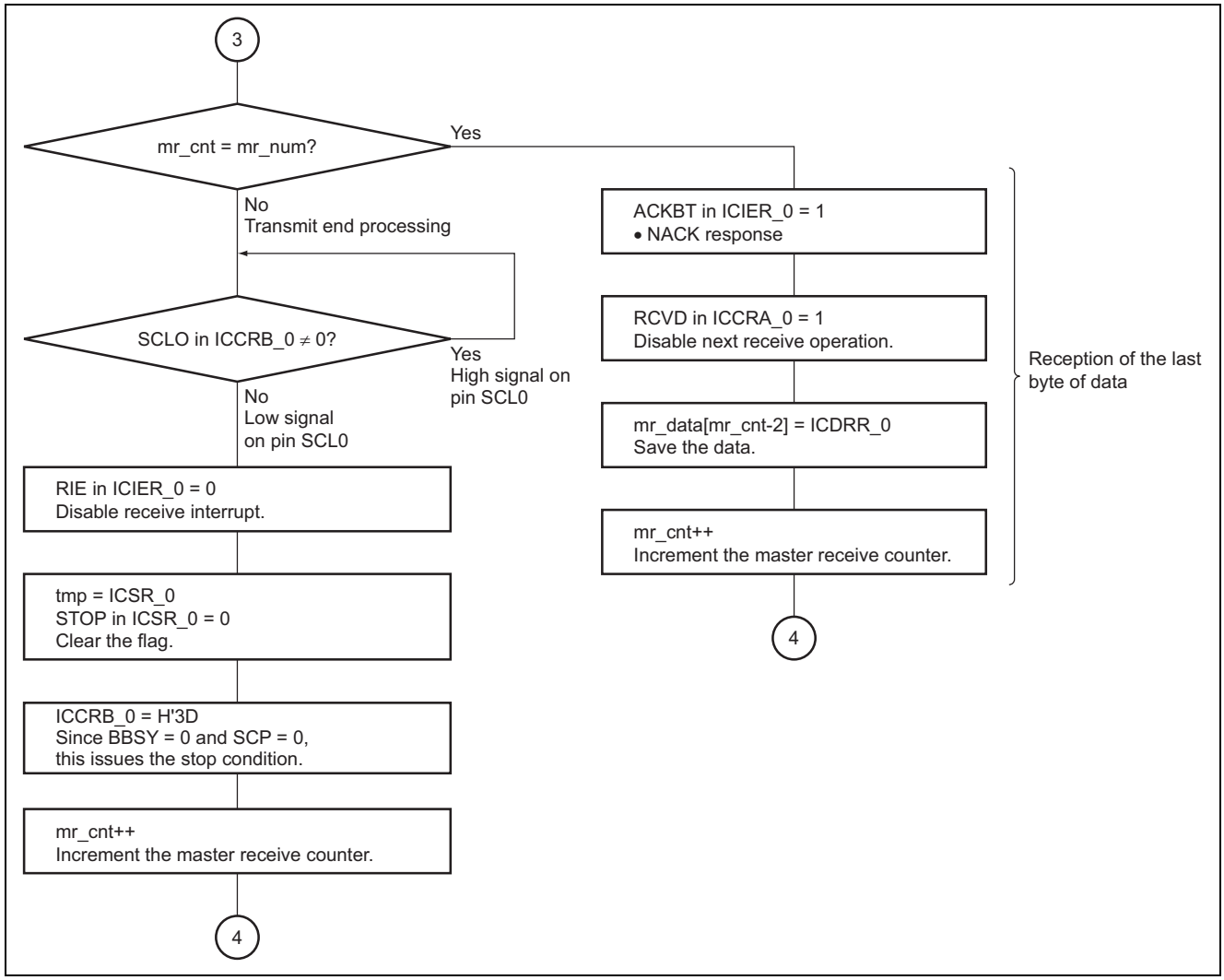
Setting: Undefined

5. Flowchart


master_receive
mr_cnt = 1?
No
2
Yes
Receive the first byte of data.
NACKF in ICSR_0 = 1?
No
1
Yes
In transmission when NACKF in ICSR_0 = 1, no acknowledgment from receiver device
TIE and TEIE in ICIER_0 = 0
• Disable transmit data empty interrupt.
• Disable transmit end interrupt.
SCLO in ICCRB_0 ≠ 0?
Yes
High signal on pin SCL
No
Low signal on pin SCL
tmp = ICSR_0
NACKF, TDRE, TEND in ICSR_0 = 0
Clear the flag.
ICCRB_0 = H'3D
Since BBSY = 0 and SCP = 0, this issues the stop condition.
mr_cnt++
Increment the master receive counter.
4
4
End


1
TEIE and RIE in ICIER_0 = 0, 1
• Disable transmit interrupt.
• Enable receive interrupt.
RCVD in ICCRA_0 = 1
Disable next receive operation.
tmp = ICSR_0
TEND in ICSR_0 = 0
Clear the flag.
TRS in ICCRA_0 = 0
Set to the receive mode.
tmp = ICSR_0
TDRE in ICSR_0 = 0
Clear the flag.
mr_num = 1?
No
Yes
ACKBT in ICIER_0 = 1
NACK response
ACKBT in ICIER_0 = 0
ACK response
tmp = ICDRR_0
Dummy read.
mr_cnt++
Increment the master receive counter.
4
Dummy reading


2
mr_cnt = 0?
Yes
No
ICDRT_0 = MR_ID
Transmit the slave address in the master receive mode.
TIE and TEIE in ICIER_0 = 0, 1
• Disable transmit data empty interrupt.
• Enable transmit end interrupt.
mr_cnt++
Increment the master receive counter.
Transmission of slave address address in the master receive mode (R/W = 1)
4
mr_cnt < mr_num?
Yes
No
mr_data[mr_cnt-2] = ICDRR_0
Save the data.
mr_cnt++
Increment the master receive counter.
Reception of the second and subsequent bytes of data
4
3


3
mr_cnt = mr_num?
Yes
No
Transmit end processing
SCLO in ICCRB_0 ≠ 0?
Yes
High signal on
pin SCL0
No
Low signal
on pin SCL0
RIE in ICIER_0 = 0
Disable receive interrupt.
tmp = ICSR_0
STOP in ICSR_0 = 0
Clear the flag.
ICCRB_0 = H'3D
Since BBSY = 0 and SCP = 0,
this issues the stop condition.
mr_cnt++
Increment the master receive counter.
4
ACKBT in ICIER_0 = 1
• NACK response
RCVD in ICCRA_0 = 1
Disable next receive operation.
mr_data[mr_cnt-2] = ICDRR_0
Save the data.
mr_cnt++
Increment the master receive counter.
4
Reception of the last
byte of data

5.7.9 master_randomread Function

1. Functional overview
   Master-reception process which is called by the I²C bus interface interrupt handler. In this case, the interrupt source will be the receive data full interrupt for each byte of received data.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- I²C bus control register A_0 (ICCRA_0) Number of bits: 8 Address: H'FFFEB0

Bit	Bit Name	Setting	R/W	Description
6	RCVD	0	R/W	Reception Disable Enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables the next reception. 1: Disables the next reception.
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	10: Master receive mode 11: Master transmit mode

- I²C bus control register B_0 (ICCRB_0) Number of bits: 8 Address: H'FFFEB1

Bit	Bit Name	Setting	R/W	Description
7	BBSY	0/1	R/W	Bus Busy The BBSY flag can be read to check whether the I²C bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions. A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0. To issue a start condition, use a MOV instruction to write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, use a MOV instruction to write 0 in BBSY and 0 in SCP.
6	SCP	0	R/W	Start Condition/Stop Condition Prohibit Bit Controls the issuing of start and stop conditions in master mode. Writing 1 in BBSY and 0 in SCP issues a start condition. A retransmit start condition is issued in the same way. Writing 0 in BBSY and SCP issues a stop condition. This bit is always read as 1. Writing of 1 has no effect.
3	SCLO	Undifined	R/W	Monitors level of signal output from SCL. When the SCLO bit is set to 1 in reading, the signal output from SCL is at high level. When the SCLO bit is set to 0 in reading, the signal output from SCL is at low level.

- I²C bus interrupt enable register_0 (ICIER_0) Number of bits: 8 Address: H'FFFEB3

Bit	Bit Name	Setting	R/W	Description
7	TIE	1	R/W	Transmit Interrupt Enable Enables or disables the transmit data empty interrupt (TXI) when the TDRE bit in ICSR is set to 1 0: Disables the transmit data empty interrupt request (TXI). 1: Enables the transmit data empty interrupt request (TXI).
6	TEIE	0	R/W	Transmit End Interrupt Enable Enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Disables the transmit end interrupt request (TEI). 1: Enables the transmit end interrupt request (TEI).
5	RIE	1	R/W	Receive Interrupt Enable Enables or disables the receive data full interrupt request (RXI) when a received data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Disables the receive data full interrupt request (RXI). 1: Enables the receive data full interrupt request (RXI).
0	ACKBT	0	R/W	Transmit Acknowledge Specifies the bit to be sent at the acknowledge timing in receive mode. 0: 0 is output at acknowledge timing. 1: 1 is output at acknowledge timing.

- I²C bus status register_0 (ICSR_0) Number of bits: 8 Address: H'FFFEB4

Bit	Bit Name	Setting	R/W	Description
7	TDRE	0	R/W	Transmit Data Register Empty [Setting conditions] • Transferring of data from ICDRT to ICDRS and having ICDRT empty • Setting of TRS • Issuing of a start condition (including retransmission) • Transition from the receive mode to the transmit mode has been made in the slave mode [Clearing conditions] • Writing of 0 in TDRE after reading TDRE as 1 • Writing of data in ICDRT
6	TEND	0	R/W	Transmit End [Setting condition] • Rising of the ninth clock of SCL while the TDRE flag is 1 [Clearing conditions] • Writing 0 in TEND after reading it as 1 • Writing of data in ICDRT
4	NACKF	0	R/W	No Acknowledge Detection Flag [Setting condition] • Detection of no acknowledge from the receive device in transmission while the ACKE bit in ICIER is 1 [Clearing condition] • Writing of 0 in NACKF after reading it as 1

- I²C bus transmit data register_0 (ICDRT_0) Number of bits: 8 Address: H'FFFEB6

Function: ICDRT is an 8-bit readable/writable register that stores the transmit data. When ICDRT detects the space in the I²C bus shift register (ICDRS), it transfers the transmit data which is written in ICDRT to ICDRS and starts transferring data. When the next transfer data is written to ICDRT during transferring data of ICDRS, continuous transfer is possible. The initial value of ICDRT is H'FF.

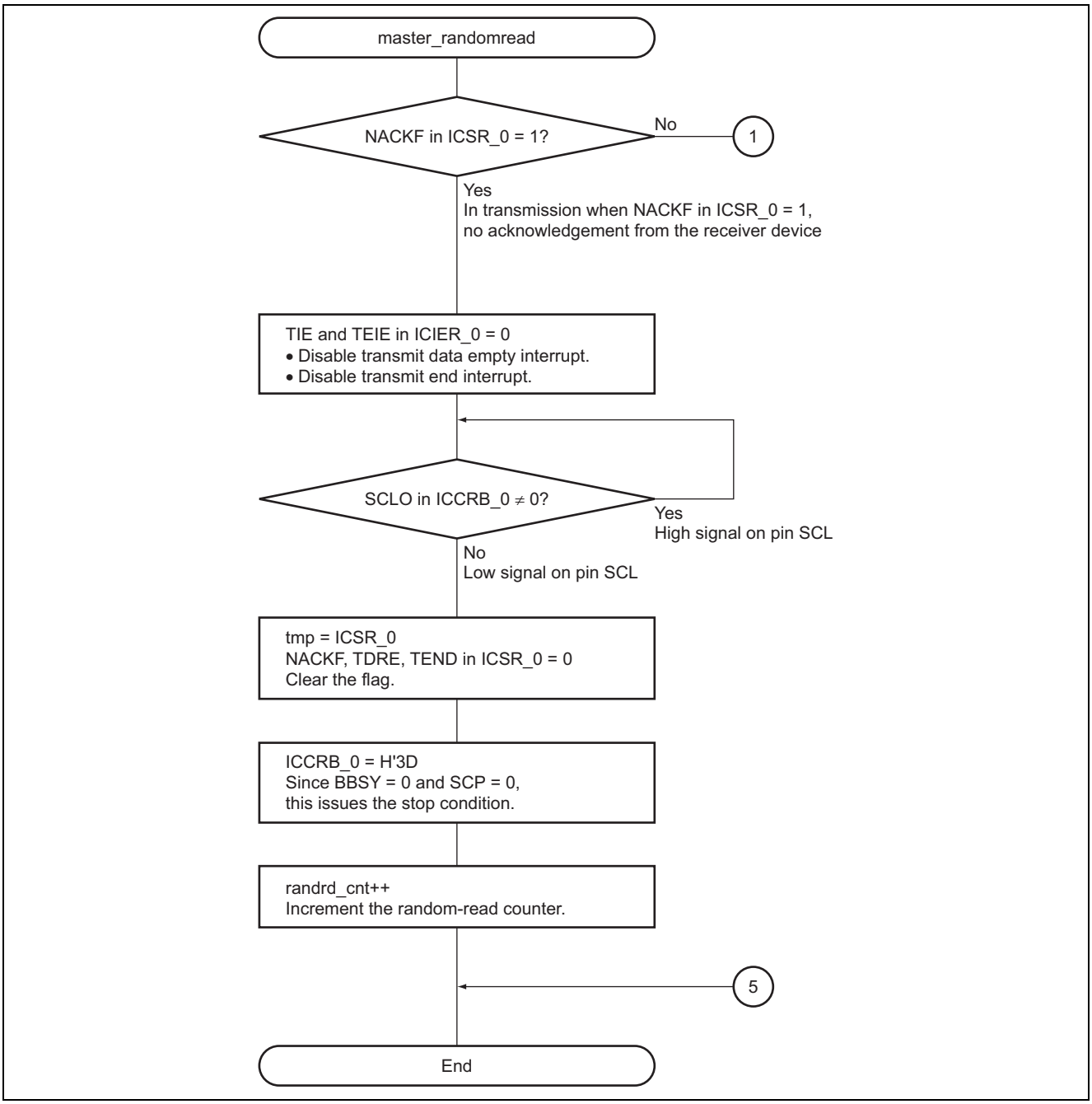
Setting: MT_ID, MR_ID, mt_data[0]

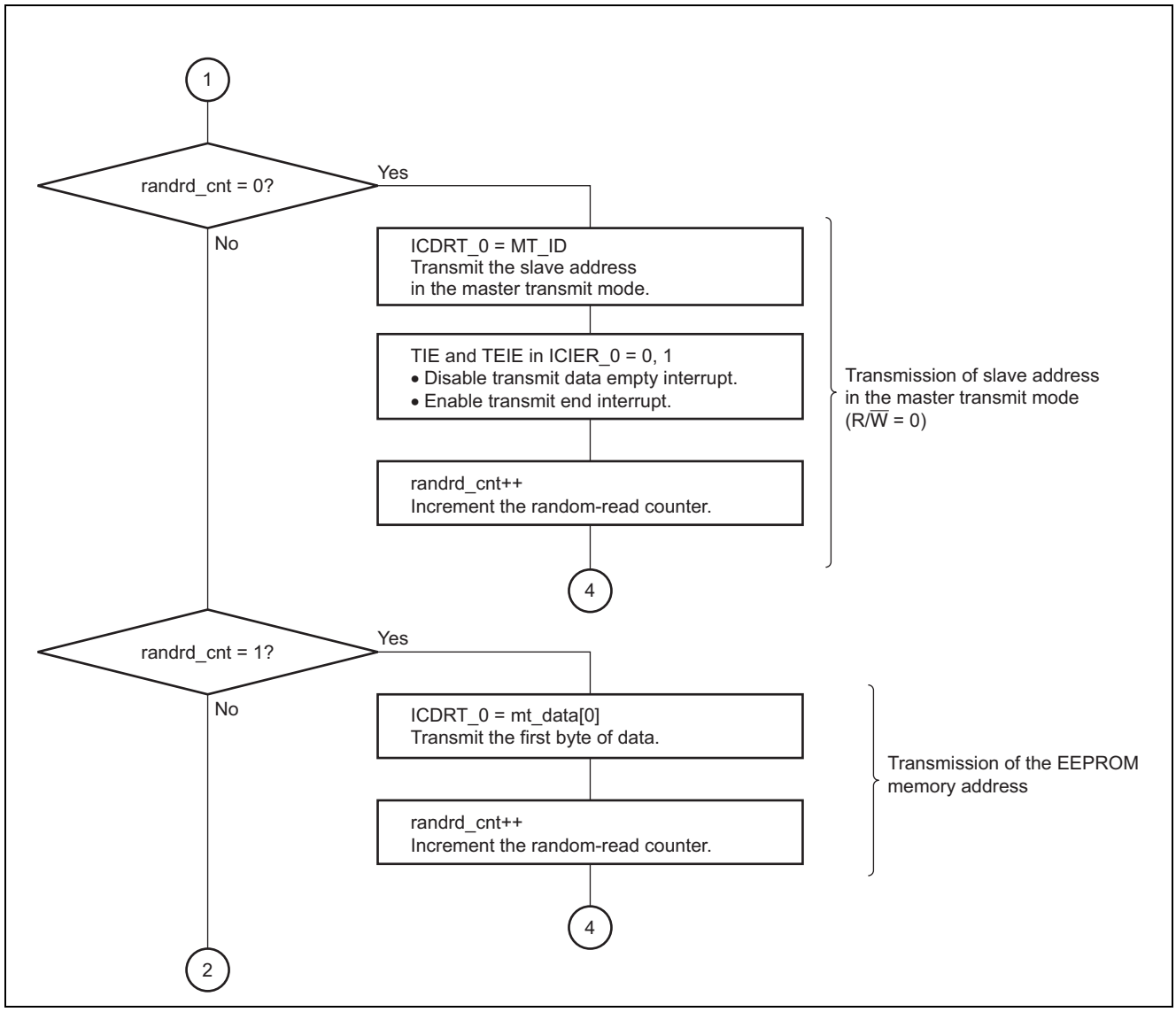
- I²C bus receive data register_0 (ICDRR_0) Number of bits: 8 Address: H'FFFEB7

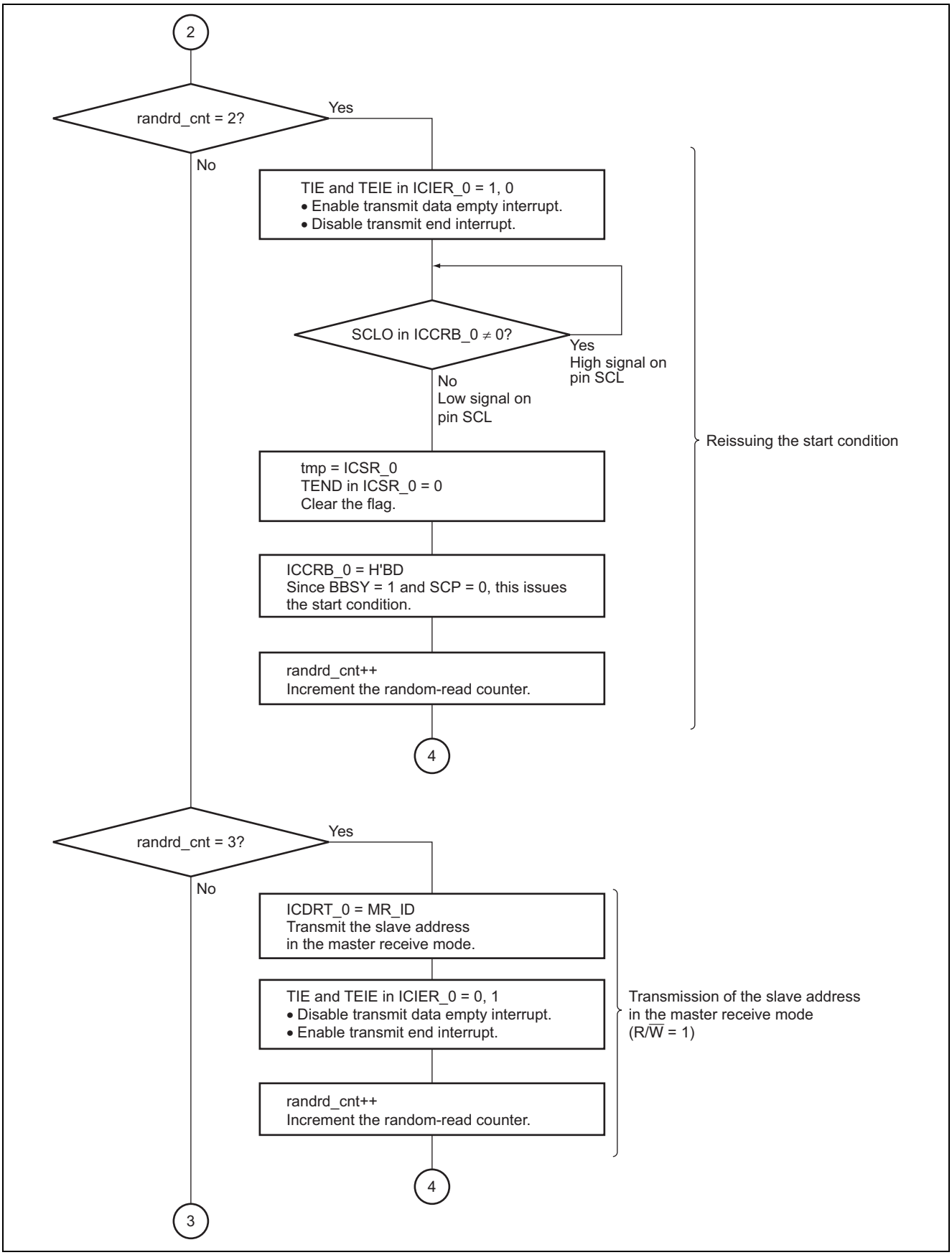
Function: ICDRR is an 8-bit register that stores the receive data. When data of one byte is received, ICDRR transfers the received data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, therefore the CPU cannot be written to this register. The initial value of ICDRR is H'FF.

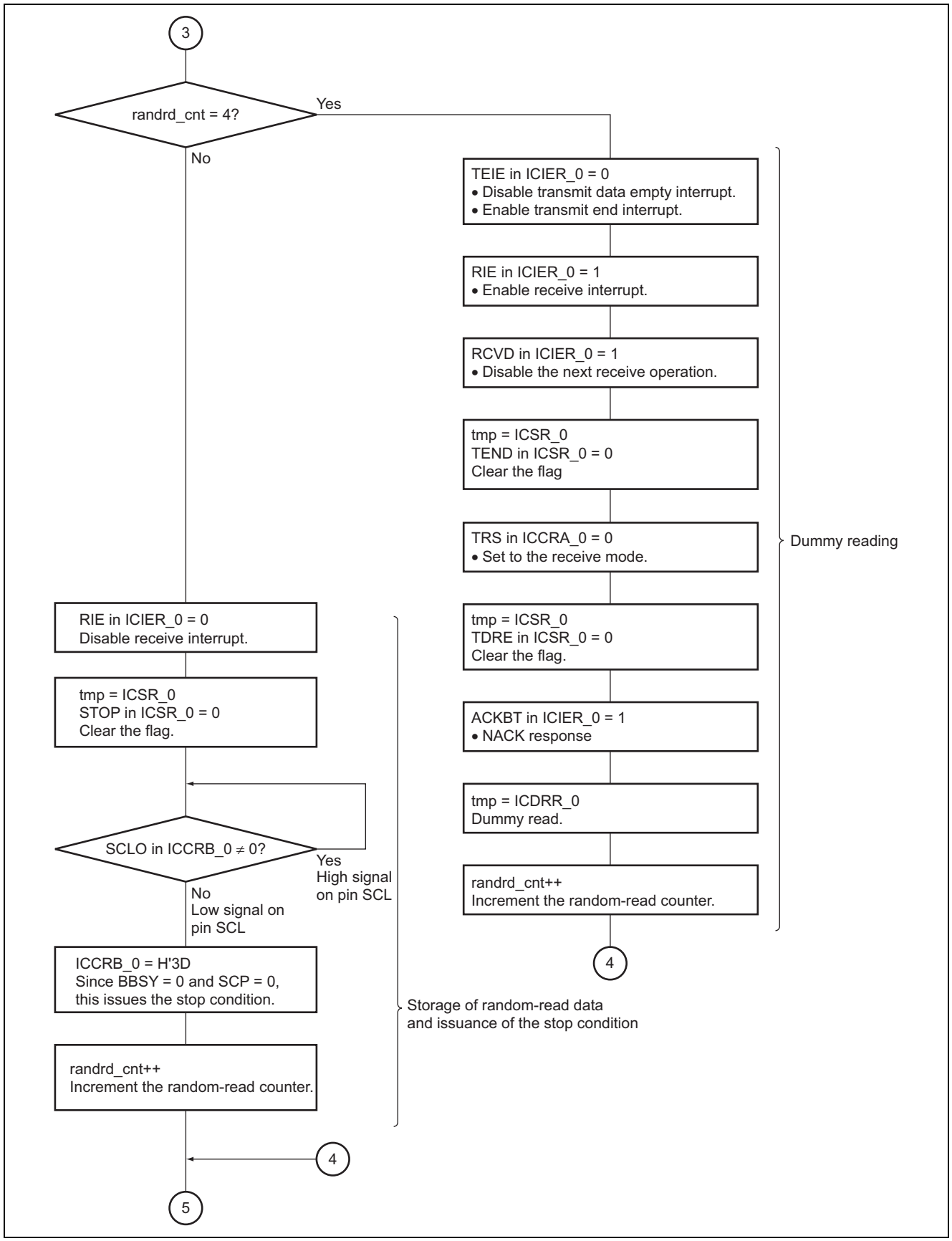
Setting: Undefined

5. Flowchart


master_randomread
NACKF in ICSR_0 = 1?
No
1
Yes
In transmission when NACKF in ICSR_0 = 1,
no acknowledgement from the receiver device
TIE and TEIE in ICIER_0 = 0
• Disable transmit data empty interrupt.
• Disable transmit end interrupt.
SCLO in ICCRB_0 ≠ 0?
Yes
High signal on pin SCL
No
Low signal on pin SCL
tmp = ICSR_0
NACKF, TDRE, TEND in ICSR_0 = 0
Clear the flag.
ICCRB_0 = H'3D
Since BBSY = 0 and SCP = 0,
this issues the stop condition.
randrd_cnt++
Increment the random-read counter.
5
End


1
randrd_cnt = 0?
Yes
No
ICDRT_0 = MT_ID
Transmit the slave address
in the master transmit mode.
TIE and TEIE in ICIER_0 = 0, 1
• Disable transmit data empty interrupt.
• Enable transmit end interrupt.
randrd_cnt++
Increment the random-read counter.
Transmission of slave address
in the master transmit mode
(R/W = 0)
4
randrd_cnt = 1?
Yes
No
ICDRT_0 = mt_data[0]
Transmit the first byte of data.
randrd_cnt++
Increment the random-read counter.
Transmission of the EEPROM
memory address
4
2


2
randrd_cnt = 2?
Yes
No
TIE and TEIE in ICIER_0 = 1, 0
• Enable transmit data empty interrupt.
• Disable transmit end interrupt.
SCLO in ICCRB_0 ≠ 0?
Yes
High signal on pin SCL
No
Low signal on pin SCL
tmp = ICSR_0
TEND in ICSR_0 = 0
Clear the flag.
ICCRB_0 = H'BD
Since BBSY = 1 and SCP = 0, this issues the start condition.
randrd_cnt++
Increment the random-read counter.
4
Reissuing the start condition
randrd_cnt = 3?
Yes
No
ICDRT_0 = MR_ID
Transmit the slave address in the master receive mode.
TIE and TEIE in ICIER_0 = 0, 1
• Disable transmit data empty interrupt.
• Enable transmit end interrupt.
randrd_cnt++
Increment the random-read counter.
4
Transmission of the slave address in the master receive mode (R/W = 1)
3


3
randrd_cnt = 4?
Yes
No
TEIE in ICIER_0 = 0
• Disable transmit data empty interrupt.
• Enable transmit end interrupt.
RIE in ICIER_0 = 1
• Enable receive interrupt.
RCVD in ICIER_0 = 1
• Disable the next receive operation.
tmp = ICSR_0
TEND in ICSR_0 = 0
Clear the flag
TRS in ICCRA_0 = 0
• Set to the receive mode.
Dummy reading
RIE in ICIER_0 = 0
Disable receive interrupt.
tmp = ICSR_0
TDRE in ICSR_0 = 0
Clear the flag.
tmp = ICSR_0
STOP in ICSR_0 = 0
Clear the flag.
ACKBT in ICIER_0 = 1
• NACK response
tmp = ICDRR_0
Dummy read.
SCLO in ICCRB_0 ≠ 0?
Yes
High signal
on pin SCL
randrd_cnt++
Increment the random-read counter.
4
No
Low signal on
pin SCL
ICCRB_0 = H'3D
Since BBSY = 0 and SCP = 0,
this issues the stop condition.
Storage of random-read data
and issuance of the stop condition
randrd_cnt++
Increment the random-read counter.
4
5

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http://www.renesas.com/

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.25.07	—	First edition issued

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