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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

Signed 32-Bit Binary Division with a 16-Bit Divisor (DIVXS)

Introduction

Performs division in this format.
dividend (signed, 32 bits) / divisor (signed, 16 bits) = quotient (signed, 32 bits) … remainder (signed, 16 bits).

Target Device

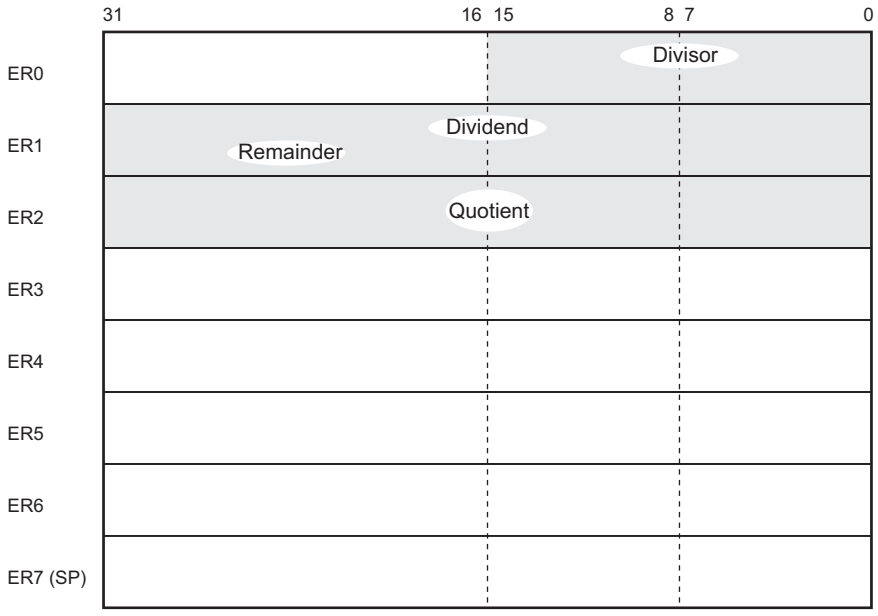
H8/300H Tiny Series

Contents

1. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Dividend (signed, 32 bits)	ER1	4
	Divisor (signed, 16 bits)	R0	2
Output	Quotient (signed, 32 bits)	ER2	4
	Remainder (signed, 16 bits)	E1	2
	Occurrence of error	Z flag (CCR)	—

2. Changes to Internal Registers and Flags



I	U	H	UI	N	Z	V	C
–	–	–	–	↕	↕	0	–

–: No change
↕: Varies
0: Fixed to 0
1: Fixed to 1

3. Programming Specifications

Program memory (bytes)
26
Data memory (bytes)
0
Stack (bytes)
0
Number of cycles
76
Re-entrant
Yes
Relocatable
Yes
Interrupts during execution
Yes

4. Note

The number of cycles in the programming specifications is the value for calculation of H'8FFFFFFF / H'7FFF.

5. Description

5.1 Description of Functions

1. The arguments are as follows.
   R0: Set the divisor (signed 16 bits) as an input argument.
   ER1: Set the dividend (signed 32 bits) as an input argument.
   ER2: The quotient (signed 32 bits) is also set here as an output argument.
   E1: The remainder (signed 16 bits) is also set here as an output argument.
   Z flag (CCR): Indicates an error (division by 0) in the execution of DIVXS.
      Z flag = 1: The division was in error.
      Z flag = 0: The division was processed without error.

2. The following figure illustrates the execution of the DIVXS subroutine. When the input arguments are set as shown below, DIVXS places the quotient in ER2 and the remainder in E1.

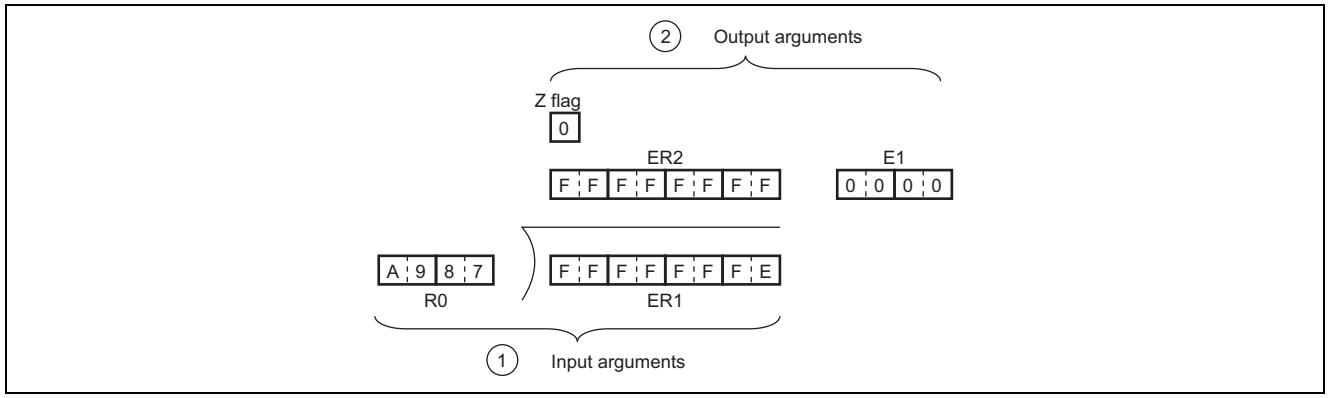


Figure 1 Example of DIVXS Execution

3. The DIVXS subroutine starts by determining whether the divisor is 0 or nonzero; if it is 0, DIVXS ends.

5.2 Usage Notes

Since the remainder is set in E1 and the lower 16 bits of the quotient are set in R1, the dividend is lost through execution of DIVXS. When you will still require the dividend, save it elsewhere in memory beforehand.

5.3 Description of Data Memory

No data memory is used by DIVXS.

5.4 Example of Usage

After setting the dividend and divisor as input arguments, call the DIVXS subroutine.

```
WORK1   . RES. L 1          ..... Reservation of the data memory area for setting of the dividend (signed, 32 bits) by the user program.
WORK2   . RES. W 1          ..... Reservation of the data memory area for setting of the divisor (signed, 16 bits) by the user program.
          .
          .
          .
        MOV. L @WORK1, ER1  ..... Sets, as an input argument the dividend specified by the user program.
        MOV. W @WORK2, R0   ..... Sets, as an input argument the divisor specified by the user program.
        JSR    @DIVXS       ..... Subroutine call of DIVXS.
        BEQ    ERROR        ..... When division by 0 is attempted, the program branches to the routine for processing this error.
ERROR   Processing routine for errors
```

5.5 Principles of Operation

1. Firstly, the program tests for a division-by-zero error. In the case of this error, the divisor is transferred to the register in which it is itself stored so that the resulting Z bit can be used to determine if the divisor is 0. If the Z bit is 1 (divisor = 0), DIVXS ends.
2. When 32 bits is being divided by 16 bits using the signed division instruction (DIVXS.W), a quotient of 16 bits is found. The quotient will thus overflow when division such as H'FFFFF / H'01 is performed. For that reason, a quotient of 32 bits is found using the following procedure.
   1) The upper 16 bits of the dividend are sent to R2 and sign-extended into 32 bits ((1) in the figure).
   2) The upper 16 bits of the dividend are divided to obtain the upper 16 bits of the quotient ((2) in the figure).
   3) The remainder found in step 2) above (remainder 1) is sent to R1 ((3) in the figure).
   4) Division is performed on the lower 16 bits of the dividend to find the lower 16 bits of the quotient and the remainder (remainder 2) ((4) in the figure).

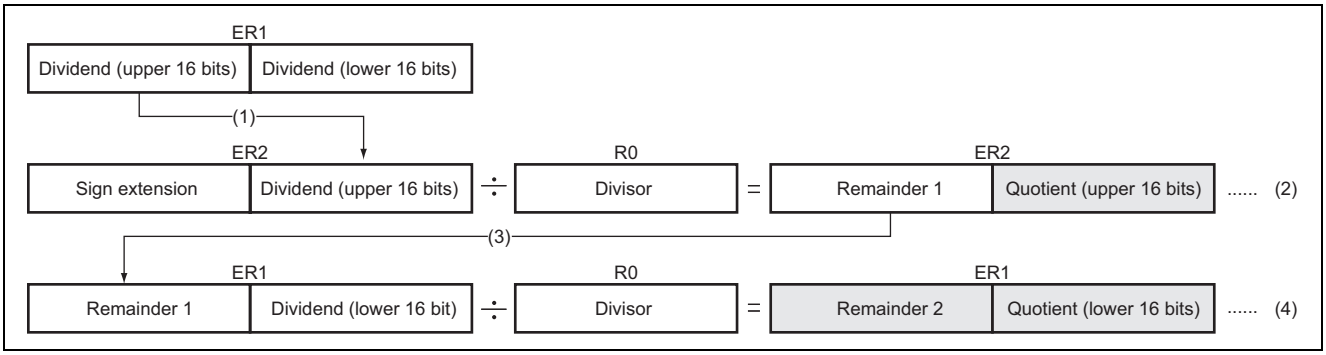
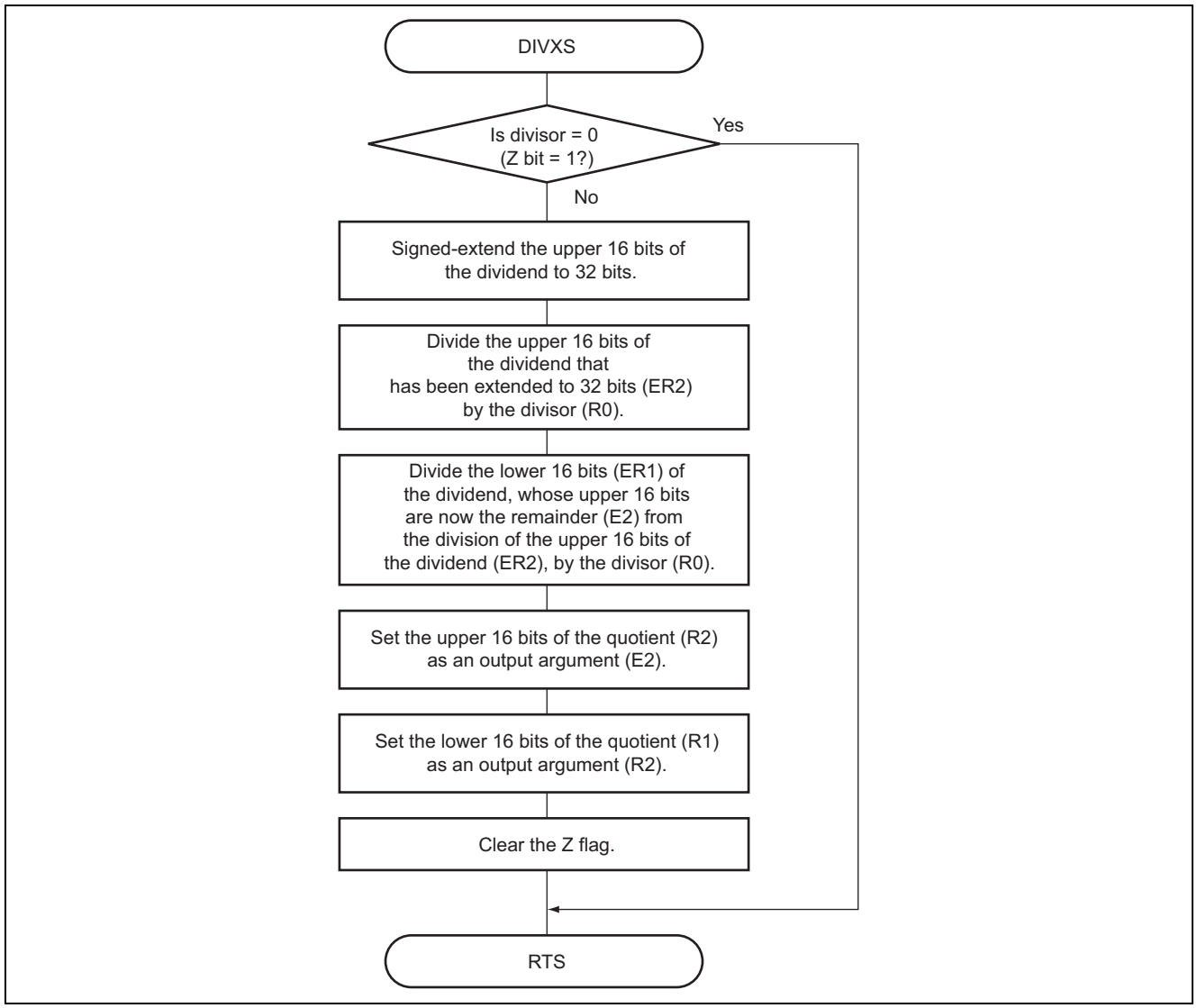


Figure 2 Overflow Processing

6. Flowchart


DIVXS
Is divisor = 0
(Z bit = 1?)
Yes
No
Signed-extend the upper 16 bits of
the dividend to 32 bits.
Divide the upper 16 bits of
the dividend that
has been extended to 32 bits (ER2)
by the divisor (R0).
Divide the lower 16 bits (ER1) of
the dividend, whose upper 16 bits
are now the remainder (E2) from
the division of the upper 16 bits of
the dividend (ER2), by the divisor (R0).
Set the upper 16 bits of the quotient (R2)
as an output argument (E2).
Set the lower 16 bits of the quotient (R1)
as an output argument (R2).
Clear the Z flag.
RTS

7. Program Listing

```
 1                                   1   ;*********************************************************************
 2                                   2   ;*                                                                   *
 3                                   3   ;*        NAME     :  32 BIT DIVISION   (DIVXS)                     *
 4                                   4   ;*                                                                   *
 5                                   5   ;*********************************************************************
 6                                   6   ;*                                                                   *
 7                                   7   ;*        ENTRY    :  ER1              (DIVIDEND)                   *
 8                                   8   ;*                     R0              (DIVISOR)                    *
 9                                   9   ;*        RETURNS  :  ER2              (QUOTIENT)                   *
10                                  10   ;*                     E1              (RESIDUAL)                   *
11                                  11   ;*                                                                   *
12                                  12   ;*********************************************************************
13                                  13   ;
14                                  14              .CPU        300HA
15    001000                        15              .SECTION A,CODE,LOCATE=H'001000
16            00001000              16   DIVXS      .EQU        $               ;Entry point
17    001000  0D00                  17              MOV.W       R0,R0           ;
18    001002  58700014              18              BEQ         DIVXS1          ;If divisor = 0 then return
19    001006  0D92                  19              MOV.W       E1,R2           ;Dividend(upper 16 bit) -> R2
20    001008  17F2                  20              EXTS.L      ER2             ;Dividend(upper 16 bit)
21    00100A  01D05302              21              DIVXS.W     R0,ER2          ;
22    00100E  0DA9                  22              MOV.W       E2,E1           ;Set residual to E1
23    001010  01D05301              23              DIVXS.W     R0,ER1          ;
24    001014  0D2A                  24              MOV.W       R2,E2           ;Set quotient (upper 16 bit) to E2
25    001016  0D12                  25              MOV.W       R1,R2           ;Set quotient (upper 16 bit) to R2
26    001018  06FB                  26              ANDC        #B'11111011,CCR ;
27    00101A  5470                  27   DIVXS1     RTS
28                                  28              .END
***** TOTAL   ERRORS    0
***** TOTAL   WARNINGS  0
```

Note: The program listing included in this application note assumes compilation under the option for the advanced mode of H8/300H CPU. If you use this sample program with an H8/300H Tiny Series product, make the following change to the program code:
.CPU 300HA → .CPU 300HN

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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