SH7670 Group

Example of Setting the CPG to Change the Operating Frequency

R01AN0298EJ0101
Rev. 1.01
Oct. 15, 2010

Summary

This application note describes an example of reconfiguration to change the operating frequency of the clock pulse generator (CPG) of an SH7670, SH7671, SH7672, or SH7673.

Target Device

SH7670 MCU

Contents

1. Introduction

1.1 Specifications

- In function main, software processing repeatedly inverts the output on a pin of port C.
- Settings made for the clock pulse generator (CPG) and operating frequency are changed by handling of the non-maskable interrupt (NMI). The rate of inversion of the pin changes with the change to the operating frequency.
- The watchdog timer (WDT) is used to secure the PLL settling time when the operating frequency is changed.

1.2 Module Used

- Clock pulse generator (CPG)
- Watchdog timer (WDT)
- NMI interrupt

1.3 Applicable Conditions

MCU	SH7670
Operating Frequency	Internal clock: 200 MHz Bus clock: 66.6 MHz Peripheral clock: 33.3 MHz
Integrated Development Environment	Renesas Electronics High-performance Embedded Workshop Ver.4.03.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.01 Release 01
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7670 Group Example of Initialization

2. Description of the Sample Application

This sample program varies the operating frequency of the CPG. The frequency multiplier for the PLL circuit is also varied, so time for PLL-synchronization to become stable is also required. The watchdog timer (WDT) is used to count the PLL-synchronization stabilization time.

2.1 Operational Overview of Modules Used

A PLL settling time is required when the multiplication ratio of the PLL circuit of the CPG is changed. The on-chip WDT counts this settling time.
In the case of changes to the PLL multiplication ratio, after the new value has been written to the frequency control register (FRQCR) of the CPG, operation of the internal CPG is temporarily paused and incrementation of the WDT starts. When the WDT overflows, clock supply by the CPG is restarted and the SH7670 LSI returns to operation.
Tables 1 and 2 are summaries of CPG and WDT features. Figures 1 and 2 show the block diagrams of CPG and WDT.

Table 1 Overview of CPG

Item	Description	
Clock operating mode	Four (mode 0, mode 1, mode 2, mode 3)	
Generated clock signals	Internal (Iϕ):	Used by the CPU and cache
	Peripheral (Pϕ):	Used by on-chip peripheral modules
	Bus (Bϕ):	Used by the external bus interface
Frequency changing function	Frequencies of the internal and peripheral clocks can be changed independently by the PLL and divider circuits in the CPG.	
Control of power-down modes	The clock can be stopped in sleep mode and software standby mode, and the specific modules can be stopped using the module standby function.	

Table 2 Overview of WDT

Item	Description
Number of channels	1
Counter	8-bit counter (counting up only)
Timer mode	Watchdog timer or interval timer
Pin function	None
Clock source	Pϕ, Pϕ/64, Pϕ/128, Pϕ/256, Pϕ/512, Pϕ/1024, Pϕ/4096, Pϕ/16384 Pϕ: Clock for on-chip peripheral modules
Method of activation	Watchdog timer/interval timer: Activated by software Frequency adjustment: Activated by software Release from software standby mode: Interrupt detection

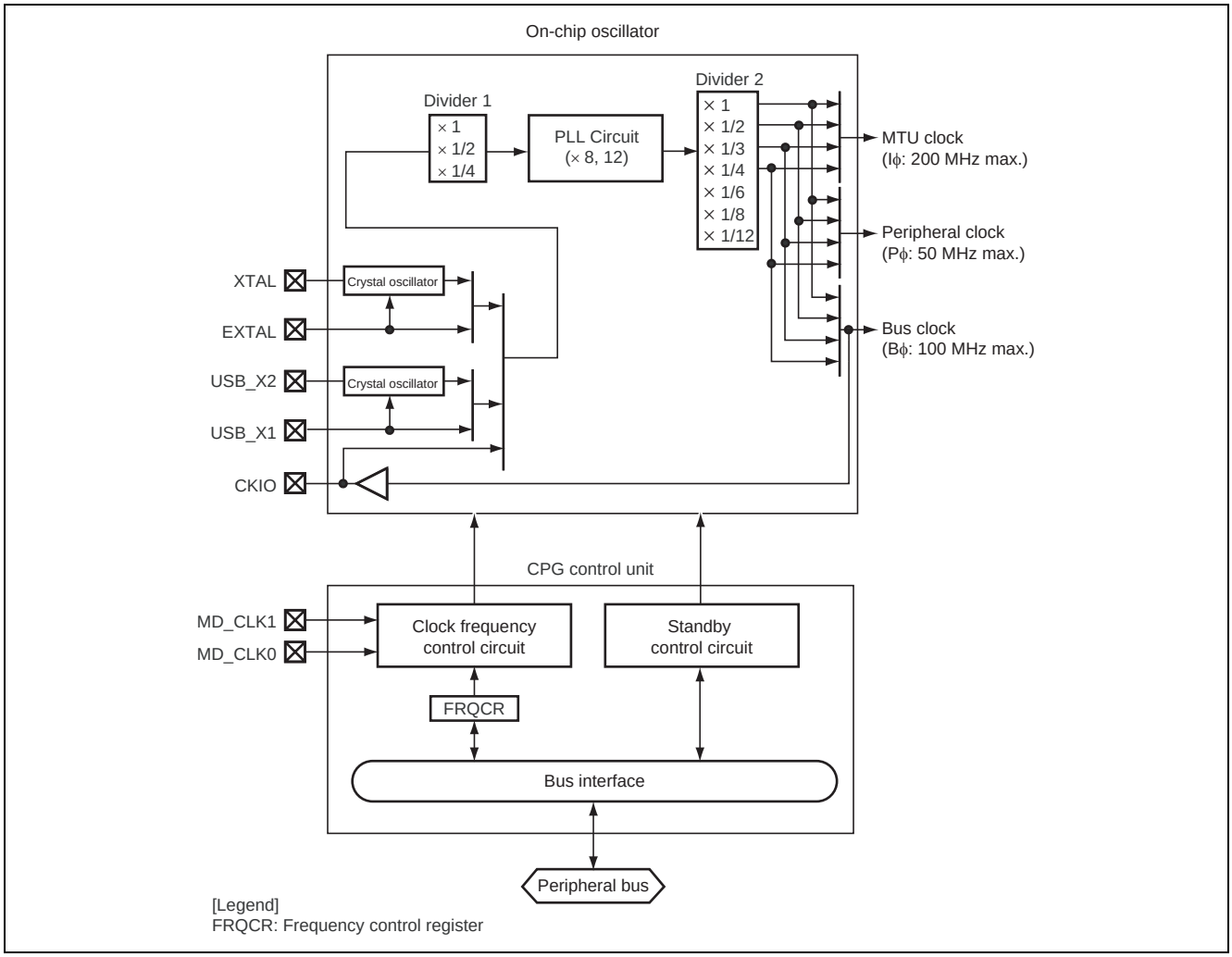

Figure 1 Block Diagram of the CPG

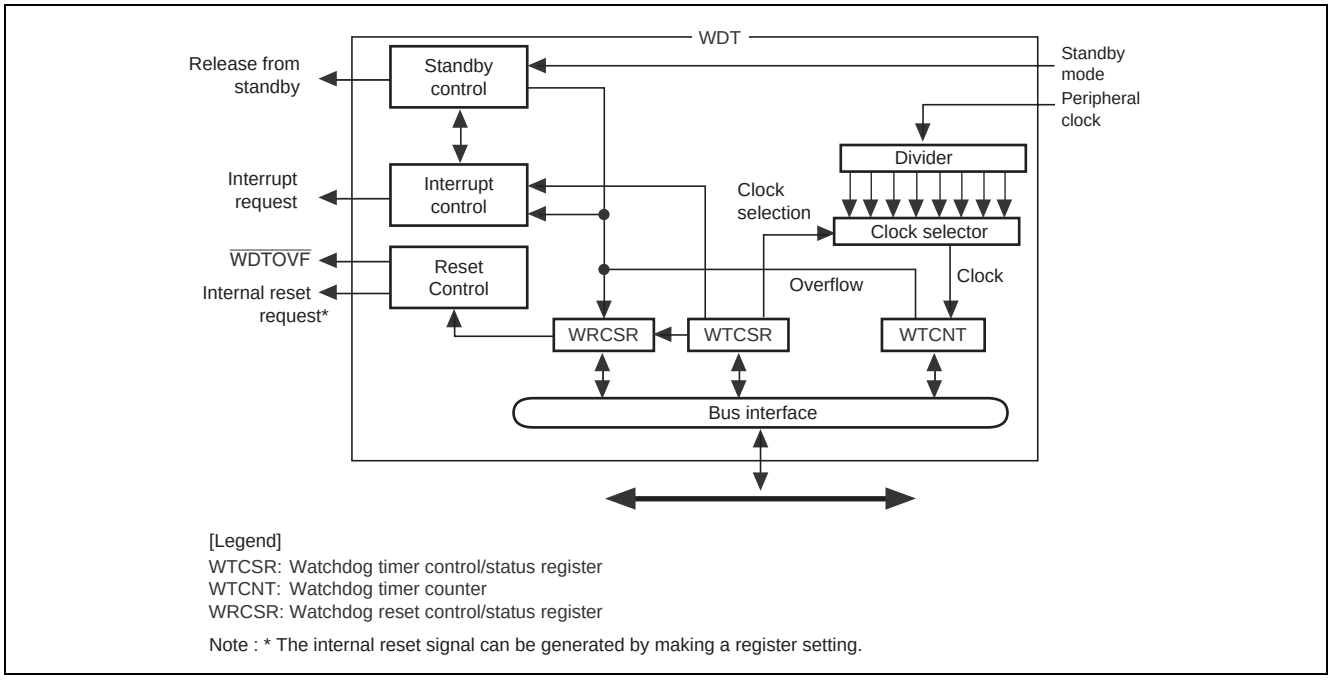

Figure 2 Block Diagram of the WDT

2.2 Procedure for Setting Modules Used

Figure 3 shows the procedure for settings to change the operating frequencies. For details on registers, refer to the *SH7670 Group Hardware Manual* (REJ09B0437).

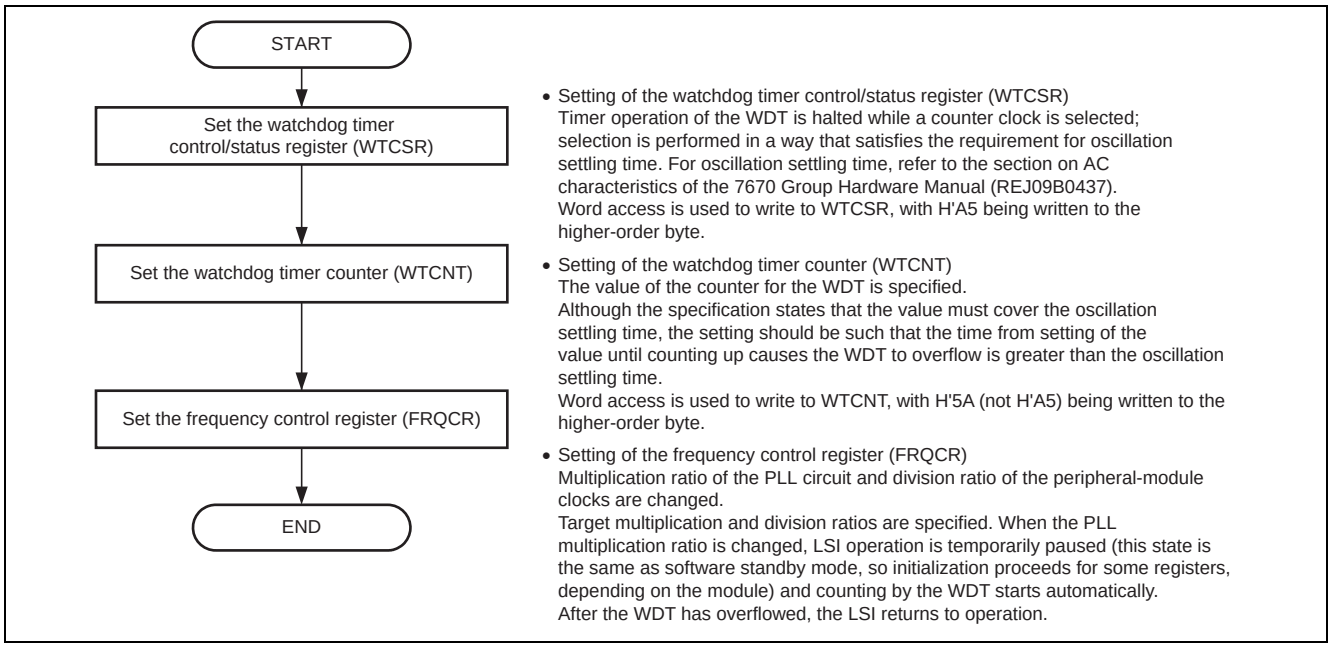

Figure 3 Flow for Settings to Change the Operating Frequency

2.3 Description of Operation by the Sample Program

In the sample program, processing to invert the levels on port pins is repeatedly performed. In response to input of the NMI, the corresponding interrupt processing routine changes the operating frequency as shown in table 3. Once the operating frequency has been changed, operation returns to function main. The rate of inversion of port pins changes with the change to the operating frequency.

Figure 4 shows the operation timing of the sample program.

Table 3 Operating Frequencies Set by the Sample Program

	Clock Operating Mode	FRQCR Setting	Clock Ratio (I : B : P)	Operating Frequencies (MHz) (I : B : P)
Initial operating frequency	Mode 0	H'1104	12 : 4 : 2	200 : 66.67 : 33.33
Operating frequency after change	Mode 0	H'1013	4 : 4 : 2	66.670 : 66.67 : 33.33

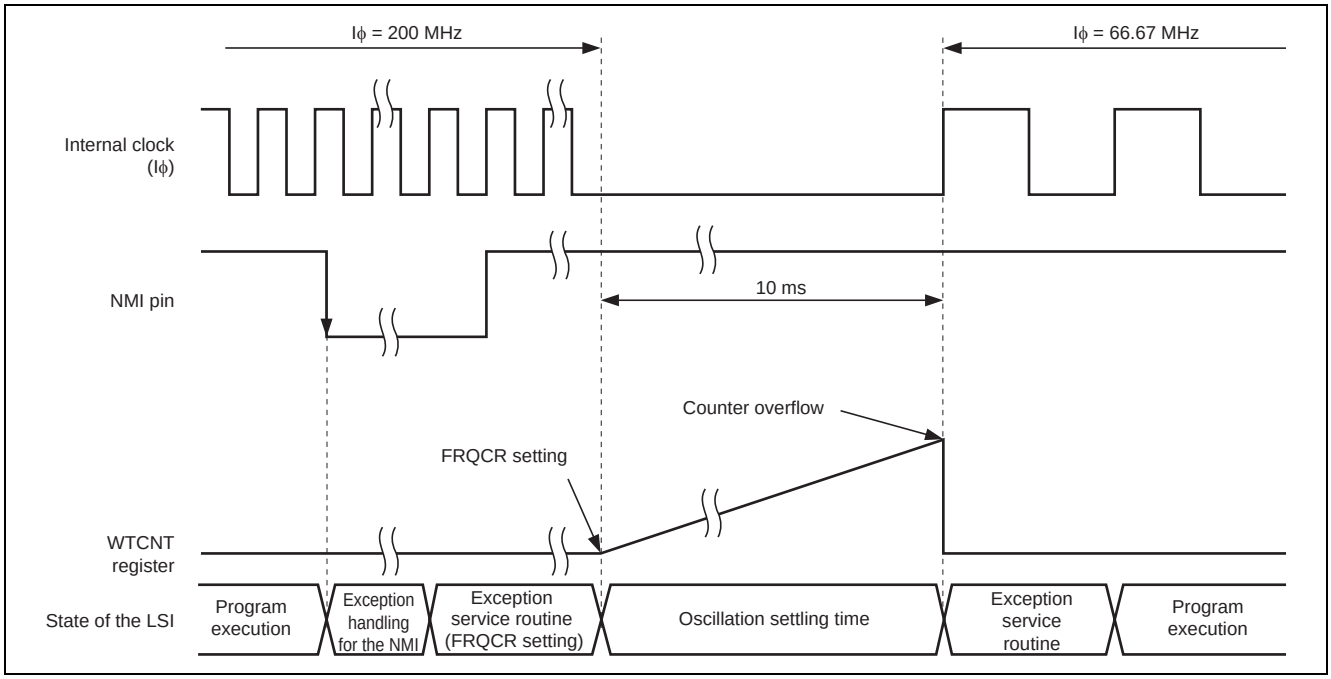

Figure 4 Operation Timing of the WDT

2.4 Procedure of Operation by the Sample Program

Table 4 shows the settings of registers at the time of the change to the operating frequency. Figures 5 and 6 show flows of processing by the sample program.

Table 4 Register Settings for Changing the Operating Frequency

Register Name	Address	Setting	Description
Watchdog timer control/status register (WTCSR)	H'FFFE 0000	H'A51E	• Interval timer mode • TME = 0: Timer is disabled. • CKS[2:0] = B'110: Pϕ/4096
Watchdog timer counter (WTCNT)	H'FFFE 0002	H'5AAD	• Initialization of timer counter (H'AD)
Frequency control register (FRQCR)	H'FFFE 0010	H'1013	• CKOEN[1:0] = B'01: Output of clock is enabled in normal operation. • STC[1:0] = B'00: × 8 (multiplication ratio for the PLL circuit) • IFC = 1: × 1/2 (frequency division ratio for the internal clock) • PFC[2:0] = B'100: × 1/4 (frequency division ratio for the peripheral clock)

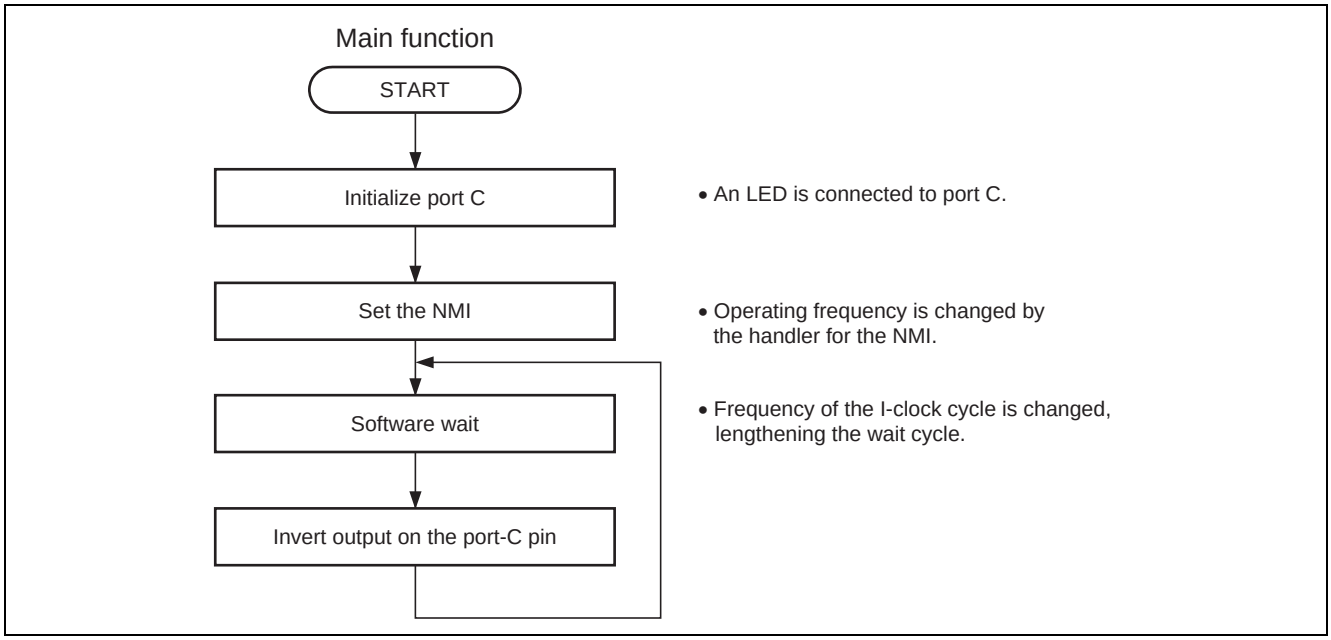

Figure 5 Processing Flow of Function main

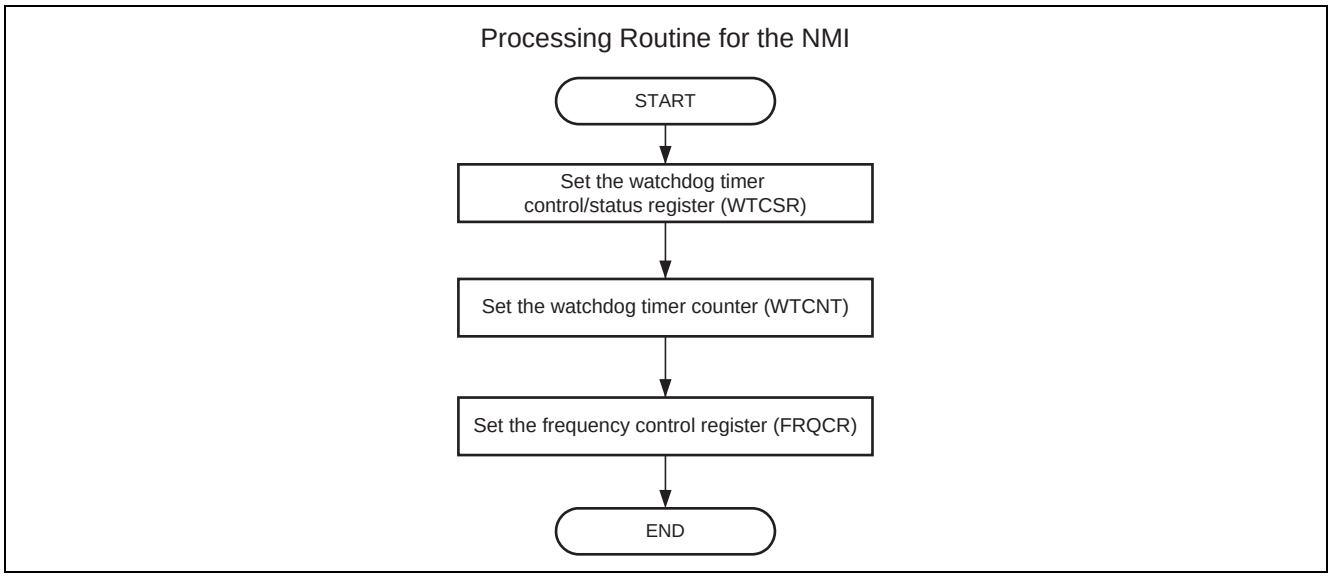

Figure 6 Flow of Processing Routine for the NMI

3. Sample Program Listing

3.1 Sample program list "main.c" (1)

```
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***********************************************************************
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*""FILE COMMENT""*********** Technical reference data *************************
*   System Name : SH7671 Sample Program
*   File Name   : main.c
*   Abstract    : Setting Sample on CPG Operatin Frequency Modification
*   Version     : 1.00.01
*   Device      : SH7671
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
*               : C/C++ compiler package for the SuperH RISC engine family
*               :                               (Ver.9.01 Release01).
*   OS          : None
*   H/W Platform: M3A-HS71(CPU board)
*   Description :
***********************************************************************
*   History     : Jul.05,2007 ver.1.00.00
*               : May 12,2010 ver.1.00.01 Changed the company name and device name
*""FILE COMMENT END""*****************************************************/
#include <machine.h>
#include "iodefine.h"
#include "defs.h"

/* ==== Prototype Declaration ==== */
void main(void);
```

3.2 Sample program list "main.c" (2)

```
51
52    /*""FUNC COMMENT""*****************************************************************
53     * ID          :
54     * Outline     : Main Function
55     *-------------------------------------------------------------------------------
56     * Include     : #include "iodefine.h"
57     *-------------------------------------------------------------------------------
58     * Declaration : void main(void)
59     *-------------------------------------------------------------------------------
60     * Function    : Port C7 output inversion processing
61     *             :
62     *-------------------------------------------------------------------------------
63     * Argument    : void
64     *-------------------------------------------------------------------------------
65     * ReturnValue : void
66     *-------------------------------------------------------------------------------
67     * Notice      :
68     *""FUNC COMMENT END""*************************************************************/
69    void main(void)
70    {
71      int i;
72
73      /* ==== Set LED7 as the user LED ==== */
74      /* ---- Set port C to input/output port ---- */
75      PORT.PCCRH1.BIT.PC20MD = 0;
76      /* ---- Set lights-off data ---- */
77      PORT.PCDRH.BIT.PC20DR  = 0;
78      /* ---- Set direction to output ---- */
79      PORT.PCIORH.BIT.PC20IOR = 1;
80
81      /* ==== NMI interrupt setting ==== */
82      INTC.ICR0.BIT.NMIE = 0;             /* Falling edge */
83
84      /* ==== LED output inversion processing ==== */
85      while(1){
86        for( i=0x100000; i>0; i-- ){
87            /* Wait processing */
88        }
89        PORT.PCDRH.BIT.PC20DR  ^= 1;
90      }
91    }
92
93    /* End of file */
```

3.3 Sample program list "intprg_NMI.c" (1)

```
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27    ***********************************************************************
28    * Copyright (C) 2007(2010) Renesas Electronics Corporation. All rights reserved.
29    *""FILE COMMENT""*********** Technical reference data *************************
30    *   System Name : SH7671 Sample Program
31    *   File Name   : intprg_NMI.c
32    *   Abstract    : interrupt entry function
33    *   Version     : 1.02.01
34    *   Device      : SH7671
35    *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36    *               : C/C++ compiler package for the SuperH RISC engine family
37    *               :                             (Ver.9.01 Release01).
38    *   OS          : None
39    *   H/W Platform: M3A-HS71(CPU board)
40    *   Description :
41    ***********************************************************************
42    *   History     : Jul.05,2007 ver.1.00.00
43    *               : Aug.07,2007 ver.1.01.00
44    *               : Sep.18,2007 ver.1.02.00
45    *               : May 12,2010 ver.1.02.01 Changed the company name and device name
46    *""FILE COMMENT END""*****************************************************/
47    #include <machine.h>
48    #include <stdio.h>
49    #include "vect.h"
50    #include "iodefine.h"
51
```

3.4 Sample program list "intprg_NMI.c" (2)

```
52    #pragma section IntPRG
53
54
55    // 4 Illegal code
56    void INT_Illegal_code(void)
57    {
58        /* sleep(); */
59    }
60    // 5 Reserved
61
62    // 6 Illegal slot
63    void INT_Illegal_slot(void)
64    {
65        /* sleep(); */
66    }
67    // 7 Reserved
68
69    // 8 Reserved
70
71    // 9 CPU Address error
72    void INT_CPU_Address(void)
73    {
74        /* sleep(); */
75    }
76
77    // 10 INT_DMAC_Address
78    void INT_DMAC_Address(void)
79    {
80        /* sleep(); */
81    }
82
```

3.5 Sample program list "intprg_NMI.c" (3)

```
83     // 11 NMI
84     /*""FUNC COMMENT""*************************************************************
85      * ID          :
86      * Outline     : Processing routine for the NMI
87      *-------------------------------------------------------------------------------
88      * Include     : #include "iodefine.h"
89      *-------------------------------------------------------------------------------
90      * Declaration : void PowerON_Reset_PC(void)
91      *-------------------------------------------------------------------------------
92      * Function    : Operating frequency is changed.
93      *             : I:B:P=200:66.6:33.3(12:4:2) -> I:B:P=66.6:66.6:33.3(4:4:2)
94      *             : In order to change the PLL multiplication ratio, settings for
95      *             : activation of the WDT to secure the settling time are also made.
96      *-------------------------------------------------------------------------------
97      * Argument    : void
98      *-------------------------------------------------------------------------------
99      * Return Value : void
100    *-------------------------------------------------------------------------------
101    * Notice      : Handling of mode-control pins is based on the condition
102    *             : MD_CK0:MD_CK1 = 0:0 (mode 0)
103    *""FUNC COMMENT END""*************************************************************/
104    void INT_NMI(void){
105      /* ==== Change of multiplication and division ratios for the CPG ==== */
106      /* ---- WDT setting ---- */
107      WDT.WTCSR.WORD = 0xa51e;    /* Stop + clock selection (Pf・096)       *
108                                   * Higher-order byte: 0xA5, word access   */
109      WDT.WTCNT.WORD = 0x5aad;    /* Clock oscillation settling time (10 ms)    *
110                                   * (0xFF-0xAC)*4096/33.3 MHz>10 ms           *
111                                  /* Higher-order byte: 0x5A, word access   */
112      /* ---- CPG setting ---- */
113      CPG.FRQCR.WORD = 0x1013;    /* If・= 66.6 MHz                         *
114                                   * Bf・= 66.6 MHz                         *
115                                   * Pf・= 33.3 MHz                         *
116                                   * CPU mode1, PLL1 x 8                       */
117
118      /* CPU operation is halted and started again after the WDT overflows. */
119
120    }

       /* Omitted */

929    /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7670 Group Hardware Manual Rev. 2.00
  The latest version of the hardware user's manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.24.08	—	First edition issued
1.01	Oct.15.10	—	Changed the sample program (AC Switching Characteristics are removed)

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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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