SH7268/SH7269 Groups

Example of Sampling Rate Converter

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Abstract

This application note describes the method to convert a sampling rate of sound data using the sampling rate converter of the SH7268/SH7269.

The features of the conversion function are listed below.

- Data format: 16-bit stereo/16-bit monaural
- Input sampling rate:

  Selectable from 8 kHz,11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz
- Output sampling rate:

  Selectable from 32 kHz, 44.1 kHz, 48 kHz

  (8 kHz and 16 kHz are selectable when input 44.1 kHz.)

Target Device

SH7268/SH7269 Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

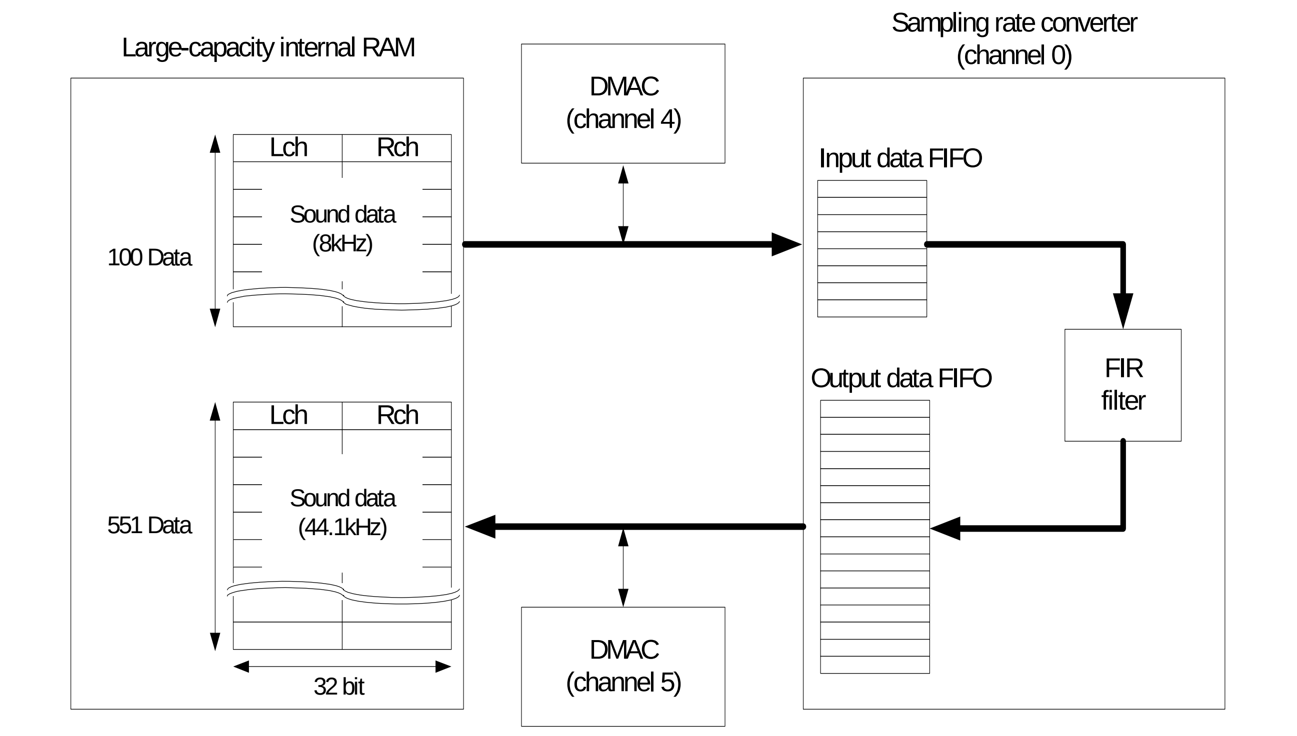
1. Specifications

Input the sampling rate of 8 kHz stored in the large-capacity internal RAM to the sampling rate converter channel 0 in order to convert the rate to 44.1 kHz. The converted sound data will be stored in the large-capacity internal RAM again. The direct memory access controller (hereinafter called the “DMAC”) is used for the data transmission.

Table 1.1 lists the peripheral functions and their applications. Figure 1.1 shows the operation overview.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Sampling Rate Converter (SRC)	Converts the sampling rate of the sound data
Direct Memory Access Controller (DMAC)	Inputs the sound data to the SRC, and transmits the conversion result.
Interrupt Controller (INTC)	Detects completion of the input of the converted data



Note: When the DMA transmission is executed to the cache valied are, a guarantee for the coherency between the cache and the memory with the software is required. The buffer is allocated in the cache invalid area for the sample code.

Figure 1.1 Operation Overview

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH7269
Operating frequency	CPU internal clock (Iφ): 266.67MHz Internal clock (Bφ): 133.33MHz Peripheral clock 1 (P1φ): 66.67MHz Peripheral clock 0 (P0φ): 33.33MHz
Operating voltage	Source power (I/O): 3.3V Source power (internal): 1.25V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC engine FamilyC/C++ Compiler Package Ver.9.03 Release02
	Complier option -cpu=sh2afpu -fpu=single. -includ"="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=allinfinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Board used	R0K572690C000BR

3. Reference Application Note(s)

For additional information associated with this document, refer to the following application note(s).

- SH7268/SH7269 Group Example of Initialization (RJ06B0998)

4. Software

4.1 Operation Overview

Figure 4.1 shows the sequence diagram of the sample code. The CPU waits until the DMA transmission of the input data has been completed after initializing the sampling rate converter and the DMAC. After the completion, the data in the process of conversion which left in the internal work memory of the sampling rate converter shall be converted to read out all of the output data (flush processing).

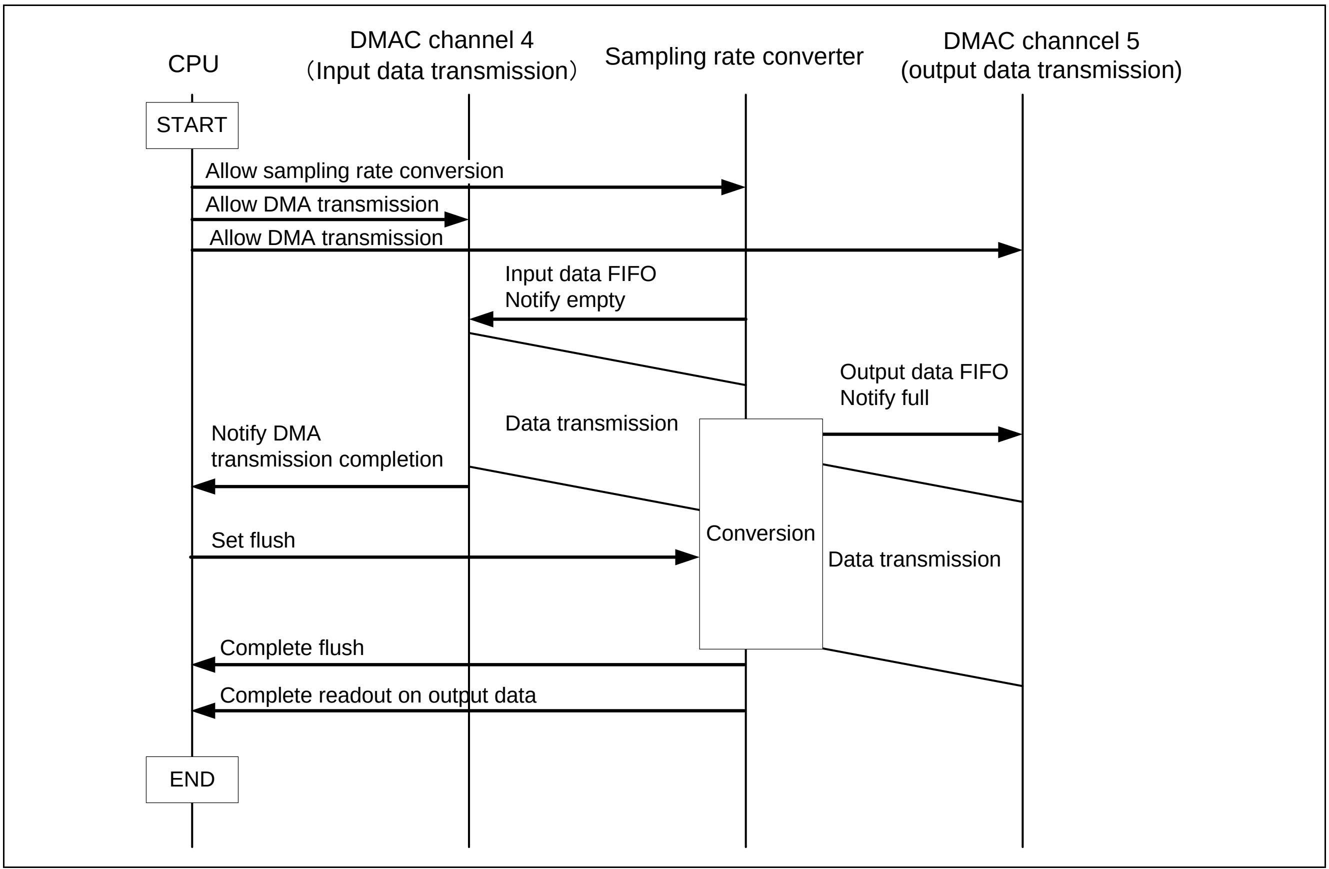


Figure 4.1 Sequence Diagram

4.2 File Configuration

Table 4.1 lists the files used in the sample code. The files automatically-generated in the Integrated development environment are excluded.

Table 4.1 File Configuration

File name	Description	Remarks
main.c	Main program	
io_src.c	Initializes the sampling rate converter	
io_src.h	Interface definition of io_src.c	
io_dmac.c	Initializes the DMAC	
io_dmac.h	Interface definition of io_dmac.c	

4.3 Constant(s)

Table 4.2 lists the constants used in the sample code.

Table 4.2 Functions Used in the Sample Code

Constant	Setting value	Description
SRC_BUFFER_SIZE	1024	User buffer size (by the long word)
SRC_INDATA_NUM	100	Sound data word counts before rate conversion
SRC_OUTDATA_NUM	551	Sound data word counts after rate conversion
SRC_IFS_8kHz	0x0000	Specified frequency value before rate conversion (8 kHz)
SRC_IFS_11_025kHz	0x0010	〃 (11.025 kHz)
SRC_IFS_12kHz	0x0020	〃 (12 kHz)
SRC_IFS_16kHz	0x0040	〃 (16 kHz)
SRC_IFS_22_05kHz	0x0050	〃 (22.05 kHz)
SRC_IFS_24kHz	0x0060	〃 (24 kHz)
SRC_IFS_32kHz	0x0080	〃 (32 kHz)
SRC_IFS_44_1kHz	0x0090	〃 (44.1 kHz)
SRC_IFS_48kHz	0x00A0	〃 (48 kHz)
SRC_OFS_8kHz	0x0004	Specified frequency value after rate conversion (8 kHz)
SRC_OFS_16kHz	0x0005	〃 (16 kHz)
SRC_OFS_32kHz	0x0000	〃 (32 kHz)
SRC_OFS_44_1kHz	0x0001	〃 (44.1 kHz)
SRC_OFS_48kHz	0x0002	〃 (48 kHz)

4.4 Variable(s)

Table 4.3 lists the static variables.

Table 4.3 Static Variables

Types	Variables name	Description	Function used
static uint32_t	src_buf_in [SRC_BUFFER_SIZE]	User buffer which stores the sound data before the rate conversion (allocated in the cache invalid area)	main
static uint32_t	src_buf_out [SRC_BUFFER_SIZE]	User buffer which stores the sound data after the rate conversion (allocated in the cache invalid area)	main

4.5 Function(s)

Table 4.4 lists the functions

Table 4.4 Function(s)

Function name	Description
main	Main processing
io_dmac4_dei4_isr	DEI interrupt function of the DMAC channel 4
io_dmac5_dei5_isr	DEI interrupt function of the DMAC channel 5
io_init_src0	Initialization of the sampling rate converter channel 0
io_init_dmac4	Initialization of the DMAC channel 4
io_init_dmac5	Initialization of the DMAC channel 5

4.6 Function Specifications

The function specifications of the sample code are listed below.

main	
Outline	Main processing
Header	No
Declaration	Void main(void)
Description	Converts the sampling rate of the sound data using the sampling rate converter and the DMAC. The DMAC channel 4 is used for the input data transmission of the sampling rate converter and the chancel 5 is used for the output data transmission.
Argument	No
Return value	No

io_dmac4_dei4_isr	
Outline	DEI interrupt function of the DMAC channel 4
Header	No
Declaration	void io_dmac4_dei4_isr(void)
Description	Executes the flush processing to the internal work memory of the sampling rate converter after forbidding the DMAC channel 4 operation.
Argument	No
Return value	No

io_dmac5_dei5_isr	
Outline	DEI interrupt function of the DMAC channel 5
Header	No
Decralation	void io_dmac5_dei5_isr(void)
Description	Forbids the DMAC channel 5 operaton.
Argument	No
Return value	No

io_init_src0		
Outline	Initialization of the sampling rate converter channel 0	
Headers	io_src.h	
Declaration	void io_init_src0(uint16_t inrate, uint16_t outrate)	
Description	Sets the sampling rate converter channel 0 and allows the rate conversion.	
Argument	uint16_t inrate	: Specifies frequency before the rate conversion.
	uint16_t outrate	: Specifies frequency after the rate conversion
Return value	No	

io_init_dmac4		
Outline	Initialization of the DMAC channel 4	
Heade	io_dmac.h	
Declaration	void io_init_dmac4(void * src, void * dest, int32_t count)	
Description	Sets the DMAC channel 4 and allows the DMA transmission from the transmit source to the transmit destination, which addresses are specified by the argument. The input data register of the sampling rate converter will be assigned as the transmit destination address. The DMA transmit completion interrupt is allowed. Note that a guarantee for the coherency between the cache and the memory is required when the cache valid area is assigned as the transmission source.	
Argument	void *src	: Transmit source address
	void *dest	: Transmit destination address
	int32_t count	: Number of transmissions
Return value	No	

io_init_dmac5		
Outline	Initialization of the DMAC channel 5	
Header	io_dmac.h	
Declaration	void io_init_dmac5(void * src, void * dest, int32_t count)	
Description	Sets the DMAC channel 5 and allows the DMA transmission from the transmit source to the transmit destination, which addresses are specified by the argument. The output data register of the sampling rate converter will be assigned as the transmit source address. The DMA transmit completion interrupt is allowed. Note that a guarantee for the coherency between the cache and the memory is required when the cache valid area is assigned as the transmission destination.	
Argument	void *src	: Transmit source address
	void *dest	: Transmit destination address
	int32_t count	: Number of transmission
Return value	No	

4.7 Flowchart(s)

4.7.1 Main processing

Figure 4.2 shows the procedure of the main processing.

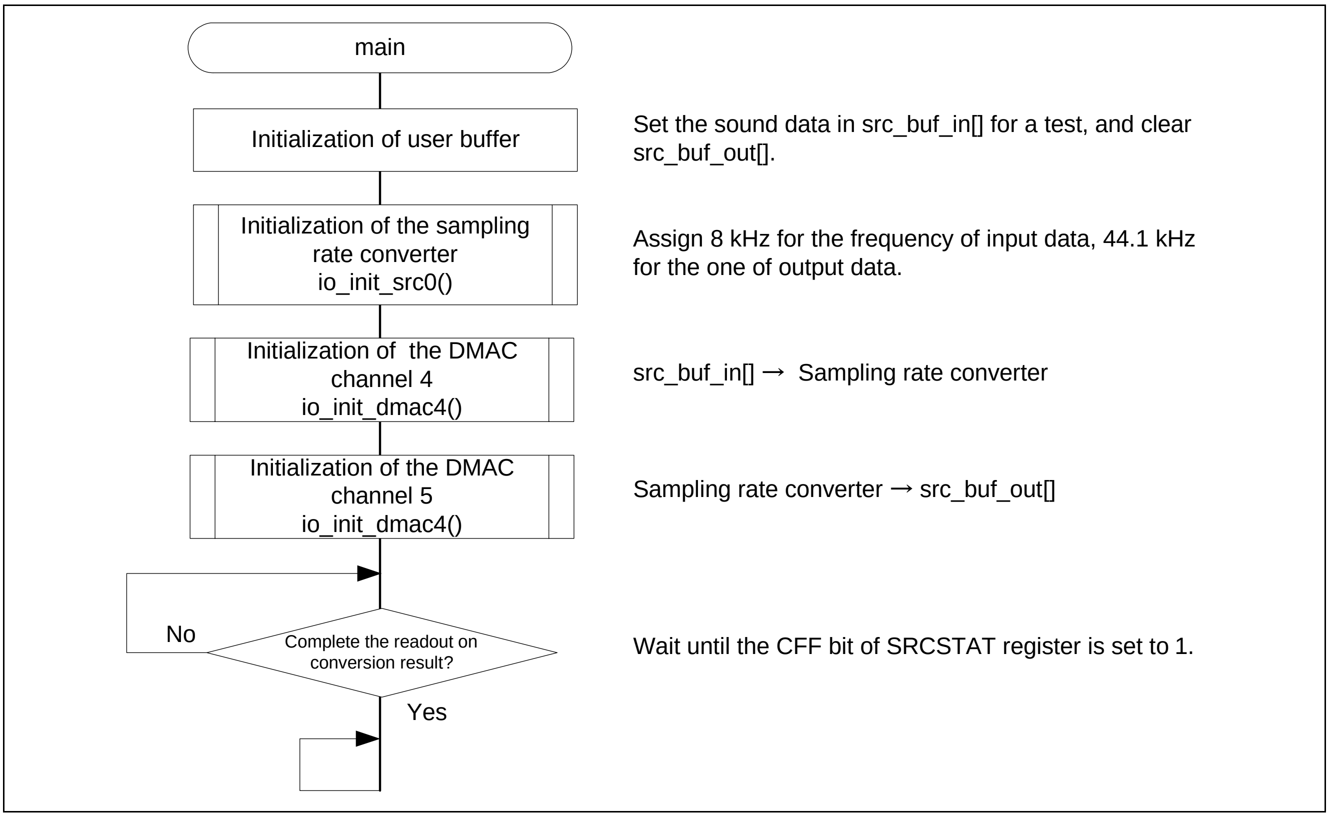


Figure 4.2 Main Processing

4.7.2 Initialization of the sampling rate converter

Figure 4.3 shows the initialization procedure of the sampling grate converter.

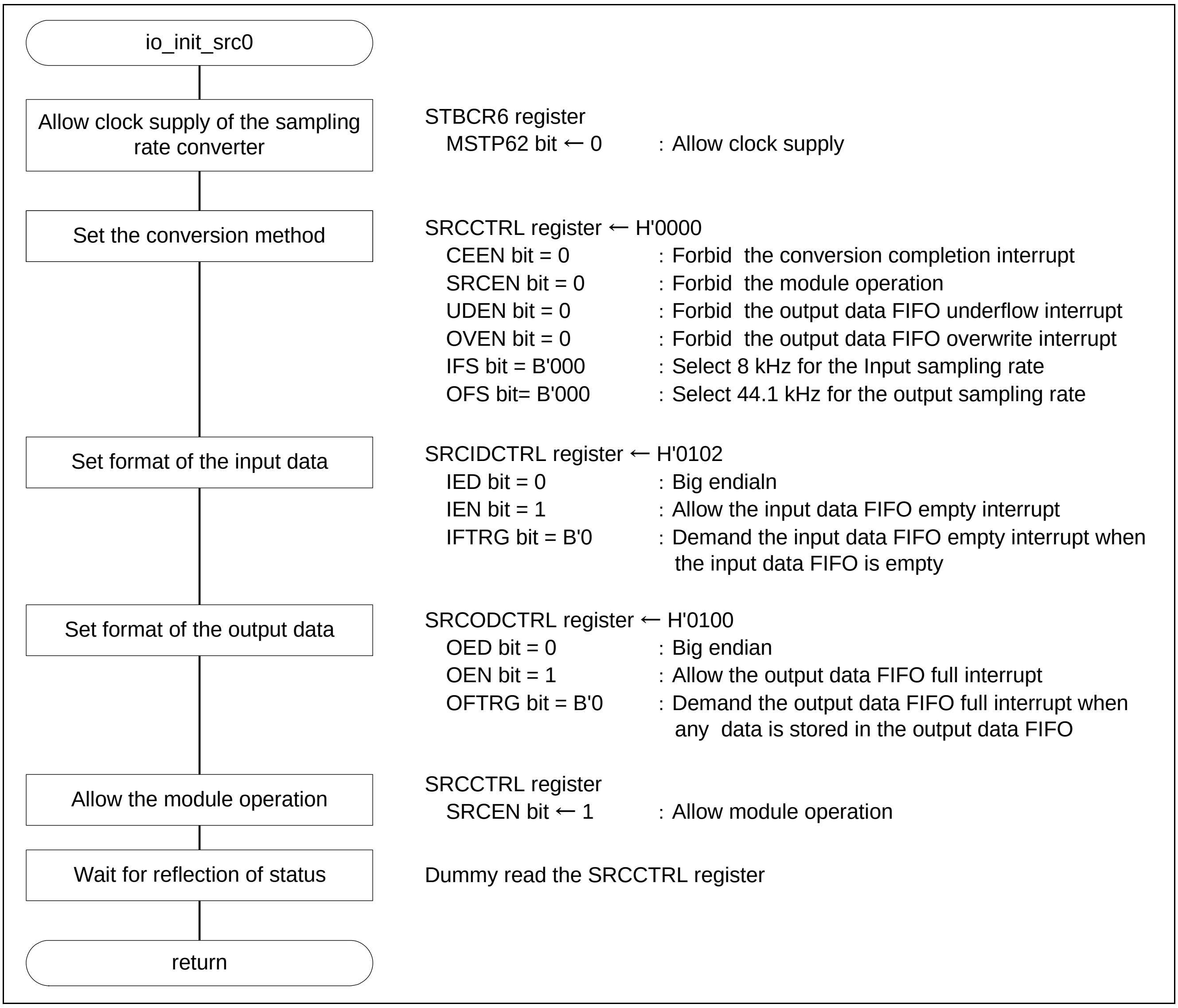
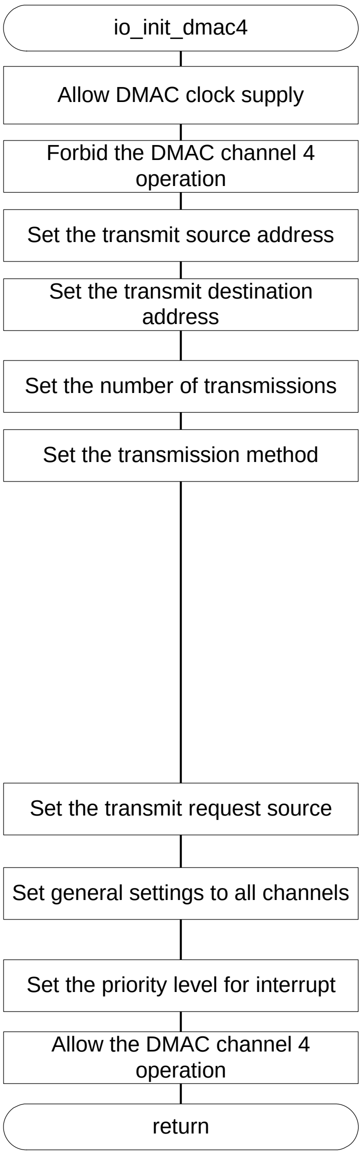


Figure 4.3 Initialization of Sampling Rate Converter

4.7.3 Initialization of the DMAC channel 4

Figure 4.4 shows the initialization procedure of the DMAC channel 4.



STBCR2 register
MSTP8 bit ← 0 : Allow clock supply

CHCR4 register
DE bit ← 0 : Forbid the DMAC channel 4 operation

SAR4 register ← &src_buf_in[0]
Assign the start address of the user buffer for input data as the transmit source address

DAR4 register ← &(SRC0.SRCID.LONG)
Assign input data register of the sampling rate converter channel 0 (SRCID) as the transmit destination.

DMATCR4 register ← SRC_INDATA_NUM (100)
Set the number of transmissions to 100 times

CHCR4 register ← H'0000 1814

TC bit = 0	: one transmission per transmit request
RLDSAR bit = 0	: SAR reload off
RLDDAR bit = 0	: DAR reload off
TEMASK bit = 0	: Stop the DMA transmission when the TE bit is set
HIE bit = 0	: Forbid the interrupt when the half of the number of transmissions has been completed
DM bit = B'00	: Fix the destination address
SM bit = B'01	: Increase source address
RS bit = B'1000	: Select transmission request source at the extension resource sector (DMARS)
TB bit = 0	: Cycle stealing mode
TS bit = B'10	: Transmit by the long word (4-byte)
IE bit = B'1	: Allow transmit completion interrupt

DMARS2 register
CH4 bit ← H'41 : Set the input data FIFO empty interrupt of the sampling rate converter (channel 0) to the transmission request

DMAOR register ← H'0007

CMS bit = B'00	: Select normal mode for the cycle stealing mode
DME bit = 1	: Allow operations of all channels

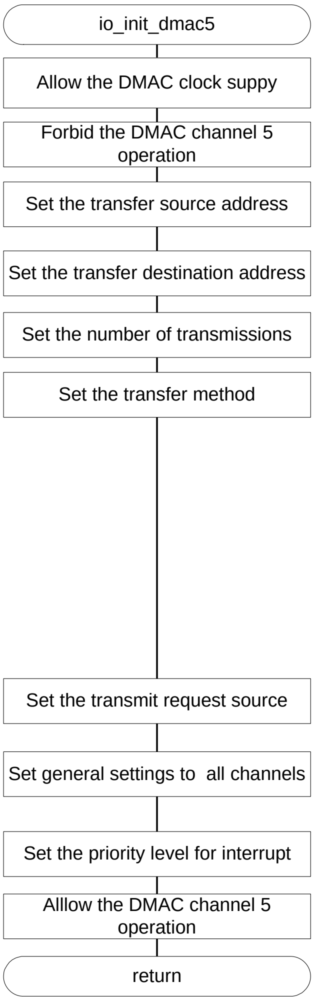
IPR07 register
_DMAC4 bit ← 3 : Set the priority level 3 to the DMAC channel 4 transmit completion interrupt (interrupt allowed)

CHCR4 register
DE bit ← 1 : Allow the DMAC channel 4 operation

Figure 4.4 Initialization of DMAC channel 4

4.7.4 Initialization of the DMAC channel 5

Figure 4.5 shows the initialization procedure of the DAMC channel 5.



STBCR2 register
MSTP8 bit ← 0 : Allow clock supply

CHCR5 register
DE bit← 0 : Forbid the DMAC channel 5 operation

SAR5 register ← &(SRC0.SRCOD.LONG)
Assign output data register of the sampling rate converter channel 0 (SRCOD) as the transmit destination

DAR5 register ← &src_buf_out[0]
Assign the start address of the user buffer for output data as the transmit source address

DMATCR5 register ← SRC_OUTDATA_NUM（551）
Set the number of transmissions to 551 times

CHCR5 register ← H'0000 4814

TC bit = 0	: on transmission per transit request
RLDSAR bit = 0	: SAR reload off
RLDDAR bit = 0	: DAR reload off
TEMASK bit = 0	: Stop the DMA transmission when TE bit is set
HIE bit= 0	: Forbid the interrupt when the half of the transmissions has been completed
DM bit = B'01	: Increase the destination address
SM bit = B'00	: Fix the transmit source address
RS bit= B'1000	: Select transmission request source at the extension resource sector (DMARS)
TB bit = 0	: Cycle stealing mode
TS bit = B'10	: Transmit by the long word (4-byte)
IE bit= B'1	: Allow the transmit completion interrupt

DMARS2 register
CH5 bit ← H'42 : Set the output data FIFO full interruption of the sampling rage converter (channel 0) to the transmission request

DMAOR register ← H'0007
CMS bit = B'00 : Select normal mode for the cycle stealing mode for
DME bit = 1 : Allow operations of all channels

IPR07 register
_DMAC5 bit ← 3 : Set the priority level 3 for the DMAC channel 5 transmit request interrupt

CHCR5 register
DE bit ← 1 : Allow the DMAC channel 5 operation

[Note] The output data size is determined by the following method;
The number of output samples = (The number of input data ×n - 1) × (Output sampling rate / (input sampling rate ×n)) + 1
(The “n” is the value depending on the converting rate. When the rate is 8 kHz to 44.1 kHz, the value of n is 6.)

Figure 4.5 Initialization of DMAC channel 5

4.7.5 Transmit completion interrupt of the DMAC

Figure 4.6 shows the procedure of the DMA transmit completion interrupt.

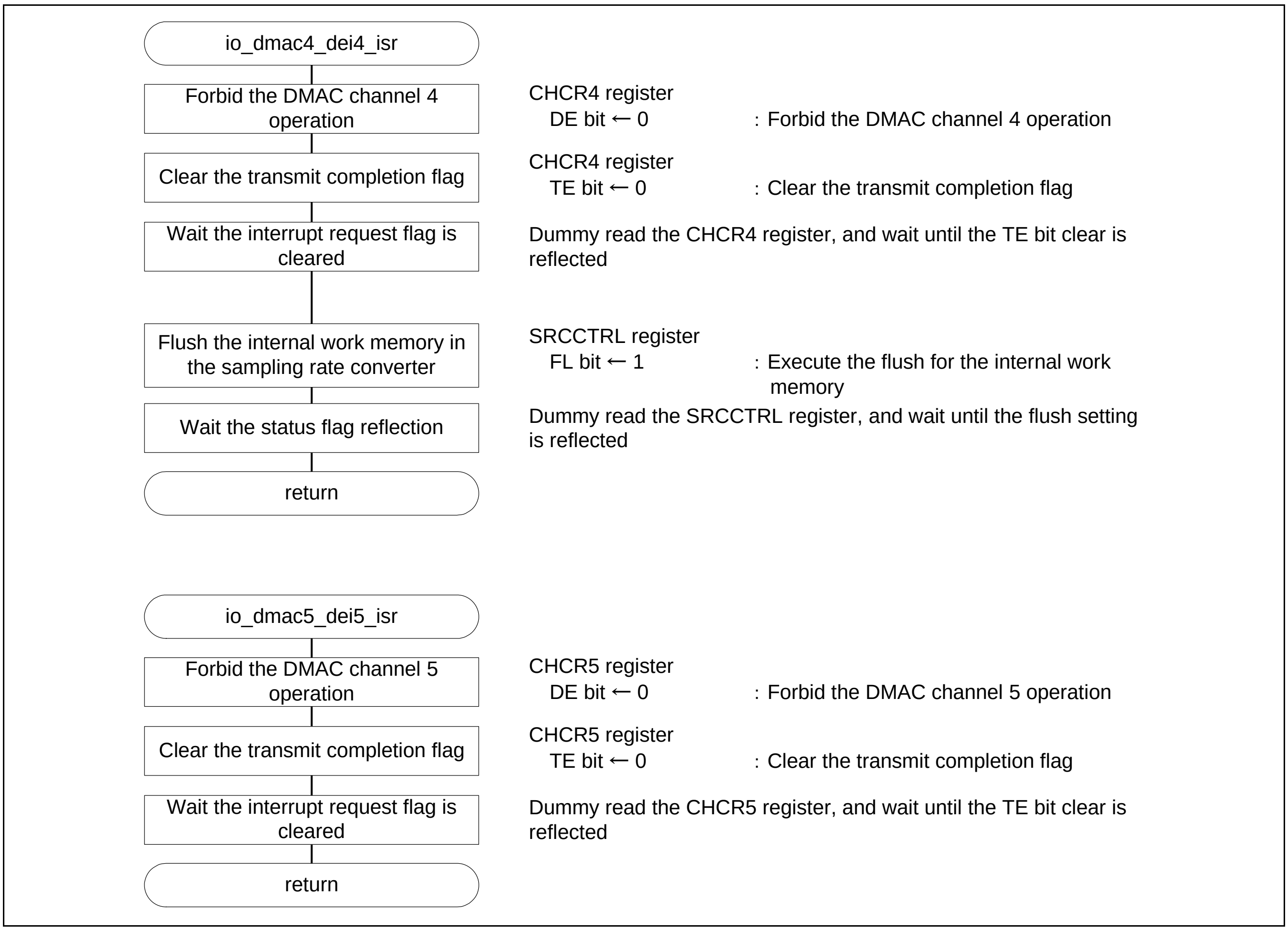


Figure 4.6 DMA transmit completion

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

Hardware Manual

SH7268/SH7269 Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

SuperH RISC Engine Family C/C++ Compiler Package V.9.04
C Complier User’s Manual Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

SuperH Family E10A-USB Emulator User’s Manual Rev.9.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	SH7268/SH7269 Group Application Note Example of Sampling Rate Converter

Rev.	**Date**	**Description**	
		Page	**Summary**
1.00	**Jun. 25, 2012**	**—**	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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