SH7268/SH7269 Group

Renesas Serial Peripheral Interface

Transmission/Reception in Slave Mode

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Abstract

This document describes transmission and reception in slave mode of the Renesas Serial Peripheral Interface (hereinafter called RSPI) for the SH7269.

Products

SH7268/SH7269 (herein after called as "SH7269")

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Set the RSPI for the SH7269 to slave mode and connect to the SPI master device. When receiving 'R' from the master device, returns the strings "Renesas Electronics Corporation". Use mode 3 for the SPI operating mode, and use interrupts for transmission/reception and error detection.

Note: When the transfer period is short, the response from the slave may not meet the required timing as the slave processes data with the software.

Table 1.1 lists the peripheral functions and applications. Figure 1.1 and Figure 1.2 show the operation overview, and operation timing in SPI mode3, respectively.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Renesas Serial Peripheral Interface	Interface as SPI slave device
Interrupt Controller	Transmission/reception and error notification of SPI communication

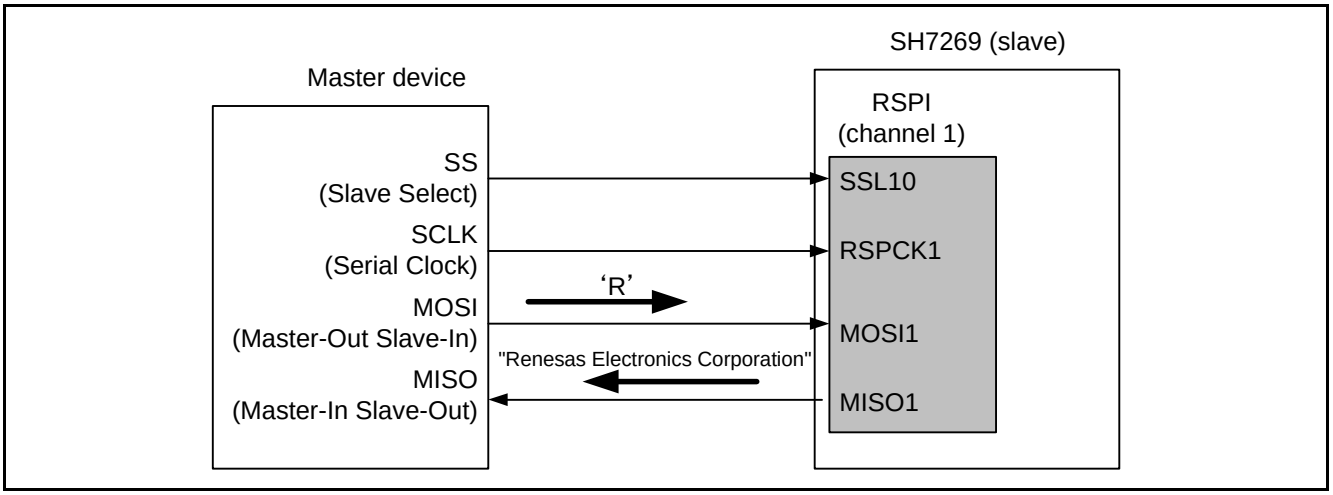


Figure 1.1 Operation Overview

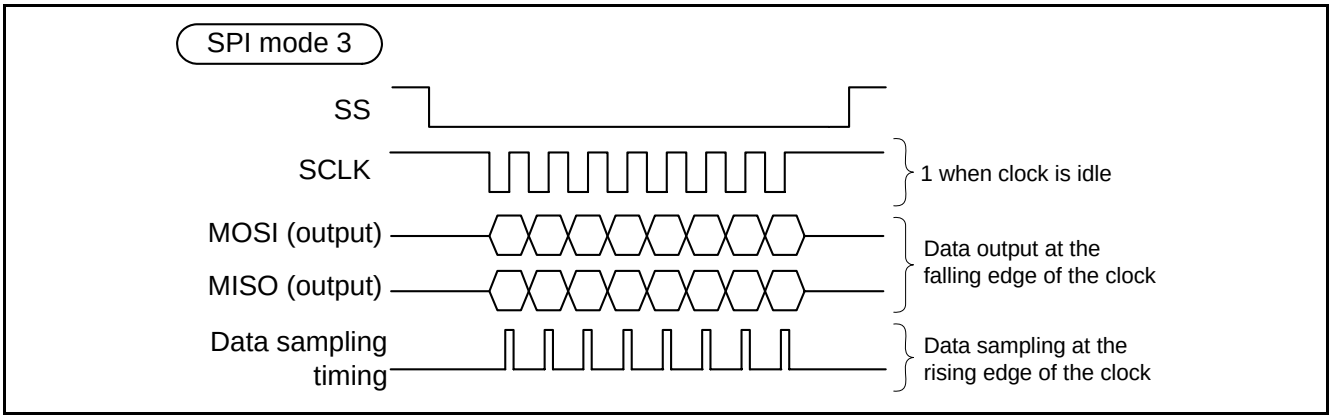


Figure 1.2 Operation Timing in SPI Mode 3

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH7269
Operating frequency	• CPU internal clock (Iϕ): 266.67MHz • Internal clock (Bϕ): 133.33MHz • Peripheral clock 1 (P1ϕ): 66.67MHz • Peripheral clock 0 (P0ϕ): 33.33MHz • RSPCK clock: 8.33MHz
Operating voltage	• PVcc: 3.3V • Vcc: 1.25V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver. 4.07.00
C compiler	Renesas Electronics Corporation SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release02
	Compiler option -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Operating mode	Boot mode 0 (boot from the memory of 16-bit bus width connected to CS0 space)
Sample code version	1.00
Board used	Renesas Electronics Corporation SH7269CPU board (mode: R0K572690C000BR)
Device used	Renesas Electronics Corporation SPI master device (model: R5S72643)

3. Reference Application Note

For additional information associated with this document, refer to the following application note(s).

- SH7262/SH7264 Group Example of Initialization (REJ06B0847)

4. Peripheral Functions

This chapter provides supplementary information on the RSPI slave mode. Refer to the "SH7269 Group User's Manual: Hardware" for basic information.

4.1 Features of Slave Mode

Table 4.1 lists the major differences between slave mode and master mode. For the initial setting to use slave mode, refer to Figure 6.5 RSPI Initialization Function.

Table 4.1 Differences from Master Mode

Item	Slave Mode		Master Mode
	CPHA bit = 0	CPHA bit = 1	
Pin input/output	RSPCK/SSL/MOSI: input MISO: output		RSPCK/SSL/MOSI: output MISO: input
Clock source	RSPCK input		On-chip baud rate generator
Maximum transfer rate	up to P1ϕ/8		up to P1ϕ/2
Error detection	Following errors are detectable: • Overrun error • Mode fault error		Not supported
Sequence control	Not supported (uses only SPCMD0)		Supported (selectable from the sequence of data length 1 to 4.)
Transfer initiation	SSL assert	RSPCK edge input *	Start transfer by either of the followings: • Writing the data register (SPDR) • Setting the dummy data transmit enable bit (TXDMY bit)
Burst transfer	Not possible	Possible	Possible
Three-wire system SPI	Not possible (SSL required)	Possible	Possible

Note: * When serial transfer is started with the transmit FIFO empty, the value stored in the shift register (the data received in the previous serial transfer) is transmitted.

4.2 Interface Timing of Slave Mode

Figure 4.1 shows a timing chart of slave mode (SPI mode 3). When using the SPI mode 3, set the CPOL bit to 1 and the CPHA bit to 1. By setting the CPHA bit to 1, burst transfer is enabled.

Table 4.2 lists the timing conditions of the SH7269 to be in slave mode. Table 4.3 lists the timing conditions of the coresponding master device. Make sure that timing conditions in both devices should be satisfied.

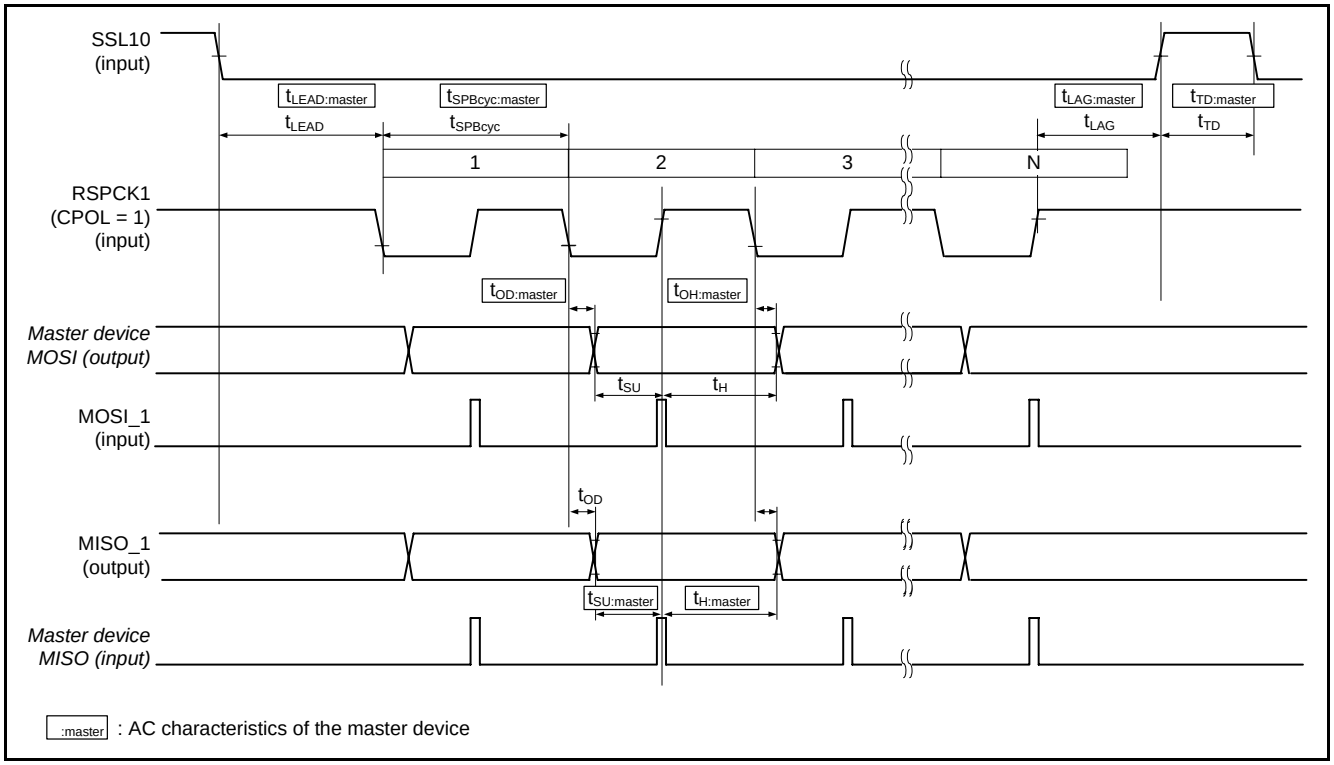


Figure 4.1 Timing Chart of Slave Mode (SPI Mode 3)

Table 4.2 RSPI (Slave Mode) Timing Conditions

Symbol	Item	Description
t_{LEAD}	SSL set up time	Time required from SSL assert initial clock input. Fulfill the following condition. $t_{LEAD:master} \geq t_{LEAD}$ (min)
t_{TD}	Continuous transmission delay time	Time required for SSL negation period. Fulfill the following condition. $t_{TD:master} \geq t_{TD}$ (min)
t_{SPcyc}	RSPCK clock cycle	Minimum clock cycle supportable. Fulfill the following condition. $t_{SPcyc:master} \geq t_{SPcyc}$ (min)
t_{LAG}	SSL hold time	Time required from the RSPCK final edge to the SSL negation. Fulfill the following condition. $_{LAG:master} + (t_{SPBcyc:master} \times 1/2) \geq t_{LAG}$ (min)
t_{SU}	Data input setup time	Set up time required for data input. Fulfill the following condition. $(t_{SPcyc:master} \times 1/2) - t_{OD:master}(max) \geq t_{SU}$ (min)
t_{H}	Data input hold time	Hold time required for data input. Fulfill the following condition. $t_{OH:master}(min) + (t_{SPcyc:master} \times 1/2) \geq t_{H}$ (min)

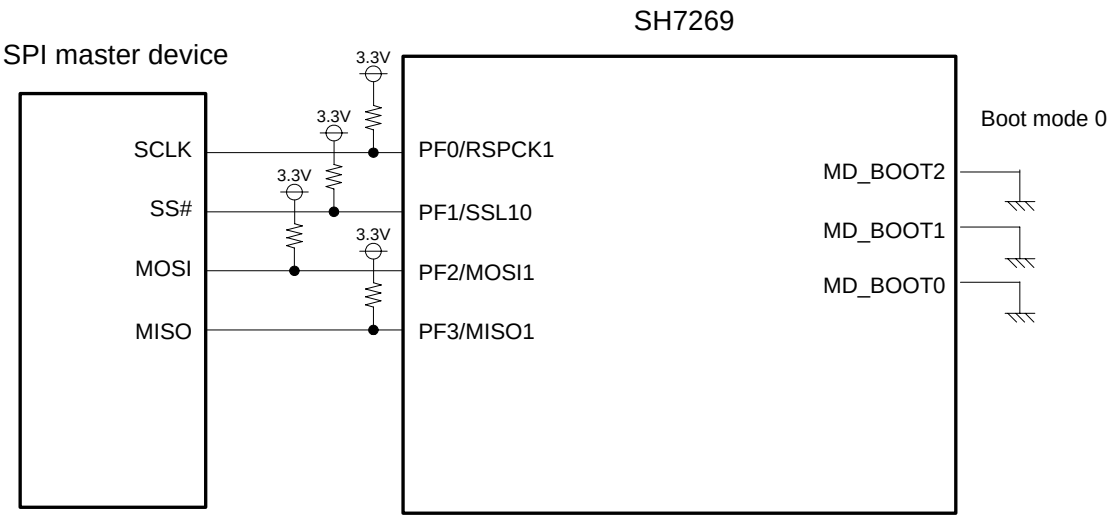
Table 4.3 Master Device Timing Conditions

Symbol	Item	Description
$t_{SU:master}$	Data input setup time	Set up time required for data input. Fulfill the following condition. $(t_{SPcyc:master} \times 1/2) - t_{OD}(max) \geq t_{SU:master}$ (min)
$t_{H:master}$	Data input hold time	Hold time required for data input. Fulfill the following condition. $t_{OH}(min) + (t_{SPcyc:master} \times 1/2) \geq t_{H:master}$ (min)

5. Hardware

5.1 Hardware Configuration

Figure 5.1 shows a connection example.



Note: "#" represents the negative logic or low active.

Figure 5.1 Connection Example

5.2 Pins Used

Table 5.1 lists the pins used and their functions.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
RSPCK1	**Input**	Interface as the SPI slave device (clock input)
SSL10	**Input**	Interface as the SPI slave device (slave select input)
MOSI1	**Input**	Interface as the SPI slave device (data input)
MISO1	**Output**	Interface as the SPI slave device (data output)

6. Software

6.1 Operation Overview

Set the RSPI channel 1 in the slave device that supports the SPI mode 3.

Read a receive data with the receive buffer full interrupt (SPFI). When receiving 'R', enables transmit buffer empty interrupt (SPTI) and transmits the character string "Renesas Electronics Corporation".

Detect communication errors with the error interrupt (SPEI). When a mode fault error occurs, clear the transmit/receive buffer, initialize the RSPI module to resume transmission. When an overrun error occurs, the receive data is read with the receive buffer full interrupt, not with the error interrupt.

Note: When the transfer period is short, the response from the slave may not meet the required timing as the slave processes data with the software.

6.2 File Composition

Table 6.1 lists the files used in the sample code. Files not generated by the integrated development environment should not be listed in this table.

Table 6.1 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing	
rspi_slave.c	RSPI (slave mode) initial setting and transmit/receive processing	
rspi_slave.h	Interface definition for spi_slave.c	

6.3 Variables

Table 6.2 shows the static type variable.

Table 6.2 static Variable

Type	Variable Name	Contents	Functions Used
volatile int32_t	tx_start_req	Request flag for transfer start	io_rspi_slave_spri_isr io_rspi_slave_spti_isr

6.4 Functions

Table 6.3 lists the functions.

Table 6.3 Functions

Function Name	Outline
main	Main function
io_rspi_slave_init	RSPI initial setting (slave mode)
io_rspi_slave_spei_isr	RSPI error interrupt processing (slave mode)
io_rspi_slave_spri_isr	RSPI receive buffer full interrupt processing (slave mode)
io_rspi_slave_spti_isr	RSPI transmit buffer empty interrupt processing (slave mode)

6.5 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main function
Header	None
Declaration	void main(void)
Description	Initializes the Renesas Serial Peripheral Interface (RSPI) to enable the slave operation. Transmission/reception, and error processing are dealt with interrupts.
Arguments	None
Return Value	None

io_rspi_slave_init	
Outline	RSPI initial setting (slave mode)
Header	rspi_slave.h、iodefine.h
Declaration	void io_rspi_slave_init(void)
Description	Initializes the Renesas Serial Peripheral Interface (RSPI), and enables the slave operation.
Arguments	None
Return Value	None

io_rspi_slave_spei_isr	
Outline	RSPI error interrupt processing (slave mode)
Header	iodefine.h
Declaration	void io_rspi_slave_spei_isr (void)
Description	This function is executed when a mode fault error or an overrun error occurs. For an overrun error, clears the flag to end the processing. In this case, read the data as soon as possible as the data is remained in the buffer. For a mode fault error, discards the data and initializes the module.
Arguments	None
Return Value	None

io_rspi_slave_spri_isr	
Outline	RSPI receive buffer full interrupt processing (slave mode)
Header	iodefine.h
Declaration	void io_rspi_slave_spri_isr (void)
Description	This function is executed when the receive data size exceeds the receive buffer data count trigger. Reads receive data for one byte. When receiving 'R', sets the variable to request transfer start, and enables transmit interrupt.
Arguments	None
Return Value	None

io_rspi_slave_spti_isr	
Outline	RSPI transmit buffer empty interrupt processing (slave mode)
Header	iodefine.h
Declaration	void io_rspi_slave_spti_isr (void)
Description	This function is executed when the data size in the transmit buffer falls below the transmit buffer data count trigger. When detecting a request for starting transmission, writes the transmit data (“Renesas Electronics Corporation”) in the empty area of the transmit FIFO, and disables the transmit interrupt. When the transmit FIFO becomes full, ends the processing.
Arguments	None
Return Value	None

6.6 Flowcharts

6.6.1 Main Processing

Figure 6.1 shows the main processing.

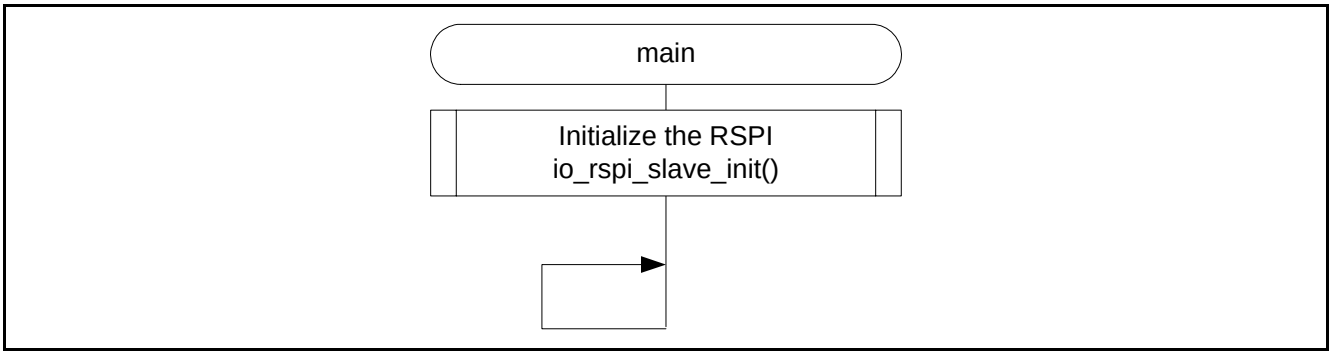


Figure 6.1 Main Processing

6.6.2 RSPI Error Interrupts

Figure 6.2 shows a procedure of the error interrupt function (SPEI).

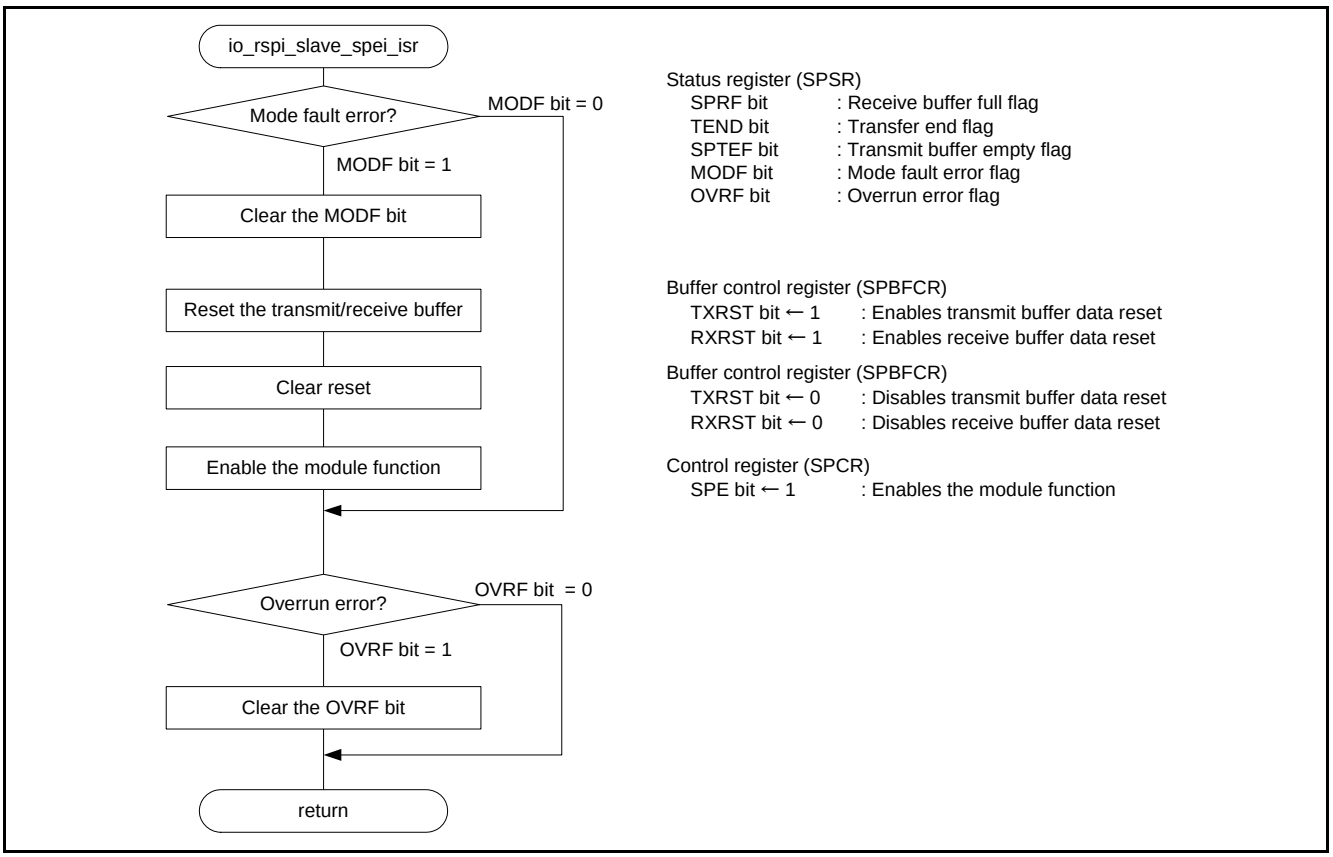


Figure 6.2 Error Interrupt Function (SPEI)

6.6.3 RSPI Receive Buffer Full Interrupt

Figure 6.3 shows a procedure of the receive buffer full interrupt function (SPRI).

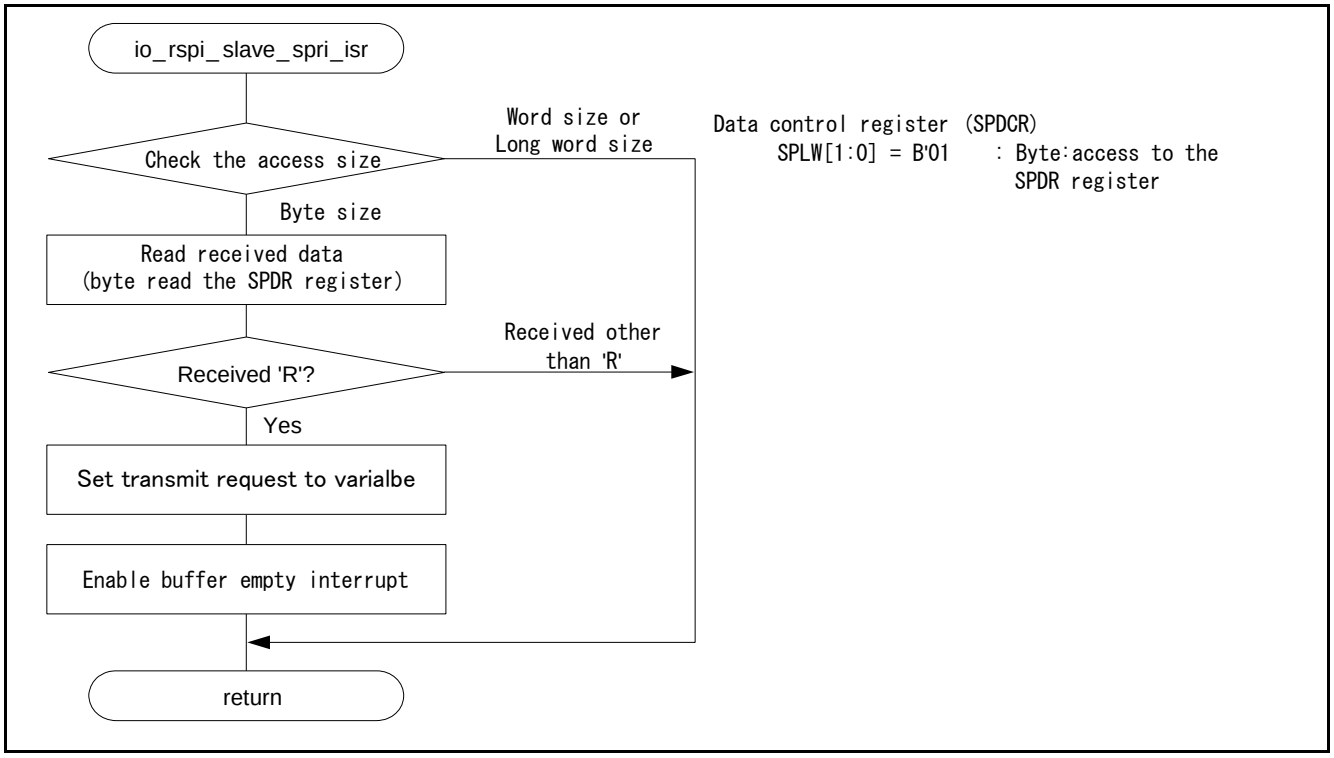


Figure 6.3 Receive Buffer Full Interrupt Function (SPRI)

6.6.4 RSPI Transmit Buffer Empty Interrupt

Figure 6.4 shows a procedure of the transmit buffer empty interrupt function (SPTI).

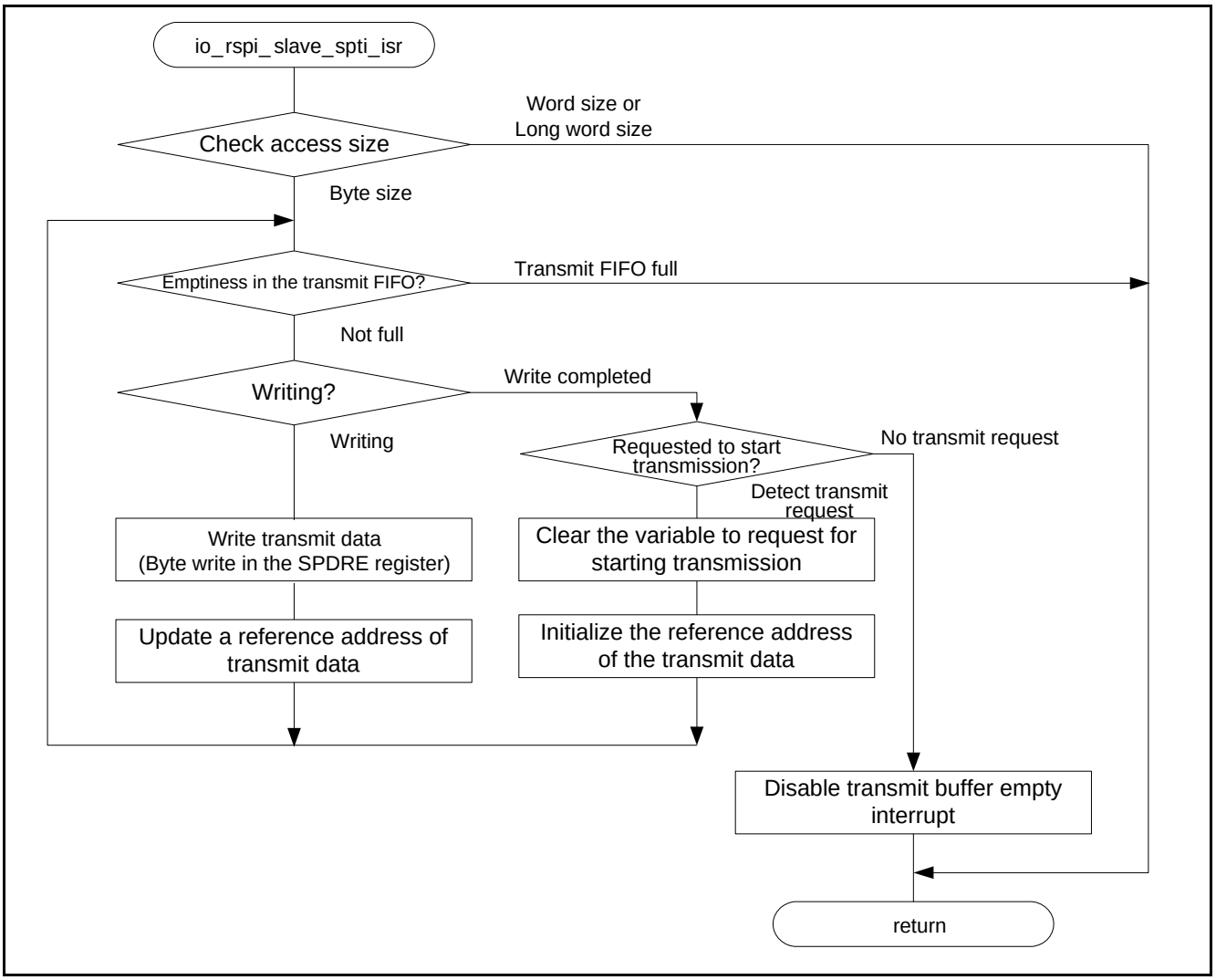


Figure 6.4 Transmit Buffer Empty Interrupt Function (SPTI)

6.6.5 Initializing RSPI

Figure 6.5 shows a procedure of the RSPI initialization function.

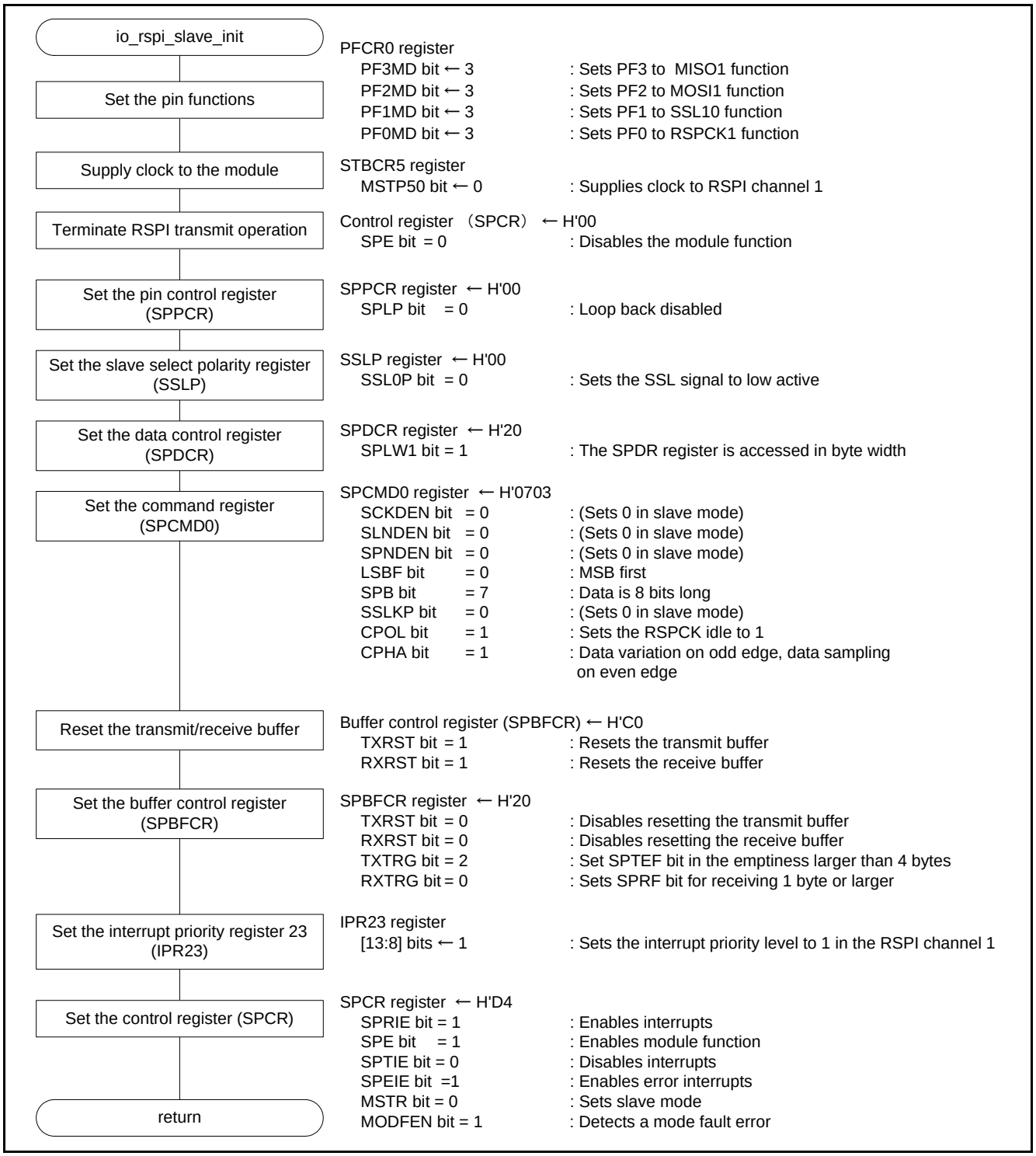


Figure 6.5 RSPI Initialization Function

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware
SH7268 Group, SH7269 Group User's Manual: Hardware Rev.1.00 (R01UH0048EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools
SuperH C/C++ Compiler Package V.9.04 User's Manual Rev.1.01 (R20UT0704EJ)
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	SH7269 Group Application Note Renesas Serial Peripheral Interface Transmission/Reception in Slave Mode

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 24, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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