SH7262/SH7264 Group

Video Display Controller 3 TFT-LCD Interfacing Example

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Summary

This application note shows the TFT-LCD interfacing example using the SH7262/SH7264 Microcontrollers (MCUs) on-chip Video Display Controller (VDC3).

Target Device

SH7264 MCU

Contents

1. Introduction

1.1 Specifications

The SH7264 MCU on-chip video display controller (VDC3) is connected with a TFT-LCD panel to display the still image.

1.2 Modules Used

- Video display controller (VDC3)
- General-purpose I/O ports

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group Video Display Controller 3 Video Display Example
- SH7262/SH7264 Group Video Display Controller 3 Video Recording Example
- SH7262/SH7264 Group Video Display Controller 3 How to Use the α (Alpha) Blending Window Function

1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

2. Applications

This application note shows the pin connection example and configuration example to display the still image by the VDC3. The specifications of the TFT-LCD panel used in this application note are shown in 2.2.

2.1 VDC3 Operation

The VDC3 provides the video display function to display the video, and the video recording function to record the video. This application note describes how to display the still image on the VDC3 as an example.

2.1.1 Overview

The VDC3 provides the following four functions. The function related to the still image display is the "function for outputting the control signals for the TFT-LCD panel". The video display function and video recording function cannot be used at the same time (These functions are not used in this application).

1. Video display function: Reduces the size of the input video, buffers the resultant video data in the memory, and then displays the video on the panel
2. Video recording function: Stores a specified number of fields of the input video in SDRAM
3. Function for overlaying graphic images (two planes) on the input video
4. Function for outputting the control signals for the TFT-LCD panel

2.1.2 Features

The following table lists the VDC3 features.

Table 1 VDC3 Features

Item	Function	Remarks
Operating frequency	Video input clock: 27 MHz Panel clock: 4 to 36 MHz (depends on the panel specifications)	For displaying the still image
Graphics images	Two planes (layers 1 and 2) RGB565 progressive format (α = none, R: 5 bits, G: 6 bits, B: 5 bits; 16 bits in total) αRGB4444 progressive format (α: 4 bits, R: 4 bits, G: 4 bits, B: 4 bits; 16 bits in total)	
Graphics functions	• α blending window function: Mixes the input video and layers 1 and 2 according to the transparency rate α in the specified region (fade-in and fade-out functions are available) • Chroma-keying function: Mixes the images with applying the specified RGB color according to the transparency rate α. • Dot α function: Mixes the images according to the transparency rate α when the target is a graphic image in α RGB4444 format. For each dot, the priority among the α values of the above functions is as follows: α blending window > chroma-keying > dot α	
Output video size (note)	640 pixels x 480 lines (VGA size) 480 pixels x 240 lines (WQVGA size) 320 pixels x 240 lines (QVGA size, landscape-mode) 240 pixels x 320 lines (QVGA size, portrait-mode)	
Output video format	RGB565 progressive video output (16-bit parallel output)	
Sync signal output	Outputs the control signals for the TFT-LCD panel	Other
Interrupt output	Line interrupt output (this can be output on a desired line) VSYNC cycle fluctuation detection signal for BT.601 and BT.656 Field write completion signal Overflow/underflow detection signal for the internal buffer	
Input video standard	8-bit input compliant to the ITU-R BT.656 standard (27 MHz) 8-bit serial input compliant to the ITU-R BT.601 standard (27 MHz)	
Video recording function	Stores the video data in the RGB565 format at a rate of the 1/2 field (NTSC: 30 fps; PAL: 25 fps)	
Video quality adjustment function	Contrast adjustment and brightness adjustment	
Video scaling processing	Vertical: x 1/2, x 1/3, x 1/4 Horizontal: x 2/3, x 1/2, x 1/3, x 1/4 Each scaled value can be further multiplied by 6/7 to support PAL.	

Note : The maximum viewable area for the input image is 480 pixels x 240 lines (NTSC), and 480 pixels x 288 lines (PAL).

2.1.3 I/O Pins

The following table lists the VDC3 I/O pins.

Table 2 VDC3 I/O Pins

Symbol	I/O	Pin Name	Description	Remarks
LCD_CLK	Output	Panel clock	Panel clock output pin	For displaying the still image
LCD_EXTCLK	Input	Panel clock source	Panel clock source input pin	
LCD_VSYNC	Output	Panel VSYNC output	Vertical sync signal output pin for the panel	
LCD_HSYNC	Output	Panel HSYNC output	Horizontal sync signal output pin for the panel	
LCD_DE	Output	Panel data enable output	Data enable signal or the data start position pulse signal output pin for the panel	
LCD_DATA15 to 0	Output	Panel data output	Data output pins for the panel MSB LSB MSB LSB [15:11] Red [4:0] [10:5] Green [5:0] [4:0] Blue [4:0]	
LCD_M_DISP	Output	Panel control signal	Alternating-signal for the panel	
DV_CLK	Input	Video input clock	Inputs the BT.601 or BT.656 clock	Other
DV_VSYNC	Input	VSYNC input	Inputs the BT.601 VSYNC signal	
DV_HSYNC	Input	HSYNC input	Inputs the BT.601 HSYNC signal	
DV_DATA7 to 0	Input	BT.601 or BT.656 input	Inputs the BT.601 or BT.656 data signal	

2.1.4 Configuration

Figure 1 shows the VDC3 block diagram. Refer to Table 3 for each block.

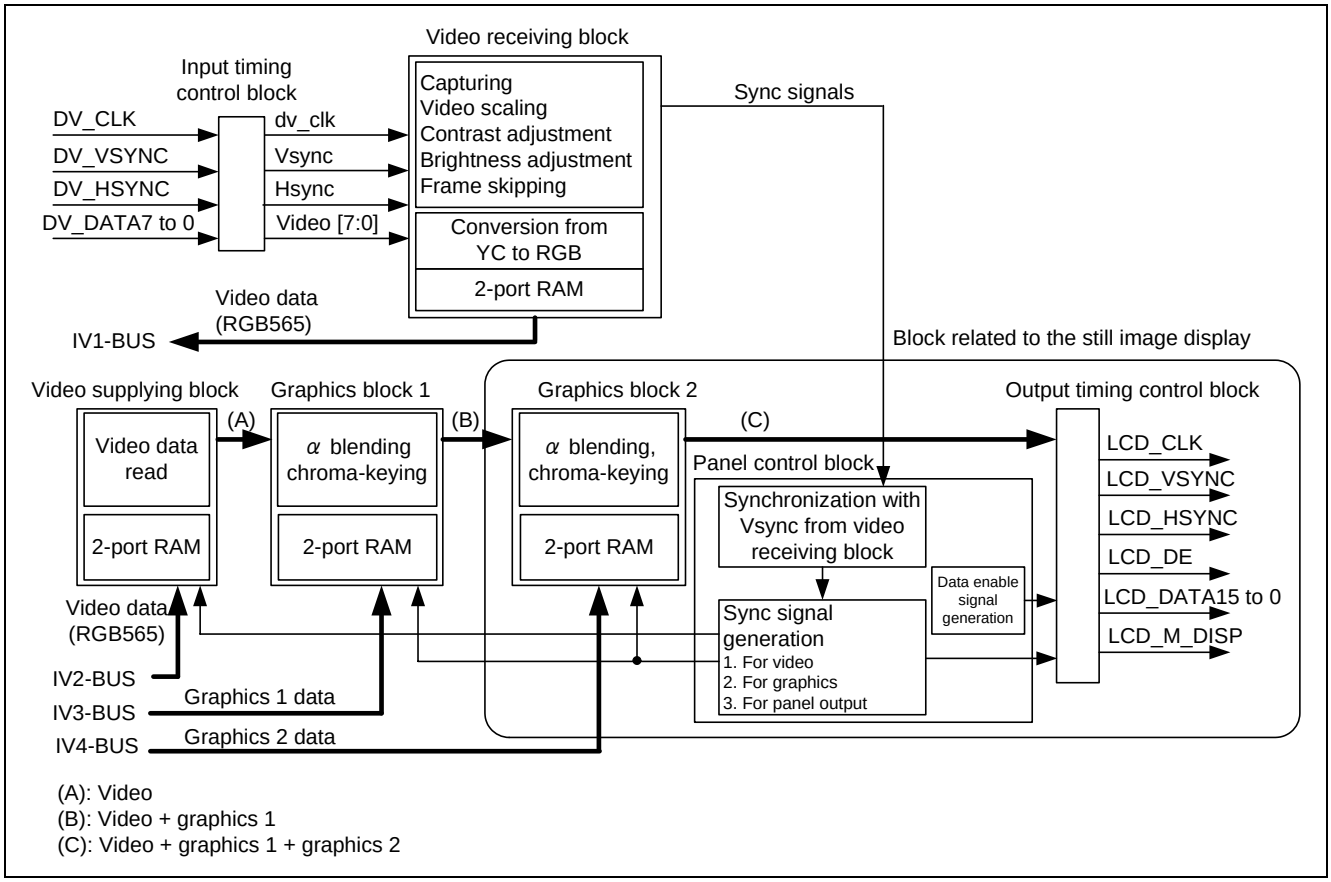


Figure 1 VDC3 Block Diagram

Table 3 VDC3 Functional Blocks

Block Name	Overview
Graphics block 1	Reads a graphics image (layer 1) from the memory via the IV3-BUS, overlays it on the video sent from the video supplying block, and outputs the result to graphics block 2.
Graphics block 2	Reads a graphics image (layer 2) from the memory via the IV4-BUS, overlays it on the output from graphics block 1, and outputs the result to the output timing control block.
Panel control block	Generates the sync signals to output to the panel
Output timing control block	Controls the timing of the output sync signal clock rising edge or falling edge, and the sync signal polarity. It also controls the timing of the RGB565 video output signals clock rising or falling edge.
Input timing control block	Controls the timing of the input sync signal clock rising edge or falling edge, and the sync polarity. It also controls the timing of the BT.601 and BT.656 video input signals clock rising or falling edge.
Video receiving block	(1) Captures the input video, scales, adjusts the contrast, and the brightness. (2) Converts the YC format to the RGB565 format, and stores the data via the IV1-BUS. (3) Skips the field, and stores the data in the RGB565 format via the IV1-BUS.
Video supplying block	Reads the video data via the IV2-BUS.

2.1.5 Still Image Display Example

The figure below shows the still image display example. To simplify the configuration, the video display, α control and the chroma-keying are not allowed in the following example.

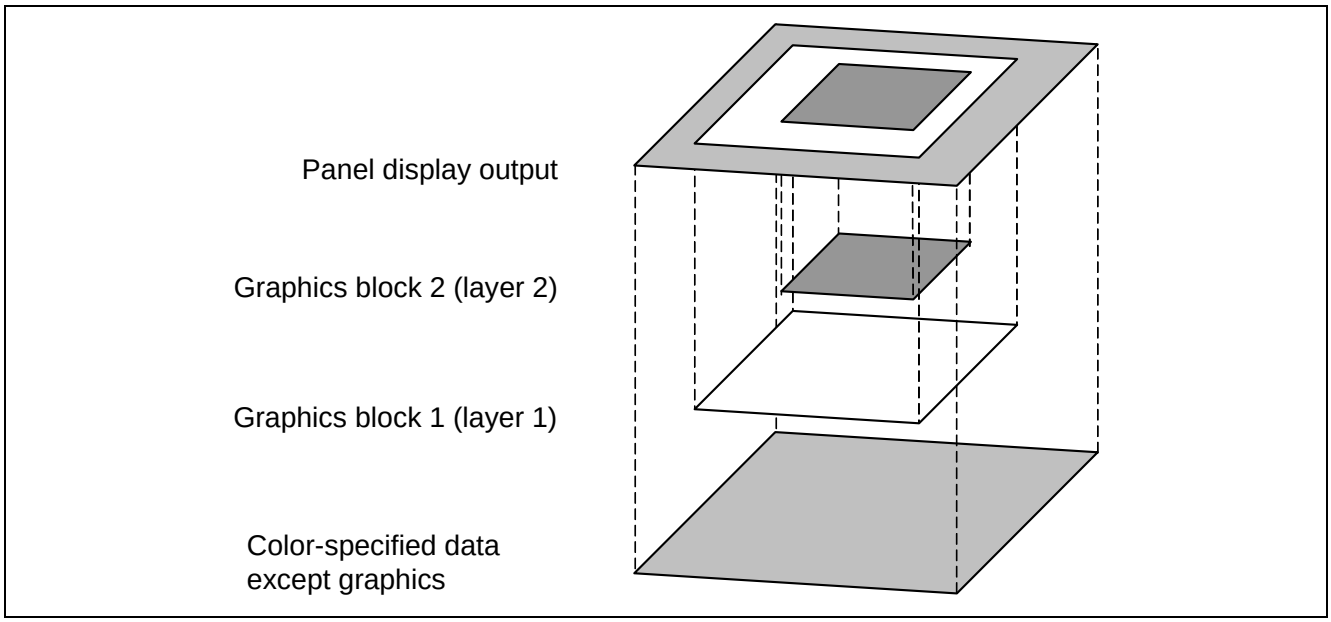


Figure 2 Still Image Display Example

2.1.6 Panel Control Signal Output Timing

Figure 3 shows the relationship between the panel control signal and displayed area. Figure 4 shows the signal output timing. Adjust the each signal polarity and timing by configuring the VDC3 registers. The bit names in the VDC3 registers are shown in the figures. Refer to Figure 5 VDC3 AC Characteristics and the TFT-LCD datasheet provided by manufacturer to configure the registers.

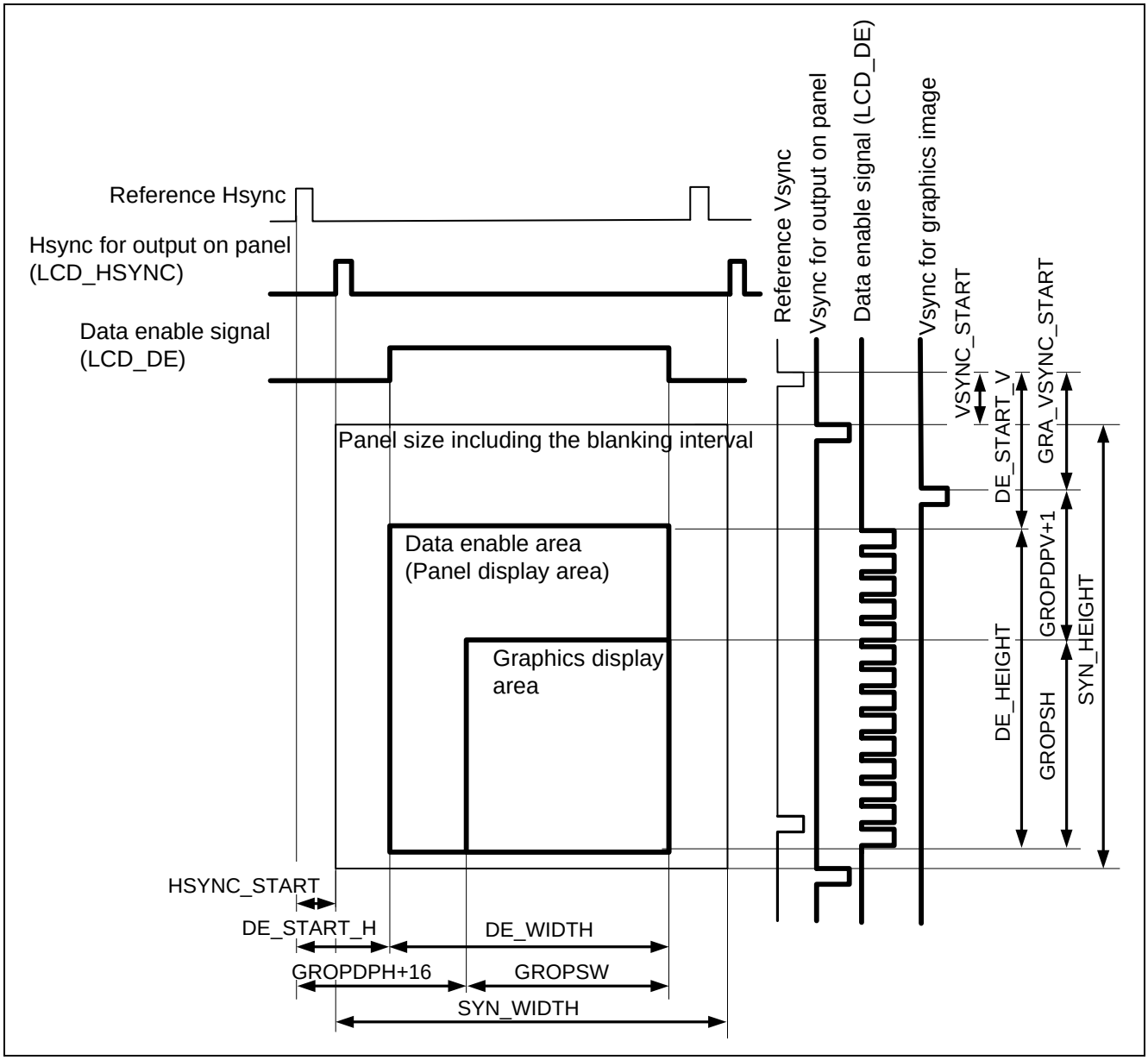
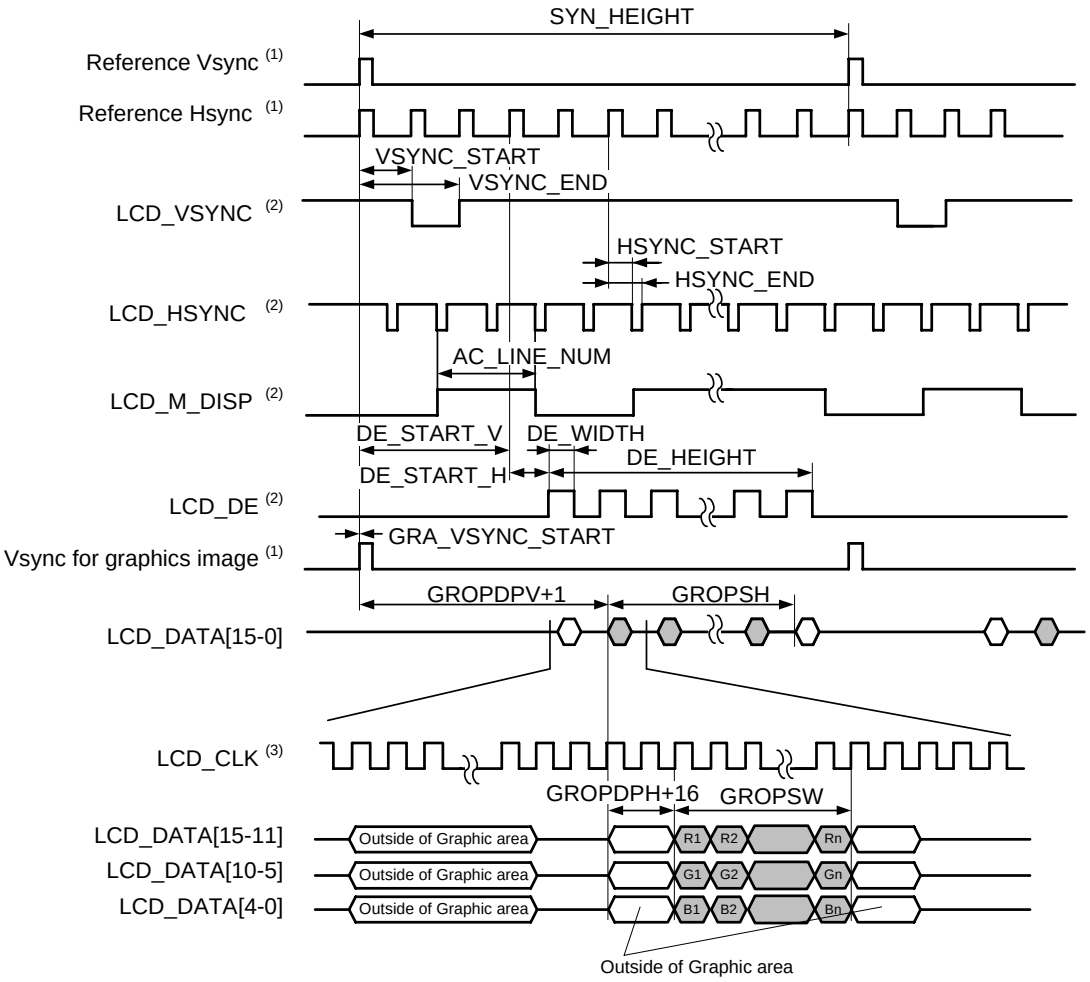


Figure 3 Relationship between the Panel Output Signal and Display Area



Note 1: Internal signal. Reference Vsync can select the free-running mode or synchronization with the Vsync of the video input by the SGMODE register.
Note 2: The polarity can be changed by the SYNCNT register.
Note 3: The signal polarity can be changed to the LCD_CLK rising edge or falling edge by the SYNCNT register.

Figure 4 Panel Control Signal Output Timing

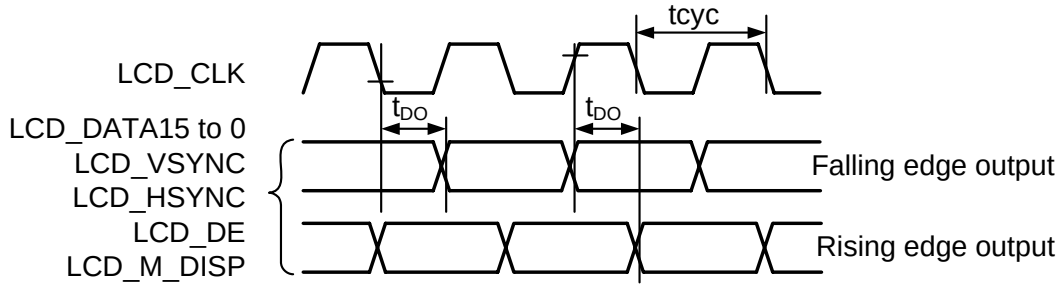


Figure 5 VDC3 AC Characteristics

2.2 TFT-LCD Panel Specifications

This section describes the specifications of the TFT-LCD panel (TX09D55VM1CDA, Hitachi Displays) used in this application. For details, refer to the datasheet provided by the manufacturer.

2.2.1 General Specifications

The following table lists the general specifications of the TFT-LCD panel used in this application.

Table 4 TFT-LCD Panel General Specifications

Item	Specifications
Resolution	QVGA in portrait-mode
Number of pixels	H 240 x V 320 (Number of dots: H (240 x 3) x V 320)
Pixel configuration	R, G, B vertical stripes
Number of colors	260,000 colors
Input signal	CMOS RGB (6 bits each digital)

2.2.2 Pin Functions

The following table lists the pin functions of the TFT-LCD panel used in this application.

Table 5 TFT-LCD Panel Pin Functions

Symbol	Description	Remarks
DCLK	Dot clock	
HSYNC	Horizontal sync signal	VSYNC (vertical sync signal) is not required.
DTMG	Display timing signal	Synchronizes with the vertical blanking interval inside the LCD panel.
R5 to R0	Red data signal (MSB: R5)	
G5 to G0	Green data signal (MSB: G5)	
B5 to B0	Blue data signal (MSB: B5)	
PCI	Power control signal	Pull up this pin by a resistor of less than or equal to 1 KΩ at 3.3 V, or do not connect.
Vctrl	Backlight control signal	Switches the backlight ON or OFF, and adjusts the brightness.

2.2.3 Interface Timing

The figure below shows the interface timing of the TFT-LCD panel used in this application. Table 6 lists the timing characteristics.

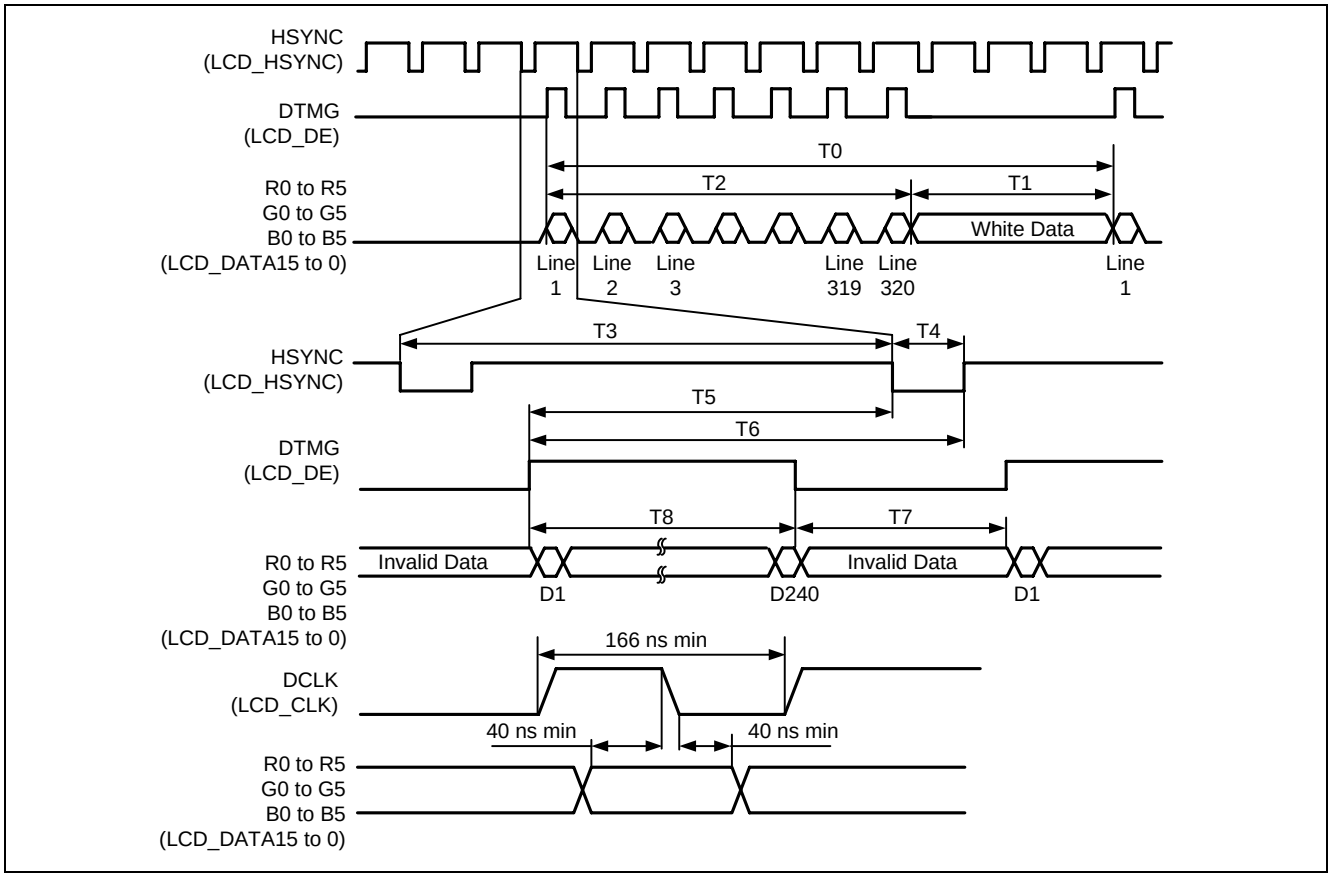


Figure 6 TFT-LCD Panel Interface Timing Example

Table 6 TFT-LCD Panel Timing Characteristics

Item	Symbol	Minimum	Typical	Maximum	Unit
Total vertical	T0	-	327	-	Line
Vertical blanking interval	T1	5	7	-	Line
Vertical display enable interval	T2	-	320	-	Line
Total horizontal	T3	265	273	509	Pixel Clock
HSYNC width	T4	4	5	10	Pixel Clock
HSYNC start	T5	244	251	307	Pixel Clock
HSYNC end	T6	248	256	317	Pixel Clock
Horizontal blanking interval	T7	25	33	269	Pixel Clock
Horizontal display enable interval	T8	-	240	-	Pixel Clock
VSYNC frequency	fV	52	60	68	Hz
HSYNC frequency	fH	10.92	19.5	22.12	kHz
DCLK frequency	fCLK	4.62	5.33	6.04	MHz

2.3 TFT-LCD Panel Circuit Example

2.3.1 Pin Connection Example

The figure below shows the TFT-LCD panel hardware connection in this application.

A TFT-LCD panel (TX09D55VM1CDA) inputs the color data in RGB in 6-bit digital per color. As the SH7264 MCU outputs the data in the RGB565 format, R0 pin and B0 pin of the LCD panel are connected to the R1 pin and B1 pin, respectively.

SH7264 LCD_CLK pin (data clock signal) is connected to the TX09D55VM1CDA DCLK pin. As the SH7264 MCU Bφ generates the clock internally, LCD_EXTCLK pin is not used. LCD_DE pin and LCD_HSYNC pin are connected to the corresponding TFT-LCD panel pins, respectively. Configure the VDC3 registers to adjust the difference of the signal polarity. The TFT-LCD panel used in this application does not require the LCD_VSYNC pin and LCD_M_DISP pin. These pins are not connected in this application.

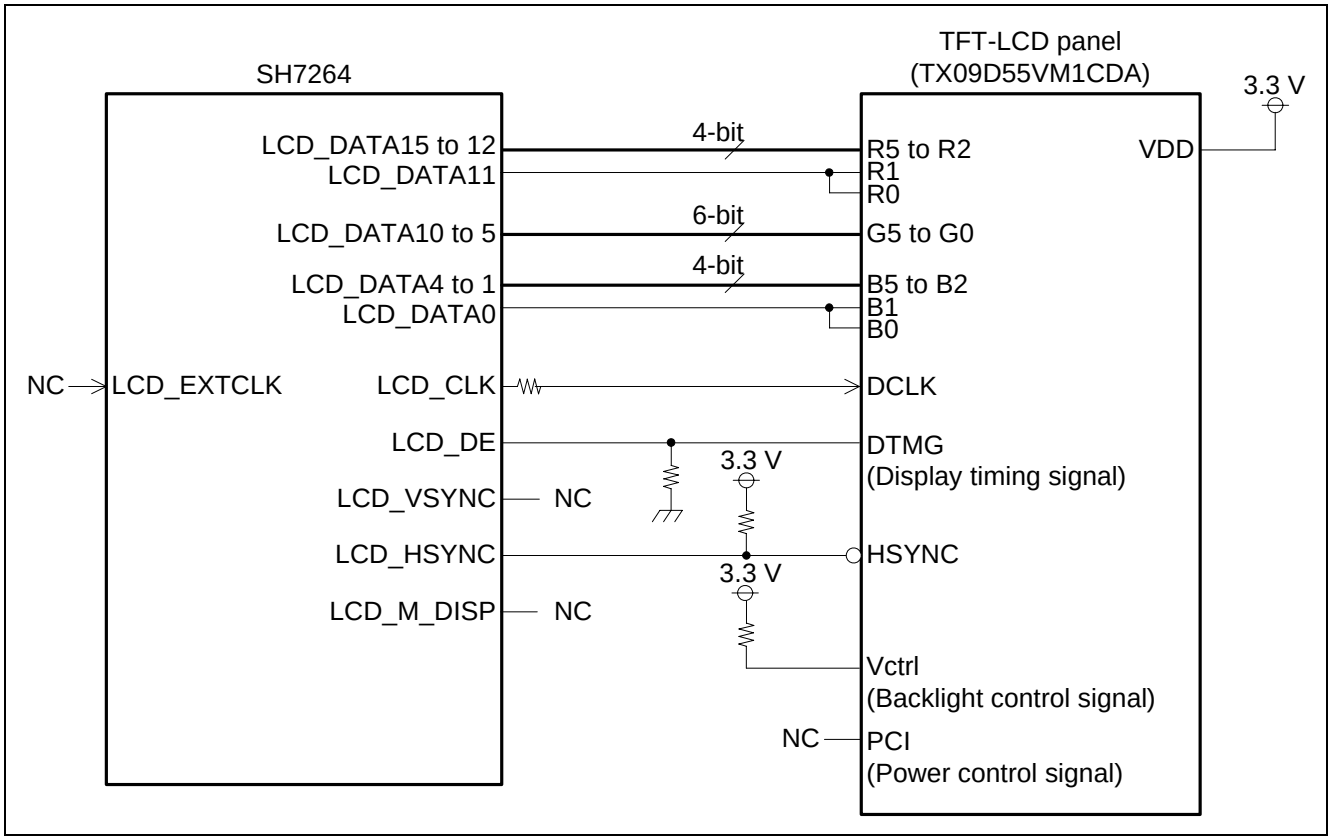


Figure 7 TFT-LCD Panel Hardware Connection

2.4 Sample Program Specifications

This section describes the specifications of the sample program and shows the flow chart of each processing.

2.4.1 Specifications

- Outputs the still image to the QVGA size (V 320 x H 240) TFT-LCD panel.
- Displays two planes; all dots in green and in blue. Two planes are switched back and forth.
- Still image appears in the center of the LCD panel with dimensions of 160 lines x 120 pixels, rectangular.
- Displays black in the blanking area.

2.4.2 Main Flow Chart of the Sample Program

Figure 8 shows the main flow chart of the sample program. The sample program initializes the VDC3 as shown in Figure 9 to Figure 11 to display the still image in the TFT-LCD panel. Then, the sample program repeatedly executes the processing shown in Figure 12 and switches between two still images.

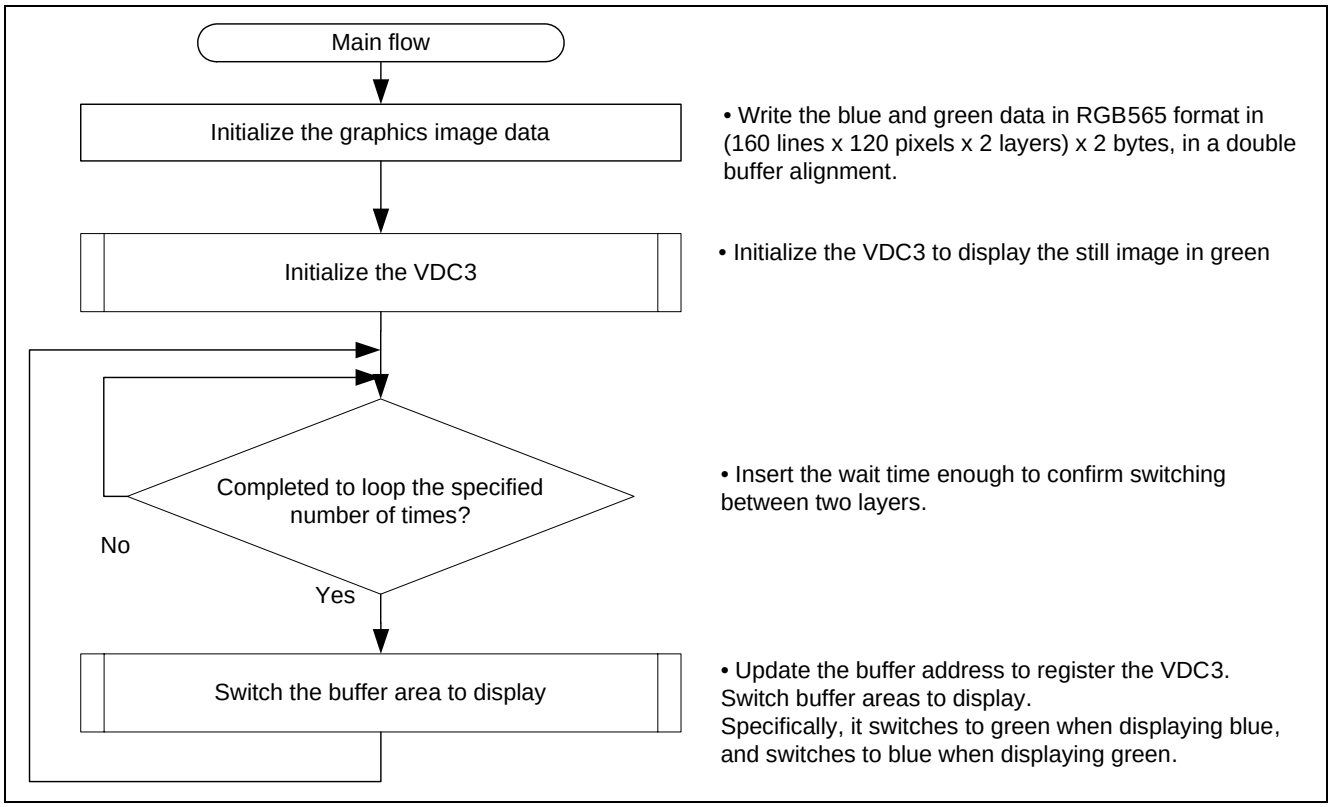


Figure 8 Sample Program Main Flow

2.4.3 Setting the Panel Control Signal Output

Figure 9 and Figure 10 shows the setting examples of the panel control signal output function. Follow these procedures in this section and in 2.4.4 Setting the Graphics Output to set the control signal output for the TFT-LCD panel. Values listed in Figure 9 and Figure 10 are set according to the TFT-LCD panel specifications described in section 2.2.

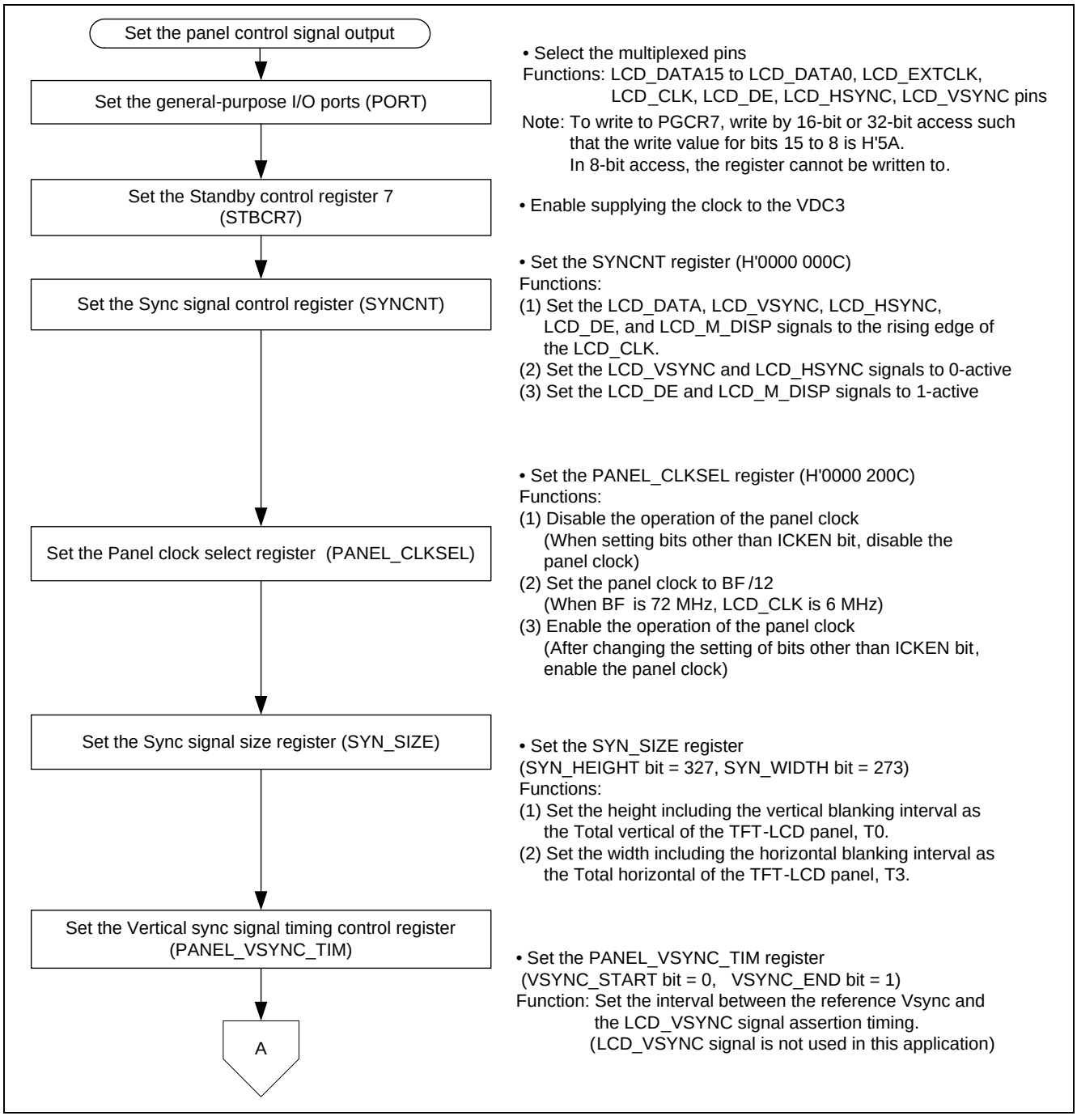


Figure 9 Panel Control Signal Output Setting Example (1/2)

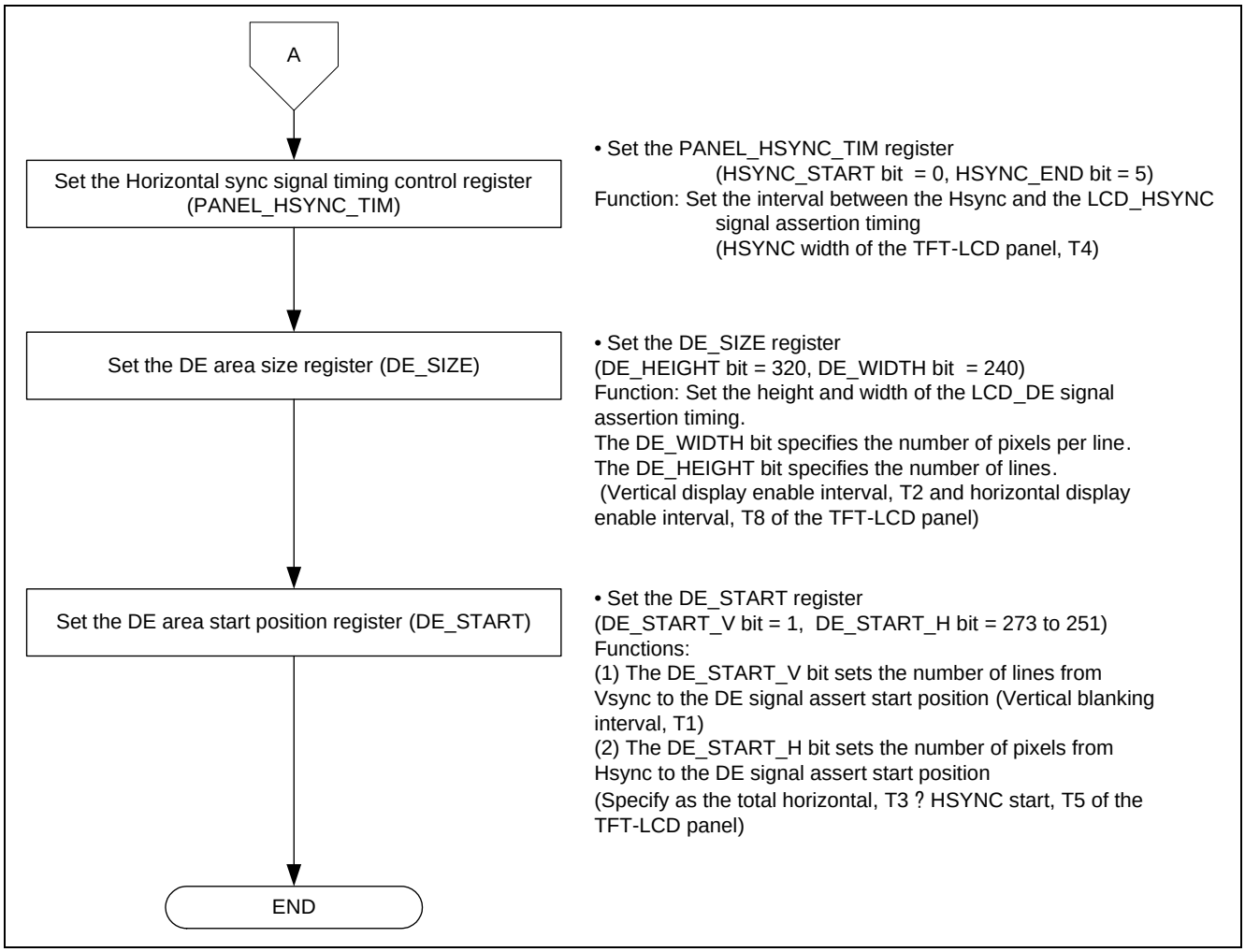


Figure 10 Panel Control Signal Output Setting Example (2/2)

2.4.4 Setting the Graphics Output

Figure 11 shows an example of outputting the graphics setting. Follow section 2.4.3 and this procedure to display the graphics image data in a specified area of the panel. The graphics block uses only layer 2 in this example.

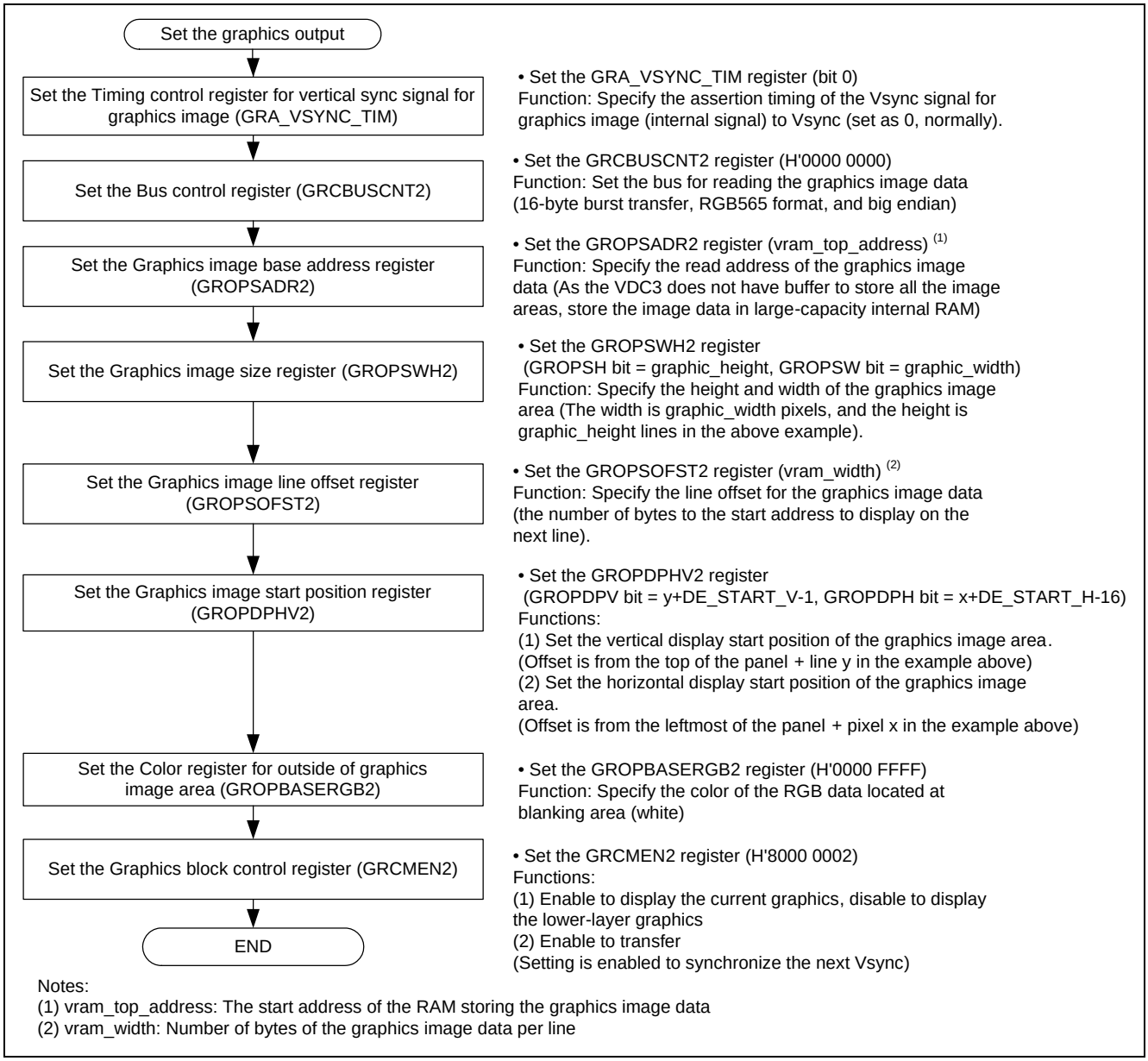


Figure 11 Graphics Output Setting Example

2.4.5 Updating the Graphics Image Data

Figure 12 shows the flow chart of updating the graphics image data.

To avoid the images distorted on the panel, the graphics image data area is configured with more than two planes. After updating the data area, update the Graphics image base address register of the VDC3 to switch the read address to show the image data. Then, use the GRCMEN register to transfer the value in the graphics image base address register for the change to effect.

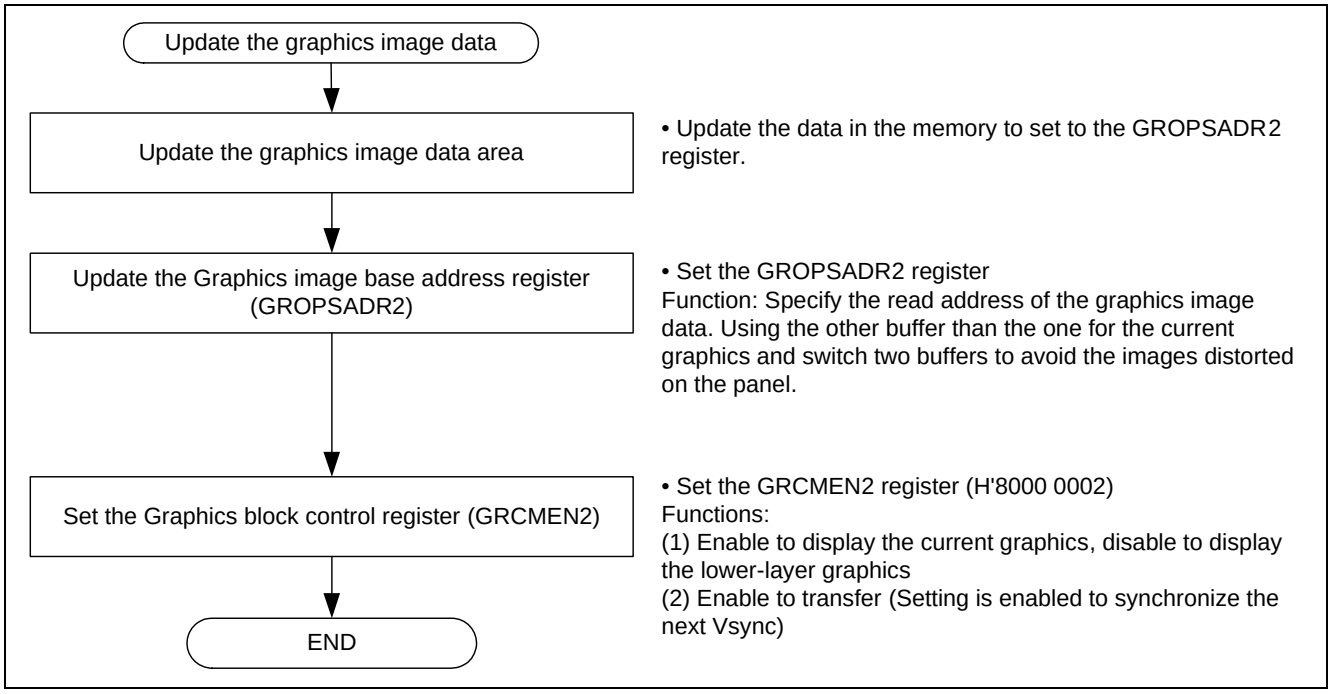


Figure 12 Graphics Image Data Update Example

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "main.c" (1/2)

```
1       /***********************************************************************
2       *   DISCLAIMER
3       *
4       *   This software is supplied by Renesas Electronics Corporation and is only
5       *   intended for use with Renesas products. No other uses are authorized.
6       *
7       *   This software is owned by Renesas Electronics Corporation and is protected under
8       *   all applicable laws, including copyright laws.
9       *
10      *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11      *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12      *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13      *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14      *   DISCLAIMED.
15      *
16      *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
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21      *
22      *   Renesas reserves the right, without notice, to make changes to this
23      *   software and to discontinue the availability of this software.
24      *   By using this software, you agree to the additional terms and
25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      ***********************************************************************/
28      /* Copyright (C) 2009(2010,2011) Renesas Electronics Corporation. All Rights Reserved.*/
29      /***********************************************************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : main.c
32      *   Abstract    : VDC3 TFT-LCD panel display example
33      *   Version     : 2.00.00
34      *   Device      : SH7264
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                               (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40      *   Description :
41      ***********************************************************************
42      *   History     : Dec.26,2008 Ver.1.00.00
43      *               : Jan.14,2010 Ver.1.01.00
44      *               : Feb.28,2011 Ver.2.00.00
45      ***********************************************************************/
46
47
```

3.3 Sample Program Listing "main.c" (2/2)

```
48    /***********************************************************************************
49    Includes  <System Includes> , "Project Includes"
50    ***********************************************************************************/
51    #include <stdio.h>
52    #include "io_vdc3_tft_panel.h"
53
54    /***********************************************************************************
55    Exported global variables and functions (to be accessed by other files)
56    ***********************************************************************************/
57    /* ==== Global functions ==== */
58    void main(void);
59
60    /***********************************************************************************
61     * ID           :
62     * Outline      : Still image display main
63     * Include      :
64     * Declaration  : void main(void);
65     * Description  : Switches two buffers in a certain period of time to display
66     *              : the still image on the TFT-LCD panel.
67     * Argument     : void
68     * Return Value : void
69     ***********************************************************************************/
70    void main(void)
71    {
72      int i, j, side;
73      volatile int w;
74
75      /* ==== Initializes the graphics image data ==== */
76      for( i = 0; i < GRPHCS2_Y_SIZE; i++){
77        for( j = 0 ; j < GRPHCS2_X_SIZE; j++){
78            grph_buffer2[0][i][j] = RGB565_GREEN;
79            grph_buffer2[1][i][j] = RGB565_BLUE;
80        }
81      }
82      /* ==== Initializes the VDC3 ==== */
83      io_vdc3_init();
84
85      /* ==== Updates the graphics image data ==== */
86      side = 0;
87      while(1){
88        for(w=10000000; w>0; w--){
89            /* wait */
90        }
91        /* ---- Switches the buffers ---- */
92        side ^= 0x1;
93        io_vdc3_change_buffer( 2, &grph_buffer2[side][0][0] );
94        }
95    }
96
97    /* End of File */
```

3.4 Sample Program Listing "io_vdc3_tft_panel.c" (1/7)

```
1    /***********************************************************************
2    *   DISCLAIMER
3    *
4    *   This software is supplied by Renesas Electronics Corporation and is only
5    *   intended for use with Renesas products. No other uses are authorized.
6    *
7    *   This software is owned by Renesas Electronics Corporation and is protected under
8    *   all applicable laws, including copyright laws.
9    *
10   *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11   *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12   *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13   *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
14   *   DISCLAIMED.
15   *
16   *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
17   *   ELECTRONICS CORPORATION NOR ANY OF ITS AFFILIATED COMPANIES SHALL BE LIABLE
18   *   FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES
19   *   FOR ANY REASON RELATED TO THIS SOFTWARE, EVEN IF RENESAS OR ITS
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21   *
22   *   Renesas reserves the right, without notice, to make changes to this
23   *   software and to discontinue the availability of this software.
24   *   By using this software, you agree to the additional terms and
25   *   conditions found by accessing the following link:
26   *   http://www.renesas.com/disclaimer
27   ***********************************************************************/
28   /*   Copyright (C) 2011 Renesas Electronics Corporation. All Rights Reserved.*/
29   /***********************************************************************
30   *   System Name : SH7264 Sample Program
31   *   File Name   : io_vdc3_tft_panel.c
32   *   Abstract    : VDC3 TFT-LCD panel display example
33   *   Version     : 1.00.00
34   *   Device      : SH7264
35   *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36   *               : C/C++ compiler package for the SuperH RISC engine family
37   *               :                              (Ver.9.03 Release00).
38   *   OS          : None
39   *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40   *   Description :
41   ***********************************************************************
42   *   History     : Feb.28,2011 Ver.1.00.00
43   ***********************************************************************/
44
45
```

3.5 Sample Program Listing " io_vdc3_tft_panel.c" (2/7)

```
46  /***********************************************************************
47  Includes  <System Includes> , "Project Includes"
48  ***********************************************************************/
49  #include "iodefine.h"
50  #include "io_vdc3_tft_panel.h"
51
52  /***********************************************************************
53  Exported global variables and functions (to be accessed by other files)
54  ***********************************************************************/
55  /* ==== Global functions ==== */
56  void io_vdc3_init(void);
57  void io_vdc3_change_buffer( int grphcs_no, unsigned short *buffer );
58
59  /* ==== Global variables ==== */
60  #pragma section GRPH2_BUFF /* Allocates the buffer at the 128-byte or 16-byte boundary
61                             in cache-disabled space */
62  unsigned short grph_buffer2[2][GRPHCS2_Y_SIZE][(GRPHCS2_LINE_OFFSET / BYTES_PER_PIXEL)];
63  #pragma section
64
65  /***********************************************************************
66  Private global variables and functions
67  ***********************************************************************/
68  /* ==== Private fuctions ==== */
69  static void io_vdc3_init_grphcs2(void);
70  static void io_vdc3_init_disp(void);
71  static void io_vdc3_start(void);
72
```

3.6 Sample Program Listing " io_vdc3_tft_panel.c " (3/7)

```
73    /***********************************************************************************
74     * ID           :
75     * Outline      : Initializes the VDC3
76     * Include      :
77     * Declaration  : void io_vdc3_init(void);
78     * Description  : Initializes the VDC3 to display the still image. Only layer 2
79     *              : in graphics block is used. Alpha-control or chroma-keying
80     *              : functions are not used. TFT-LCD panel TX09D55VM1CDA (Hitachi
81     *              : Displays) is used in this application.
82     * Argument     : void
83     * Return Value : void
84     ***********************************************************************************/
85    void io_vdc3_init(void)
86    {
87      int i, j;
88
89      /* ==== Initializes the data ==== */
90      /* ---- The graphics image 2 ---- */
91      for( i = 0; i < GRPHCS2_Y_SIZE; i++){
92        for( j = 0 ; j < GRPHCS2_X_SIZE; j++){
93            grph_buffer2[0][i][j] = RGB565_GREEN;
94            grph_buffer2[1][i][j] = RGB565_BLUE;
95        }
96      }
97      /* ==== PORT ==== */
98      /* ---- Display (out) ---- */
99      PORT.PGCR7.WORD = 0x5A01u;      /* LCD_DATA0 ( Bits 15 to 8 is H'5A. )*/
100     PORT.PGCR5.BIT.PG20MD= 1;       /* LCD_EXTCLK */
101     PORT.PGCR4.WORD = 0x1111u;      /* LCD_CLK, LCD_DE, LCD_HSYNC, LCD_VSYNC */
102     PORT.PGCR3.WORD = 0x1111u;      /* LCD_DATA15-12 */
103     PORT.PGCR2.WORD = 0x1111u;      /* LCD_DATA11-08 */
104     PORT.PGCR1.WORD = 0x1111u;      /* LCD_DATA07-04 */
105     PORT.PGCR0.BIT.PG3MD = 1;       /* LCD_DATA03 */
106     PORT.PGCR0.BIT.PG2MD = 1;       /* LCD_DATA02 */
107     PORT.PGCR0.BIT.PG1MD = 1;       /* LCD_DATA01 */
108
109     /* ==== CPG ==== */
110     CPG.STBCR7.BIT.MSTP74 = 0;      /* VDC3 */
111
112     /* ==== VDC3 ==== */
113     /* ---- Initializes the graphics block 2 ----  */
114     io_vdc3_init_grphcs2();
115
116     /* ---- Initializes the panel control block and output timing control block ---- */
117     io_vdc3_init_disp();
118
119     /* ---- Enables the operation ---- */
120     io_vdc3_start();
121   }
122
```

3.7 Sample Program Listing " io_vdc3_tft_panel.c " (4/7)

```
123  /***********************************************************************
124   * ID           :
125   * Outline      : Update the graphics image data
126   * Include      :
127   * Declaration  : void io_vdc3_change_buffer( int grphcs_no, unsigned short *buffer);
128   * Description  : Switches to another buffer specified by an argument to read the
129   *              : graphics image data. Update the image data before executing
130   *              : this function.
131   * Argument     : int grphcs_no ; I : Index number of the buffer to display
132   *              :                   : (1 : graphics 1, 2 : graphics 2)
133   *              : unsigned short * buffer ; I : buffer address
134   * Return Value : void
135   ***********************************************************************/
136  void io_vdc3_change_buffer( int grphcs_no, unsigned short *buffer )
137  {
138    if( grphcs_no == 1 ){
139      VDC3.GROPSADR1.LONG = (0x1FFFFFFFul & (unsigned long)buffer);
140      VDC3.GRCMEN1.BIT.WE = 1;      /* Transfers the graphics setting
141                                                 (Enabled from next Vsync) */
142    }
143    else{
144      VDC3.GROPSADR2.LONG = (0x1FFFFFFFul & (unsigned long)buffer);
145      VDC3.GRCMEN2.BIT.WE = 1;      /* Transfers the graphics setting
146                                                 (Enabled from next Vsync) */
147    }
148  }
149
```

3.8 Sample Program Listing " io_vdc3_tft_panel.c " (5/7)

```
150    /*****************************************************************************
151     * ID           :
152     * Outline      : Initializes the graphics block 2
153     * Include      : iodefine.h
154     * Declaration  : static void io_vdc3_init_grphcs2(void);
155     * Description  : Initializes the graphics block 2.
156     * Argument     : void
157     * Return Value : void
158     *****************************************************************************/
159    static void io_vdc3_init_grphcs2(void)
160    {
161      /* ---- Graphics output setting ---- */
162      VDC3.GRA_VSYNC_TIM.LONG = 0;           /* Sets the timing for
163                                                the graphics image VSYNC */
164      VDC3.GRCBUSCNT2.LONG = 0;              /* Sets the bus between the graphics
165                                                image data and the VDC3 */
166                                             /* (16-byte burst transfer,
167                                                RGB565 format, and big endian) */
168      VDC3.GROPSADR2.BIT.GROPSADR = (0x1FFFFFFFul & (unsigned long)grph_buffer2[0]);
169                                             /* Sets the start address of
170                                                the graphics image data */
171      VDC3.GROPSWH2.BIT.GROPSH = GRPHCS2_Y_SIZE; /* Number of lines for
172                                                the graphics image area */
173      VDC3.GROPSWH2.BIT.GROPSW = GRPHCS2_X_SIZE; /* Number of pixels for
174                                                the graphics image area */
175      VDC3.GROPSOFST2.BIT.GROPSOFST = GRPHCS2_LINE_OFFSET;
176                                             /* Sets the number of bytes per line */
177      VDC3.GROPDPHV2.BIT.GROPDPV = GRPHCS2_POS_Y + TFT_DE_START_V - 1;
178                                             /* Graphics image area start position in
179                                                the vertical direction */
180      VDC3.GROPDPHV2.BIT.GROPDPH = GRPHCS2_POS_X + TFT_DE_START_H -16;
181                                             /* Graphics image area start position in
182                                                the horizontal direction */
183      VDC3.GROPBASERGB2.LONG   = 0x00000000ul;    /* Specifies the color in the
184                                                blanking area (RGB565, black) */
185    }
186
```

3.9 Sample Program Listing " io_vdc3_tft_panel.c " (6/7)

```
187    /***********************************************************************************
188     * ID           :
189     * Outline      : Initializes the panel control block and output timing control block
190     * Include      : iodefine.h
191     * Declaration  : static void io_vdc3_init_disp(void);
192     * Description  : Initializes the panel control block and output timing control block.
193     * Argument     : void
194     * Return Value : void
195     ***********************************************************************************/
196    static void io_vdc3_init_disp(void)
197    {
198      /* ---- TFT-LCD panel control signal output setting ---- */
199      VDC3.SYNCNT.LONG = 0x0000000Cul;               /* Outputs all signals at the
200                                                        rising edge */
201                                                  /* LCD_VSYNC/LCD_HSYNC signal:
202                                                        output is inverted */
203      VDC3.PANEL_CLKSEL.BIT.ICKEN = 0;              /* Disables the operation of
204                                                        the panel clock */
205      VDC3.PANEL_CLKSEL.LONG      = 0x0000200Cul;   /* Clock source: Bφ (72 MHz) */
206                                                  /* Clock frequency: 6 MHz */
207      VDC3.PANEL_CLKSEL.BIT.ICKEN = 1;              /* Enables the operation of
208                                                        the panel clock */
209      VDC3.SYN_SIZE.BIT.SYN_HEIGHT= TFT_TOTAL_SZ_V; /* Number of lines including the
210                                                        vertical blanking interval */
211      VDC3.SYN_SIZE.BIT.SYN_WIDTH = TFT_TOTAL_SZ_H; /* Number of pixels including the
212                                                        horizontal blanking interval */
213      VDC3.PANEL_VSYNC_TIM.LONG   = TFT_VSYNC_WDTH; /* Sets the timing for the
214                                                        panel output VSYNC */
215      VDC3.PANEL_HSYNC_TIM.LONG   = TFT_HSYNC_WDTH; /* Sets the timing for the
216                                                        panel output HSYNC */
217      VDC3.DE_SIZE.BIT.DE_HEIGHT  = TFT_DISP_SZ_V;  /* Number of lines for the DE area */
218      VDC3.DE_SIZE.BIT.DE_WIDTH   = TFT_DISP_SZ_H;  /* Number of pixels for the DE area */
219      VDC3.DE_START.BIT.DE_START_V= TFT_DE_START_V; /* DE area start position in
220                                                        the vertical direction */
221      VDC3.DE_START.BIT.DE_START_H= TFT_DE_START_H; /* DE area start position in
222                                                        the horizontal direction */
223    }
224
```

3.10 Sample Program Listing " io_vdc3_tft_panel.c " (7/7)

```
225    /***********************************************************************************
226     * ID           :
227     * Outline      : Enables the operation
228     * Include      : iodefine.h
229     * Declaration  : static void io_vdc3_start(void);
230     * Description  : Enables the operation.(Enabled from the next Vsync)
231     * Argument     : void
232     * Return Value : void
233     ***********************************************************************************/
234    static void io_vdc3_start(void)
235    {
236      /*  ---- Enables the graphics block 2  ---- */
237      VDC3.GRCMEN2.LONG = 0x80000002ul;   /* Enables to display the current graphics,
238                                             disables to display the lower-layer graphics */
239
240    }
241    /* End of File */
242
```

3.11 Sample Program Listing "io_vdc3_tft_panel.h" (1/2)

```
1    /***********************************************************************
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3    *
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6    *
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25   *   conditions found by accessing the following link:
26   *   http://www.renesas.com/disclaimer
27   ***********************************************************************/
28   /*   Copyright (C) 2011 Renesas Electronics Corporation. All Rights Reserved.*/
29   /***********************************************************************
30   *   System Name : SH7264 Sample Program
31   *   File Name   : io_vdc3_tft_panel.h
32   *   Abstract    : VDC3 TFT-LCD panel display example
33   *   Version     : 1.00.00
34   *   Device      : SH7264
35   *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36   *               : C/C++ compiler package for the SuperH RISC engine family
37   *               :                              (Ver.9.03 Release00).
38   *   OS          : None
39   *   H/W Platform: M3A-HS64G50(CPU board), M3A-HS64G02(Option board)
40   *   Description :
41   ************************************************************************
42   *   History     : Feb.28,2011 Ver.1.00.00
43   ************************************************************************/
44
45
```

3.12 Sample Program Listing "io_vdc3_tft_panel.h" (1/2)

```
46  /***********************************************************************
47  Macro definitions
48  ***********************************************************************/
49  #define BYTES_PER_PIXEL           2       /* Number of bytes per pixel */
50  #define RGB565_BLACK          0x0000u /* Black */
51  #define RGB565_WHITE          0xFFFFu /* White */
52  #define RGB565_GREEN          0x07E0u /* Green */
53  #define RGB565_BLUE               0x001Fu /* Blue */
54
55  /* ---- Graphics image parameters ---- */
56  #define GRPHCS2_Y_SIZE        160     /* Height of Graphics image 2 */
57  #define GRPHCS2_X_SIZE        120     /* Width of Graphics image 2 */
58  #define GRPHCS2_LINE_OFFSET       (((GRPHCS2_X_SIZE * BYTES_PER_PIXEL) + 15 ) & 0xFFFFFFF0ul)
59                                    /* Line offset of Graphics image 2 */
60  #define GRPHCS2_POS_Y         80      /* Vertical display start position
61                                         (0: top of the panel) */
62  #define GRPHCS2_POS_X         60      /* Horizontal display start position
63                                         (0: leftmost of the panel) */
64
65  /* ---- TFT-LCD panel parameters ---- */
66  #define TFT_TOTAL_SZ_V        327     /* Number of lines including the vertical
67                                        blanking interval */
68  #define TFT_TOTAL_SZ_H        273     /* Number of pixels including the horizontal
69                                        blanking interval */
70  #define TFT_DISP_SZ_V         320     /* Vertical display enable interval */
71  #define TFT_DISP_SZ_H         240     /* Horizontal display enable interval */
72  #define TFT_VSYNC_WDTH        1       /* LCD_VSYNC pulse width (number of lines) */
73  #define TFT_HSYNC_WDTH        5       /* LCD_HSYNC pulse width (number of pixels) */
74  #define TFT_DE_START_V        1       /* Number of lines between the reference Vsync
75                                        and the enable interval */
76  #define TFT_DE_START_H        (TFT_TOTAL_SZ_H - 251)
77                                    /* Number of pixels between the reference
78                                        Hsync and the enable interval */
79
80  /***********************************************************************
81  Imported global variables and functions (from other files)
82  ***********************************************************************/
83  /* ==== Global functions ==== */
84  extern void io_vdc3_init(void);
85  extern void io_vdc3_change_buffer( int grphcs_no, unsigned short *buffer );
86
87  /* ==== Global variables ==== */
88  extern unsigned short grph_buffer2[2][GRPHCS2_Y_SIZE][(GRPHCS2_LINE_OFFSET/BYTES_PER_PIXEL)];
89
90  /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev.3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware manual Rev.2.00
  The latest version of the hardware manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.14.09	—	First edition issued
1.01	Jan.19.10	14	Figure 9, Note added
		18	Supplement to the sample program added for 640-KB RAM
		24	Writing procedure to the PGCR7 updated
		19 to 26	Format for header comments updated
1.02	Mar.23.11	13 to 29	Changed the configuration of the source code

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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