SH7216 Group

SCI (Clock Synchronous) Data Transfer Using DTC

REJ06B0985-0101
Rev.1.01
Jun 25, 2010

Introduction

This application note presents an overview of using the data transfer controller (DTC) and serial communication interface (SCI) of the SH7216 to perform clock synchronous serial data transfer.

Note that although the sample tasks and applications presented in this application note have been verified to work as intended, they should be checked in the actual operating environment before being put into actual use.

Target Device

SH7216

Contents

1. Introduction

1.1 Specifications

The sample program performs serial transmission and reception by using the DTC to transfer data between the serial communication interface (SCI) and the on-chip RAM.

- SCI channel 1 is used.
- The communication format is 8-bit fixed data.
- For transmission, the DTC is activated by a transmit data empty interrupt request and transfers data from the on-chip flash memory to the transmit data register (SCTDR).
- For reception, the DTC is activated by a receive data full interrupt request and transfers the received data to the on-chip RAM.
- Operation stops when transmission or reception of 32 bytes of data has completed.

1.2 Functions Used

- Serial communication interface (SCI), channel 1
- Data transfer controller (DTC)

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.06.00
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.03.00, Release 00
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu –pic=1 –object="$(CONFIGDIR)¥$(FILELEAF).obj" -debug -gbr=auto –chgincpath –errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

2. Description of Sample Application

The sample application uses the transmit data empty interrupt (TXI) and receive data full interrupt (RXI) of the SCI as activation sources for the DTC. It performs clock synchronous serial data transmission and reception, using the normal transfer mode to transfer data.

2.1 Operation of Functions Used

2.1.1 Serial Communication Interface (SCI)

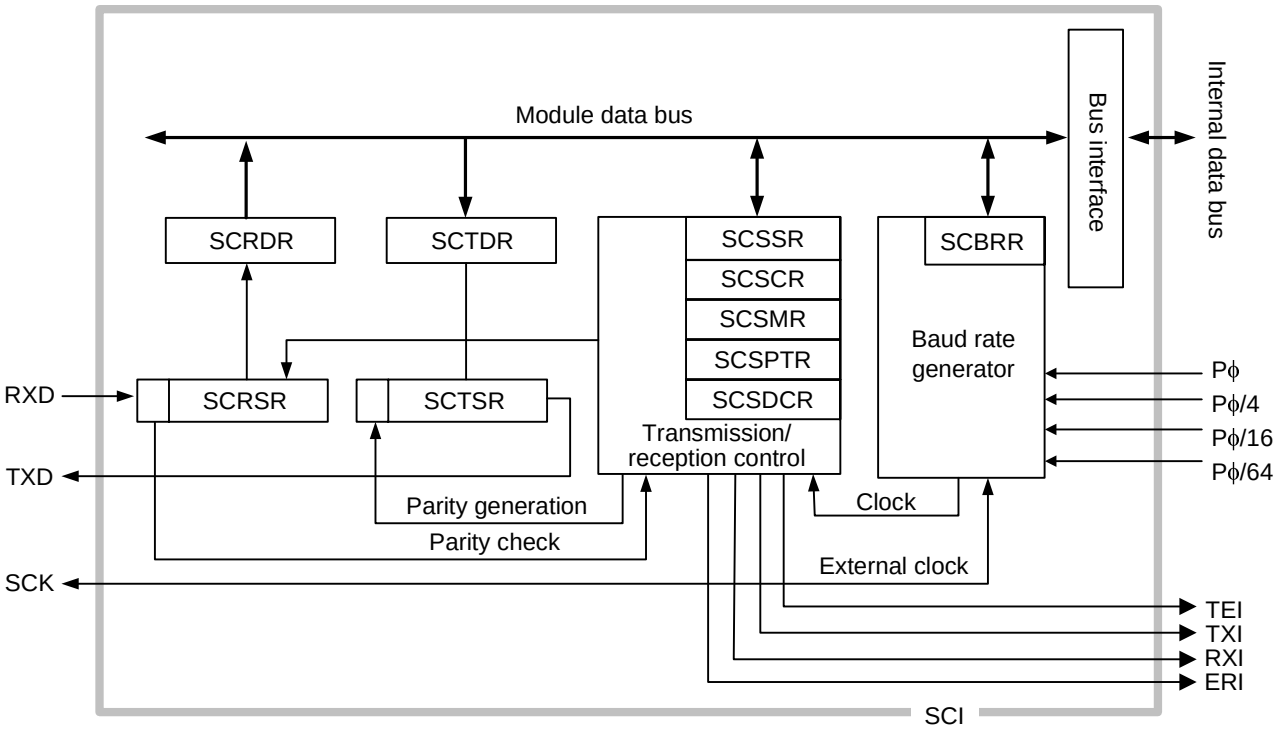
In clock synchronous mode data is transmitted or received in synchronization with a clock pulse, enabling high-speed serial communication. Either an internal clock or an external clock input to the SCK pin may be selected as the clock source. When an internal clock is selected, the sync clock is output from the SCK pin. When an external clock is selected, the sync clock is input to the SCK pin. The transmit and receive blocks in the SCI are independent, and full-duplex communication is supported by using a common clock. In addition, the transmit and receive blocks each have a double-buffered structure, enabling high-speed continuous transmission or reception of serial data. In clock synchronous serial communication, data is output on the communication line from one falling edge of the sync clock to the next. Data is guaranteed valid at the rising edge of the sync clock. In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB.

For details of the SCI, see the Serial Communication Interface (SCI) section in the *SH7216 Group Hardware Manual*.

Table 1 shows an outline of clock synchronous communication. Figure 1 is a block diagram of the SCI.

Table 1 Outline of Clock Synchronous Communication

Item	Description
Channels	4 channels (SCI_0, SCI_1, SCI_2, SCI_4)
Clock source	Internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) External clock: SCK pin clock input
Data format	Transfer data length: 8 bits, fixed Data sequence: Selectable between LSB-first and MSB-first
Baud rate	When internal clock selected: 1 kbps to 500 kbps (Pϕ = 40 MHz operation) When external clock selected: Max. 8,333,333.3 bps (Pϕ = 50 MHz, external clock input = 8.3333 MHz)
Error detection	Overrun error
Interrupt requests	Transmit data empty interrupt (TXI) Receive data full interrupt (RXI) Receive error interrupt (ERI) Transmit end interrupt (TEI)
Clock source	Selectable between internal clock and external clock • When internal clock selected: The SCI operates using the baud rate generator clock, and the sync clock can be output to the outside. • When external clock selected: The internal baud rate generator is not used, and the SCI operates using the input clock.



Legend:
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 1 SCI Block Diagram

2.1.2 Data Transfer Controller (DTC)

Three transfer modes are supported: normal, repeat, and block. Data transfer can be performed using a number of channels specified by the user by storing transfer information in the data area. When the DTC is activated, it reads the transfer information from the data area, performs the data transfer, and then writes back the transfer information after the data transfer completes.

The transfer information is allocated in the data area.

For details of the DTC, see the Data Transfer Controller (DTC) section in the *SH7216 Group Hardware Manual* (rej09b0543).

Table 2 shows an overview of the DTC, and figure 2 is a block diagram of the DTC.

Table 2 DTC Overview

Item	Description
Transfer modes	Normal transfer mode, repeat transfer mode, block transfer mode
Transfer count	Normal transfer mode: 1 to 65,536 Repeat transfer mode: 1 to 256 Block transfer mode: 1 to 65,536
Data size	Selectable among byte, word, and longword
CPU interrupt requests	An interrupt request can be sent to the CPU after a single data transfer completes. An interrupt request can be sent to the CPU after the specified number of data transfers complete.
Activation sources	External pin, A/D, CMT, USB, MTU2, MTU2S, IIC3, SSU, SCI, SCIF
Other	Support for chain transfer (multiple data transfers triggered by a single activation source) Transfer information read skip mode setting Module stop mode setting Short address mode setting Selectable among three bus release timing settings Selectable among two DTC activation priority settings

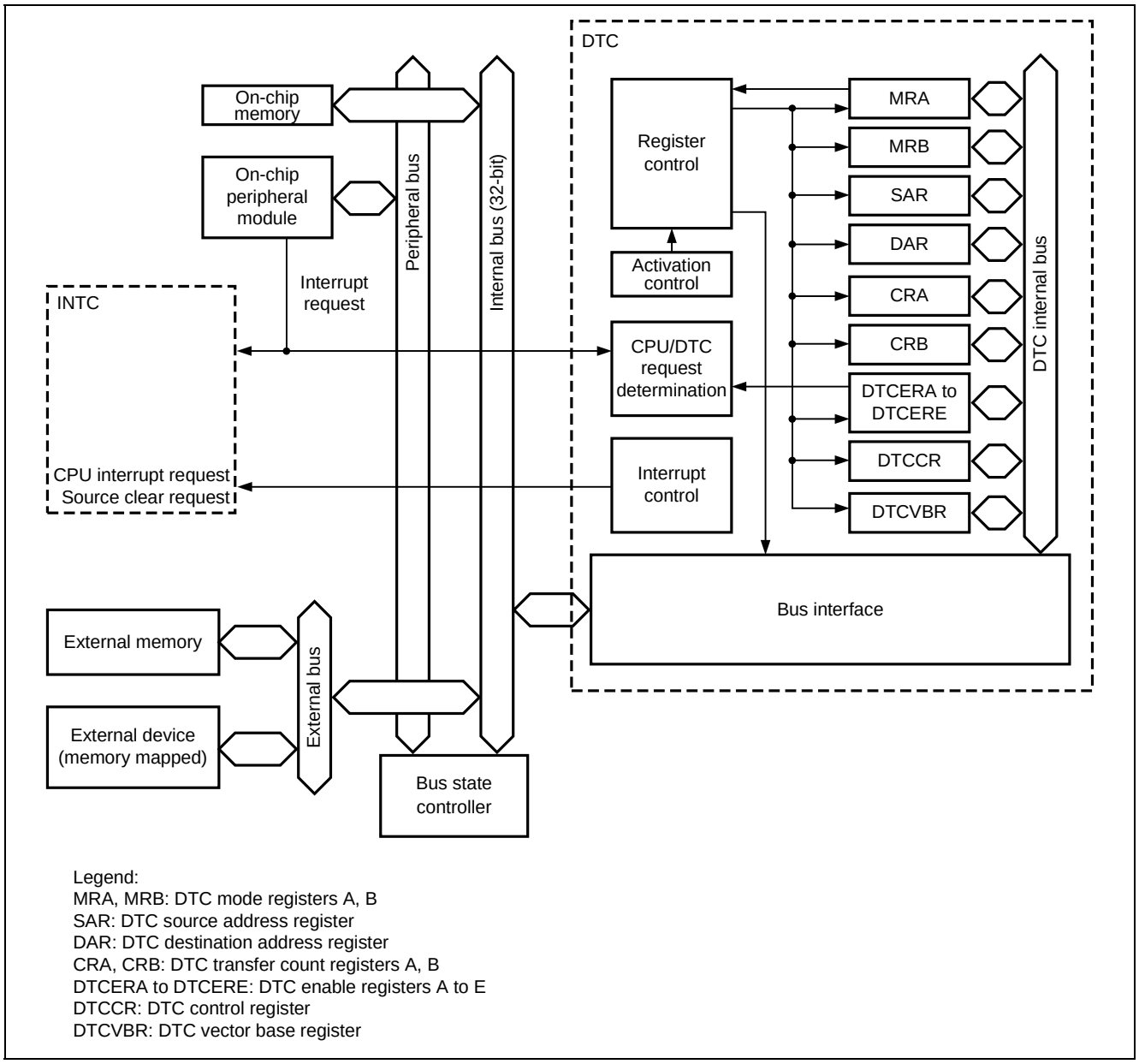


Figure 2 DTC Block Diagram

(a) DTC Transfer Information Allocation

The transfer information is allocated within the data area. Use 4n as the transfer information start address. When an address other than 4n is specified, the bottom two bits are ignored when accessing the data area ([1:0] = B'00). Figure 3 illustrates the allocation of transfer information in the data area. Exclusively in cases when all transfer sources and transfer destinations for DTC transfers are located in the on-chip RAM and on-chip peripheral modules, the short address mode may be selected by setting to 1 the DTSA bit in the bus function extending register (BSCEHR).*[1]

Note: 1. See 9.4.8 Bus Function Extending Register (BSCEHR) in the Bus State Controller (BSC) section in the *SH7216 Group Hardware Manual* (rej09b0543).

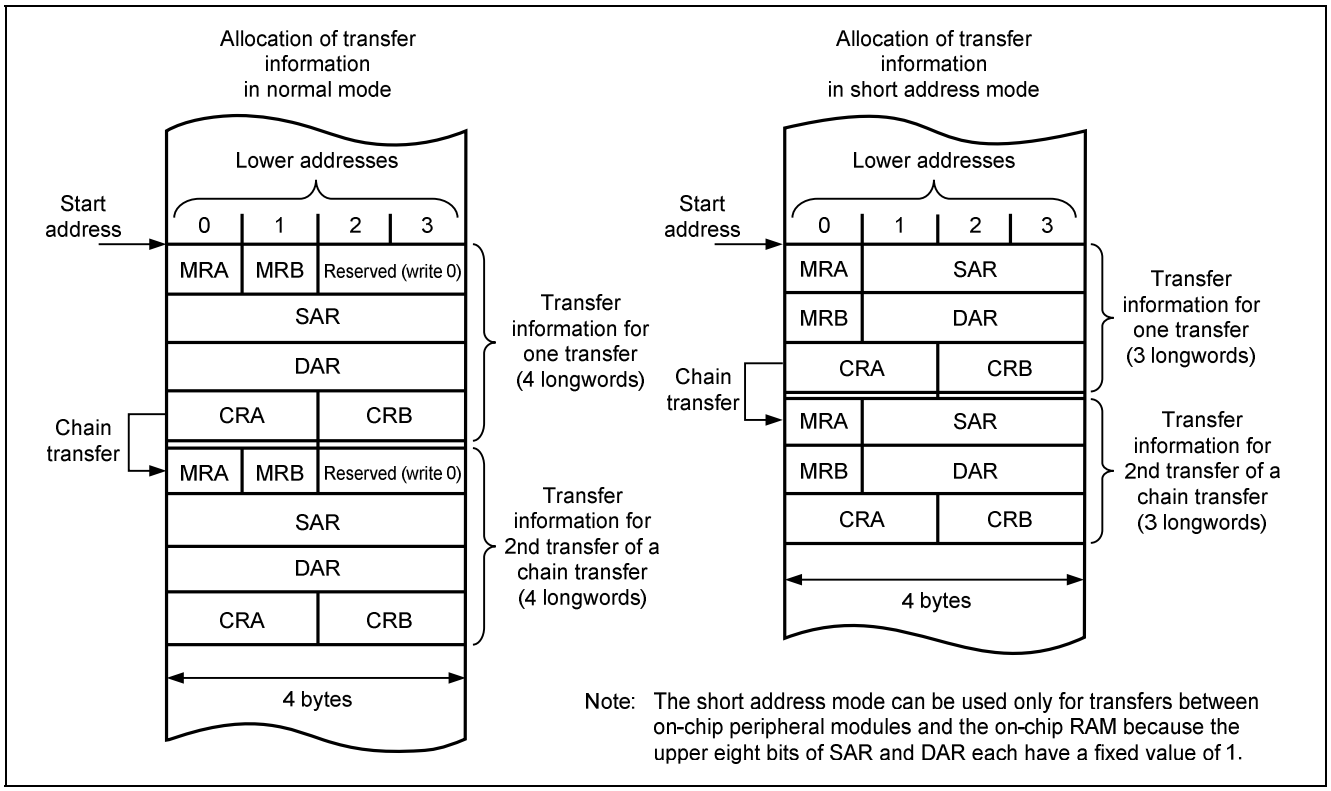


Figure 3 Allocation of Transfer Information in Data Area

(b) DTC Vector Table Allocation

- The DTC vector table is allocated in the RAM, so the address to be used as the vector base is set in the DTC vector base address register (DTCVBR).
- The start address of the transfer information is stored at the address pointed to by the DTC vector address offset.

For each activation source, the DTC reads the transfer information start address from the vector table and then reads the transfer information at that start address.

Figure 4 shows the correspondence between the DTC vector table and transfer information.

Table 3 lists the correspondences between the interrupt sources, DTC vector addresses, and DTCE Bits.

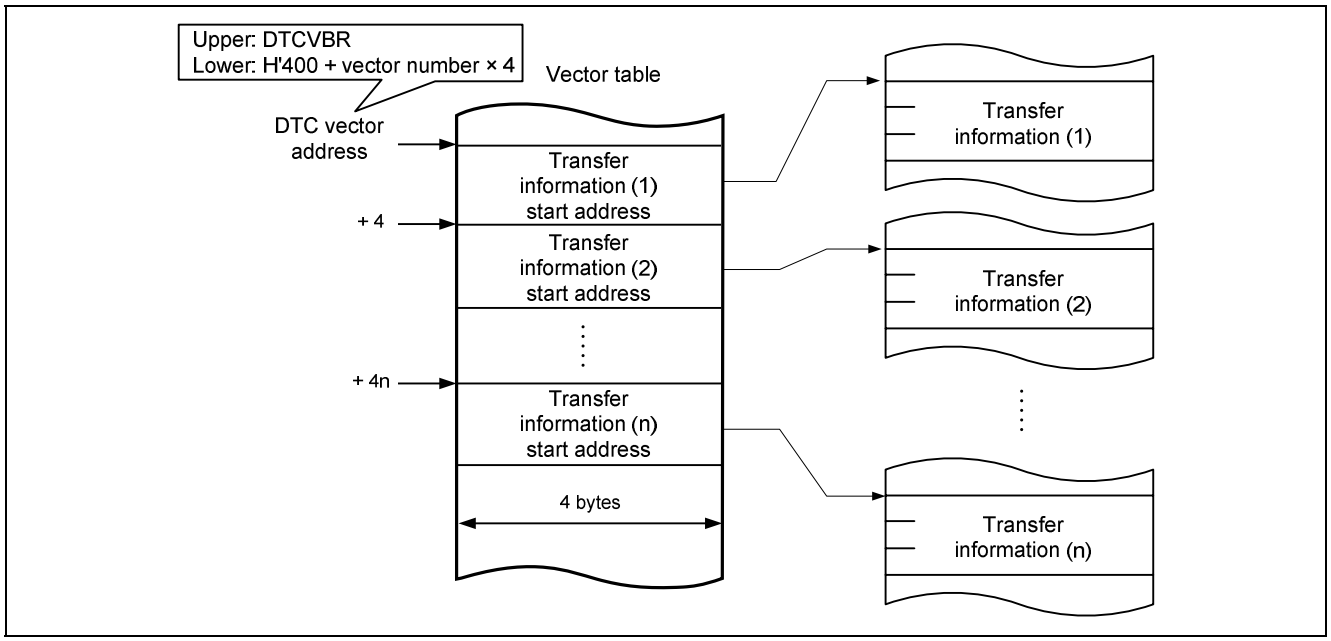


Figure 4 Correspondences between DTC Vector Table and Transfer Information

Table 3 Correspondences between Interrupt Sources, DTC Vector Addresses, and DTCE Bits

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*[1]
External pin	IRQ0	64	H'00000500	DTCERA15
	IRQ1	65	H'00000504	DTCERA14
	IRQ2	66	H'00000508	DTCERA13
	IRQ3	67	H'0000050C	DTCERA12
	IRQ4	68	H'00000510	DTCERA11
	IRQ5	69	H'00000514	DTCERA10
	IRQ6	70	H'00000518	DTCERA9
	IRQ7	71	H'0000051C	DTCERA8
A/D	ADI0	92	H'00000570	DTCERA7
	ADI1	96	H'00000580	DTCERA6
RCAN-ET	RM0_0	106	H'000005A8	DTCERA4
CMT	CMI0	140	H'00000630	DTCERA3
	CMI1	144	H'00000640	DTCERA2
USB	USBRXI1	150	H'00000658	DTCERE7
	USBTXI1	151	H'0000065C	DTCERE6
	USBRXI0	154	H'00000668	DTCERA1
	USBTXI0	155	H'0000066C	DTCERA0
MTU2_CH0	TGIA_0	156	H'00000670	DTCERB15
	TGIB_0	157	H'00000674	DTCERB14
	TGIC_0	158	H'00000678	DTCERB13
	TGID_0	159	H'0000067C	DTCERB12
MTU2_CH1	TGIA_1	164	H'00000690	DTCERB11
	TGIB_1	165	H'00000694	DTCERB10
MTU2_CH2	TGIA_2	172	H'000006B0	DTCERB9
	TGIB_2	173	H'000006B4	DTCERB8
MTU2_CH3	TGIA_3	180	H'000006D0	DTCERB7
	TGIB_3	181	H'000006D4	DTCERB6
	TGIC_3	182	H'000006D8	DTCERB5
	TGID_3	183	H'000006DC	DTCERB4
MTU2_CH4	TGIA_4	188	H'000006F0	DTCERB3
	TGIB_4	189	H'000006F4	DTCERB2
	TGIC_4	190	H'000006F8	DTCERB1
	TGID_4	191	H'000006FC	DTCERB0
	TCIV_4	192	H'00000700	DTCERC15
MTU2_CH5	TGIU_5	196	H'00000710	DTCERC14
	TGIV_5	197	H'00000714	DTCERC13
	TGIW_5	198	H'00000718	DTCERC12
MTU2S_CH3	TGIA_3S	204	H'00000730	DTCERC3
	TGIB_3S	205	H'00000734	DTCERC2
	TGIC_3S	206	H'00000738	DTCERC1
	TGID_3S	207	H'0000073C	DTCERC0
MTU2S_CH4	TGIA_4S	212	H'00000750	DTCERD15
	TGIB_4S	213	H'00000754	DTCERD14
	TGIC_4S	214	H'00000758	DTCERD13
	TGID_4S	215	H'0000075C	DTCERD12
	TCIV_4S	216	H'00000760	DTCERD11

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*[1]
MTU2S_CH5	TGIU_5S	220	H'00000770	DTCERD10
	TGIV_5S	221	H'00000774	DTCERD9
	TGIW_5S	222	H'00000778	DTCERD8
IIC3	RXI	230	H'00000798	DTCERD7
	TXI	231	H'0000079C	DTCERD6
RSPI	SPRI	234	H'000007A8	DTCERD5
	SPTI	235	H'000007Ac	DTCERD4
SCI4	RXI4	237	H'000007B4	DTCERD3
	TXI4	238	H'000007B8	DTCERD2
SCI0	RXI0	241	H'000007C4	DTCERE15
	TXI0	242	H'000007C8	DTCERE14
SCI1	RXI1	245	H'000007D4	DTCERE13
	TXI1	246	H'000007D8	DTCERE12
SCI2	RXI2	249	H'000007E4	DTCERE11
	TXI2	250	H'000007E8	DTCERE10
SCIF3	RXI3	254	H'000007F8	DTCERE9
	TXI3	255	H'000007FC	DTCERE8

Note: 1. DTCE bits with no corresponding interrupt are reserved. Always write 0 to these bits.

2.2 Sample Program Operation

Table 4 lists the DTC transfer conditions and table 5 the SCI settings for the sample program.

Figure 5 shows a transfer information memory map and figure 6 illustrates transmit and receive operation.

Table 4 DTC Transfer Conditions

Condition	SCI Transmit Side DTC Transfer Condition (TXI1)	SCI Receive Side DTC Transfer Condition (RXI1)
Transfer mode	Normal mode	Normal mode
Transfer count	32	32
Transfer size	Byte	Byte
DTC vector table	Allocated at H'FFF90000 (on-chip RAM)	Allocated at H'FFF90000 (on-chip RAM)
Transfer source	On-chip RAM	Receive data register (SCRDR_1)
Transfer destination	Transmit data register (SCTDR_1)	On-chip RAM
Transfer source addressing mode	SAR incremented after transfer	SAR fixed after transfer
Transfer destination addressing mode	DAR fixed after transfer	DAR incremented after transfer
Activation source	TXI1 of SCI1	RXI1 of SCI1
Interrupt handling	Interrupt to CPU after specified number of data transfers complete enabled	Interrupt to CPU after specified number of data transfers complete enabled

Table 5 SCI Settings

Channel	CH1
Communication mode	Clock synchronous mode
Interrupts	Transmit data empty interrupt (TXI) Receive data full interrupt (RXI), receive error interrupt (ERI)
Communication speed	100 kbps (Pϕ = 50 MHz)
Data length	8-bit data (fixed)
Stop bits	1 stop bit
Sync clock	Internal clock/ SCK pin sync clock output
Bit order	LSB-first transmission

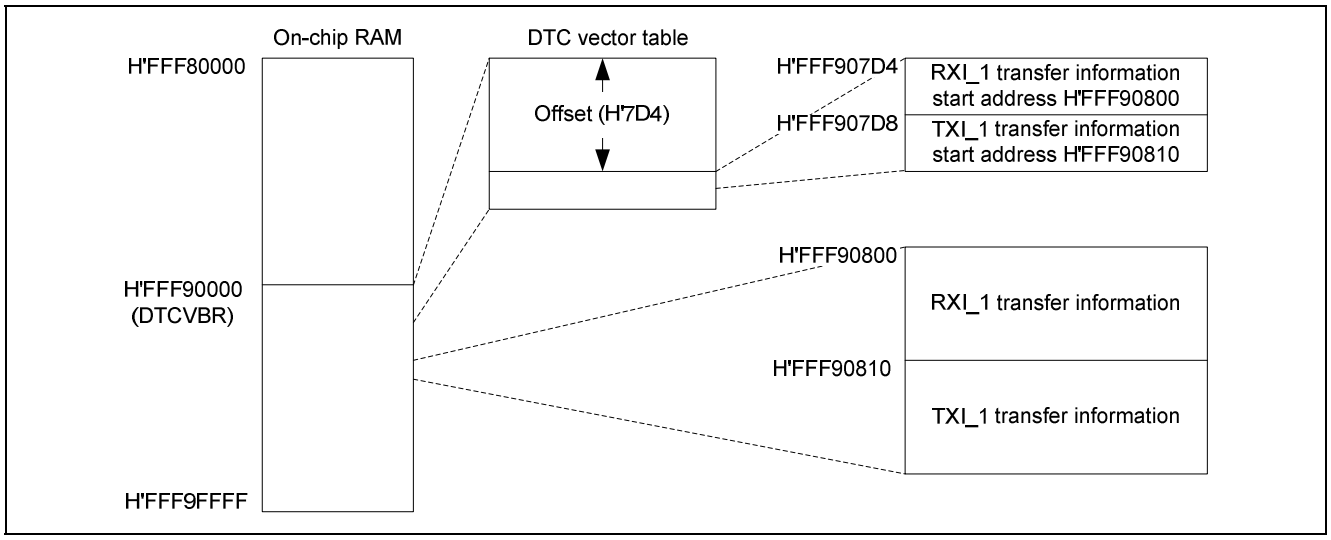


Figure 5 Transfer Information Memory Map

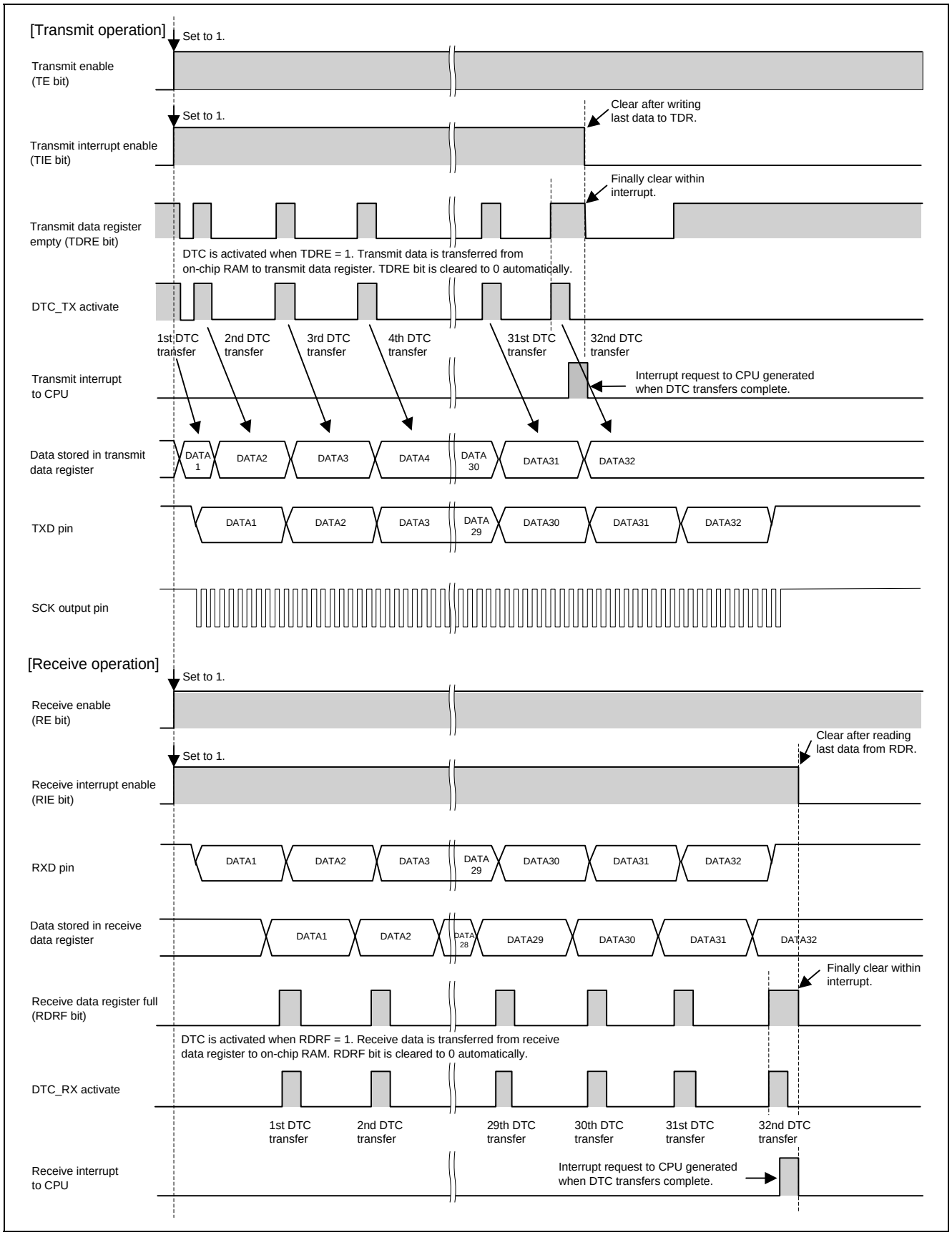


Figure 6 Operation

2.3 Setting Procedure for Functions Used

The procedure for making initial settings for the functions used by the sample program is described below.

Figure 7 shows the processing sequence of the sample program, figure 8 shows the setting sequence for canceling module standby, figure 9 shows the setting sequence for the pin configuration controller, figure 10 shows part 1 of the DTC initialization sequence, figure 11 shows part 2 of the DTC initialization sequence, figure 12 shows the initial setting sequence for transmission and reception in clock synchronous mode. Figure 13 shows the processing sequence of the clock synchronous mode transmit interrupt handler, figure 14 shows the processing sequence of the clock synchronous mode receive interrupt handler, and figure 15 shows the processing sequence of the receive error interrupt handler. For details on the settings of each register, see the *SH7216 Group Hardware Manual*.

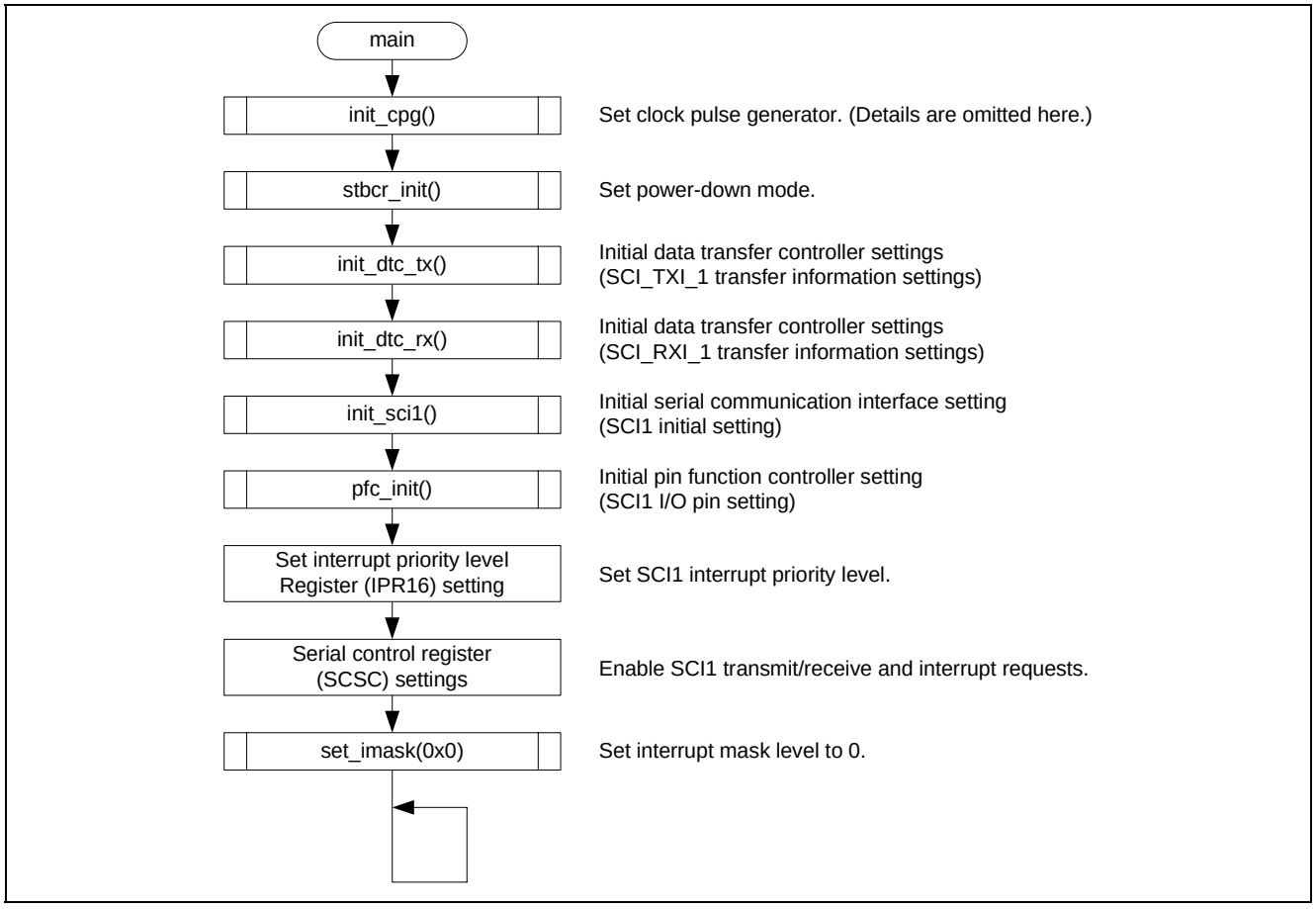


Figure 7 Sample Program Processing Sequence

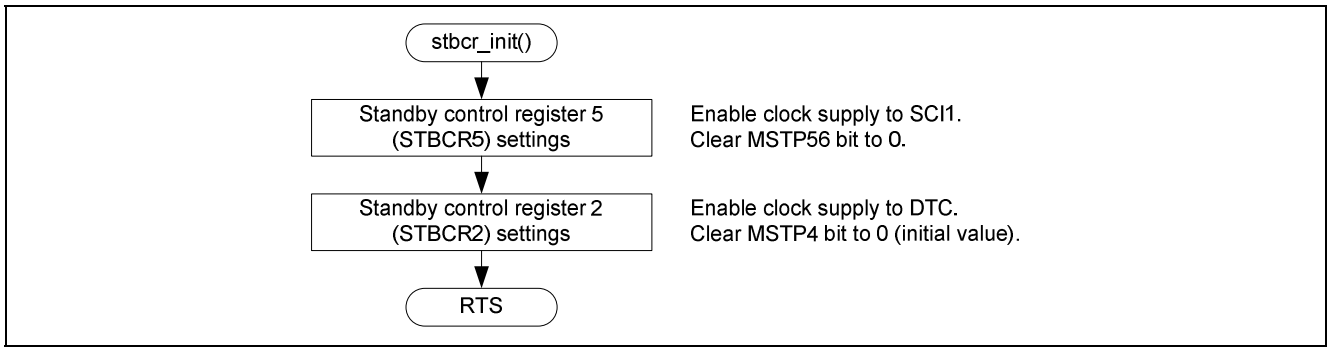


Figure 8 Setting Sequence for Canceling Module Standby

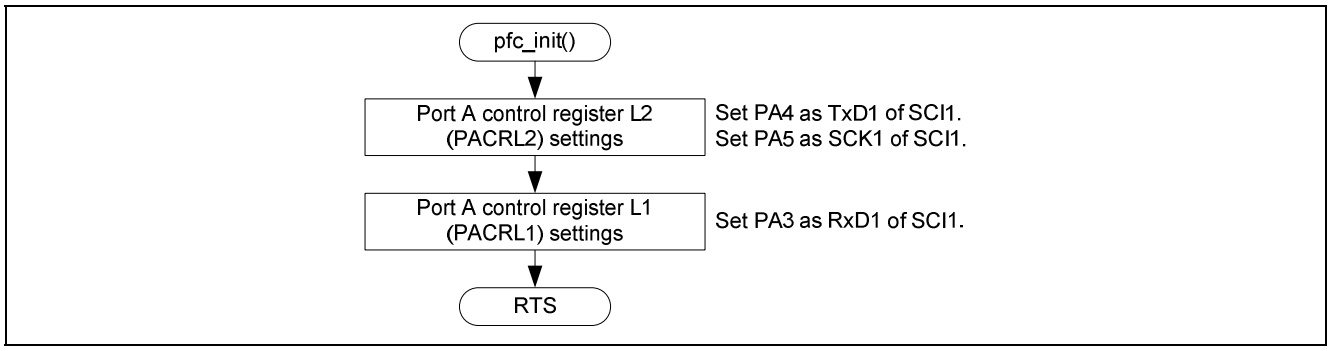


Figure 9 Pin Function Controller Setting Sequence

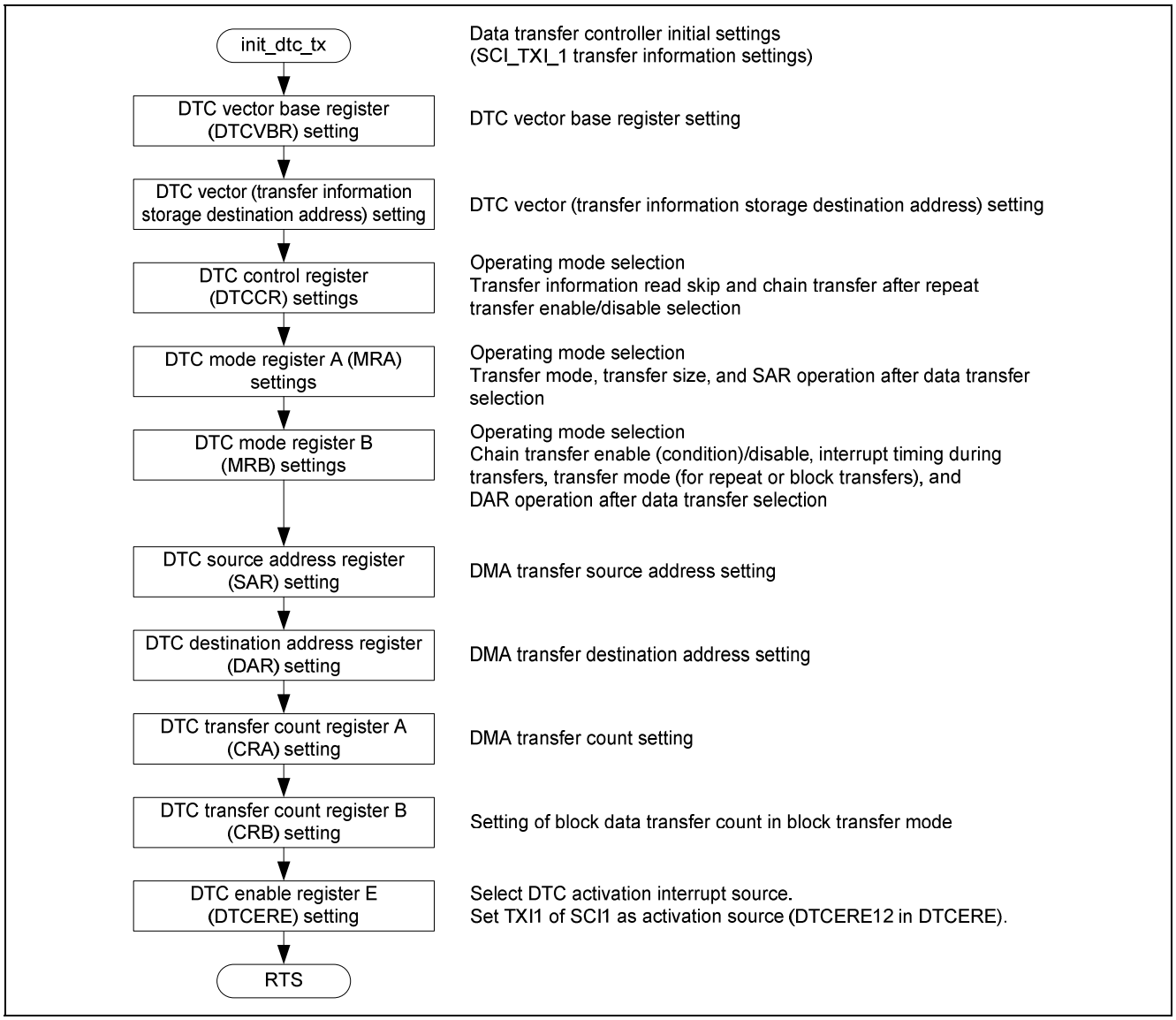


Figure 10 DTC Initialization Sequence (1)

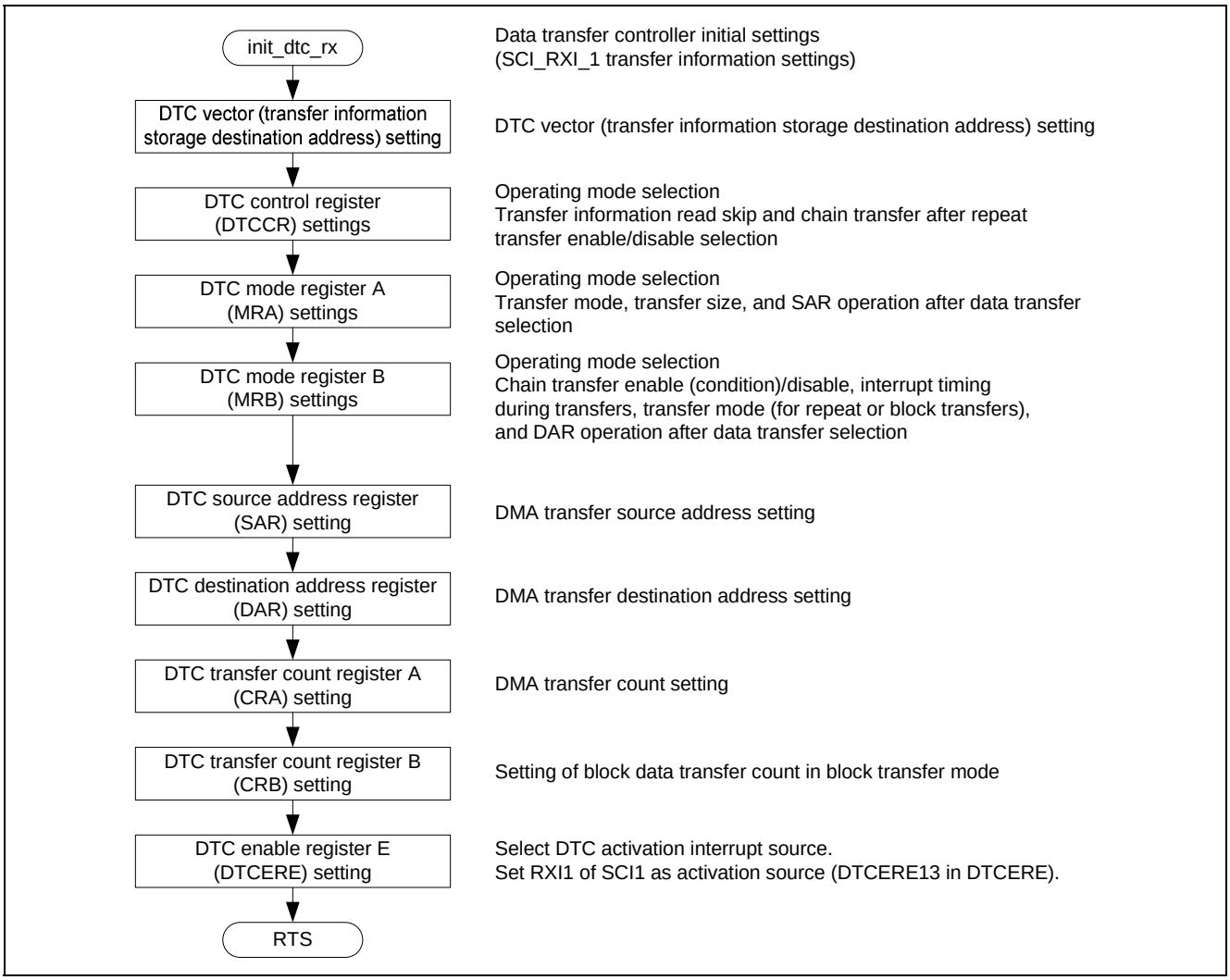


Figure 11 DTC Initialization Sequence (2)

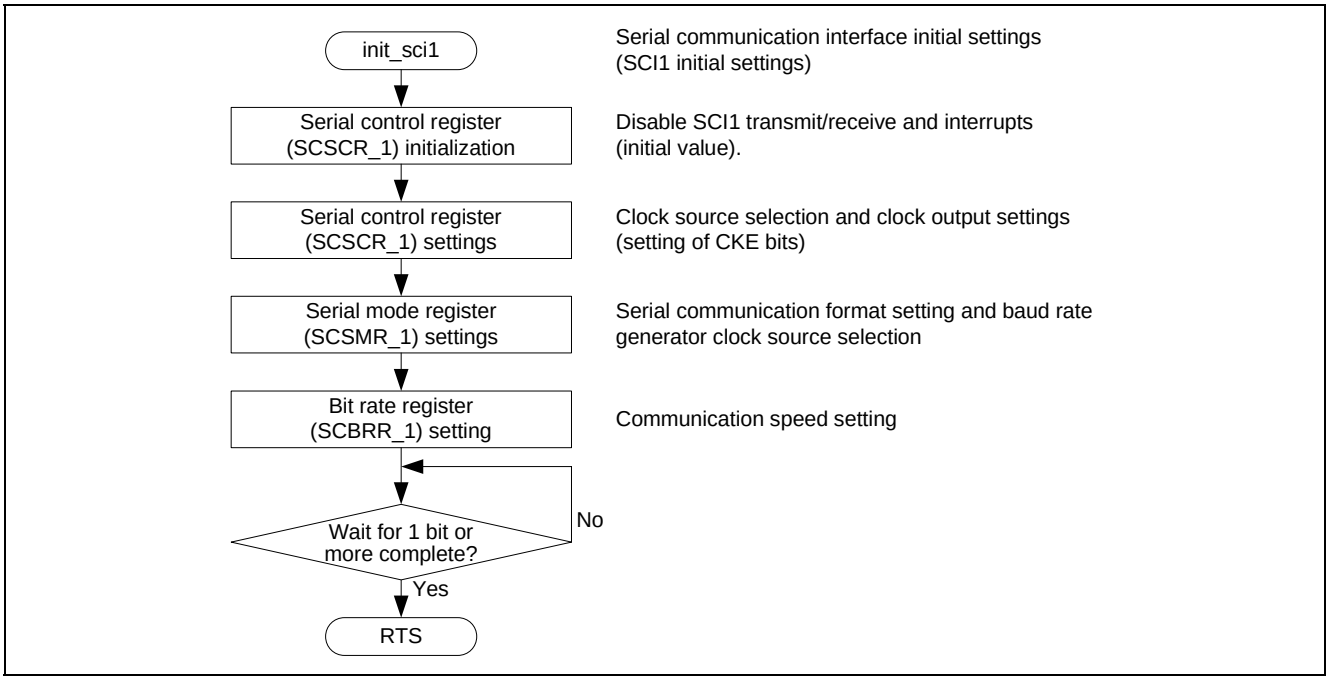


Figure 12 Initial Setting Sequence for Transmission and Reception in Clock Synchronous Mode

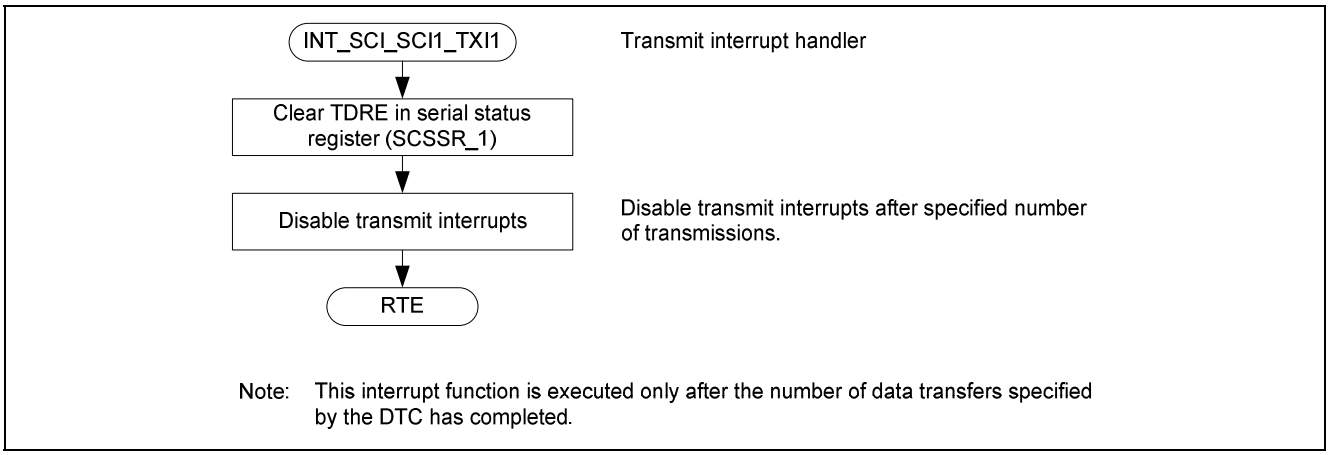


Figure 13 Processing Sequence of Clock Synchronous Mode Transmit Interrupt Handler

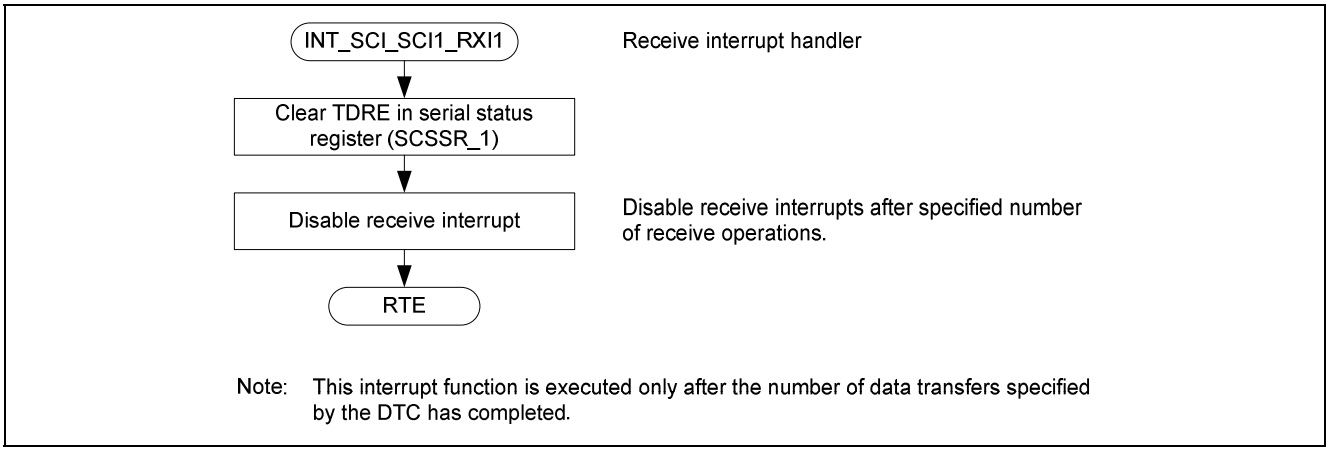


Figure 14 Processing Sequence of Clock Synchronous Mode Receive Interrupt Handler

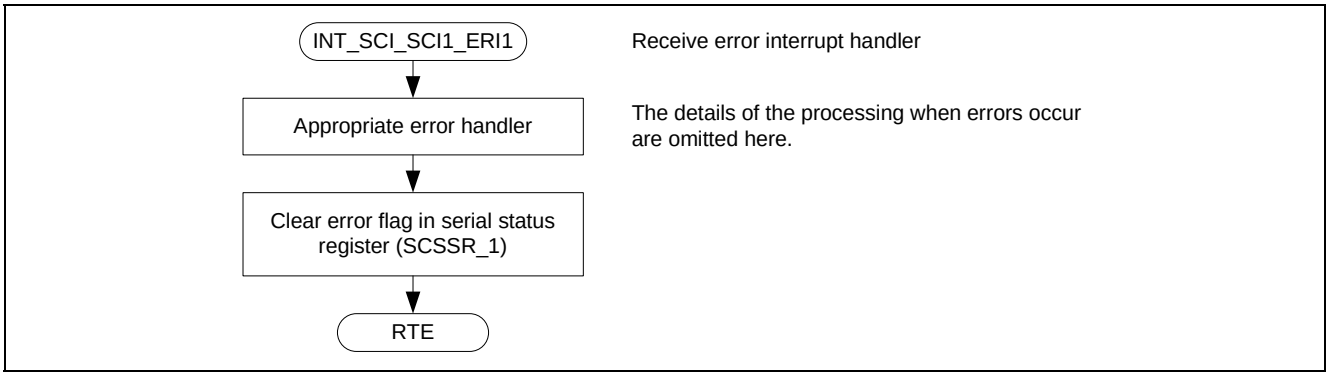


Figure 15 Processing Sequence of Receive Error Interrupt Handler

2.4 Register Settings for Sample Program

2.4.1 Clock Pulse Generator (CPG)

Table 6 lists the clock pulse generator settings.

Table 6 Clock Pulse Generator Settings

Register	Address	Setting value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0303	STC[2:0] = B'011: ×1/8 (Bϕ) IFC[2:0] = B'000: ×1/4 (Iϕ) PFC[2:0] = B'011: ×1/8 (Pϕ)

2.4.2 Power-Down Mode

Table 7 lists the standby control register (STBCR) settings.

Table 7 Standby Control Register Settings

Register	Address	Setting value	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	Clear MSTP4 to 0: DTC operates (initial value) Other bits: Initial values
Standby control register 5 (STBCR5)	H'FFFE0418	H'BF	Clear MSTP56 to 0: SCI1 operates Other bits: Initial values

2.4.3 Interrupt Controller (INTC)

Table 8 lists the interrupt priority register (IPR) settings.

Table 8 Interrupt Priority Register Settings

Register	Address	Setting value	Description
Interrupt priority register 16 (IPR16)	H'FFFE0C14	H'0F00	Set SCI1 interrupt level to 15 (bits 11 to 8).

2.4.4 Data Transfer Controller (DTC)

Table 9 lists the DTC register settings used in the sample program.

Table 9 DTC Register Settings

Register	Address	Setting value	Description
DTC control register (DTCCR)	H'FFFFCC90	H'00	RRS = 0: No transfer information read skip RCHNE = 0: Chain transfer after repeat transfer disabled ERR = 0: No interrupt request
DTC vector base register (DTCVBR)	H'FFFFCC94	H'FFF90000	DTC vector base address setting

DTC transfer information settings with TXI1 of SCI1 as interrupt source

Register	Address	Setting value	Description
DTC mode register A (MRA)	H'FFF90800	H'08	MD[1:0] = B'00: Normal transfer mode Sz[1:0] = B'00: Byte transfer size SM[1:0] = B'10: SAR incremented after transfer
DTC mode register B (MRB)	H'FFF90801	H'00	CHNE = 0: Chain transfer disabled CHNS = 0: No effect because chain transfer disabled DISEL = 0: Interrupt request to CPU after specified number of transfers complete DTS = 0: No effect because normal transfer mode disabled DM[1:0] = B'00: Fixed at DAR
DTC source address register (SAR)	H'FFF90804	—	Transfer source address setting Start address of data table (TR_DATA[]) allocated in on-chip flash memory
DTC destination address register (DAR)	H'FFF90808	SCTDR_1	Transfer destination address setting Transmit data register (SCTDR)
DTC transfer count register A (CRA)	H'FFF9080C	H'20	Transfer count setting 32
DTC transfer count register B (CRB)	H'FFF9080E	H'00	No effect because normal transfer mode disabled
DTC enable register E (DTCERE)	H'FFFE6008	H'1000	Selection of interrupt source to activate DTC TXI1 of SCI1 (DTCERE12)

DTC transfer information settings with RXI1 of SCI1 as interrupt source

Register	**Address**	**Setting value**	**Description**
DTC mode register A (MRA)	H'FFF90810	H'00	MD[1:0] = B'00: Normal transfer mode Sz[1:0] = B'00: Byte transfer size SM[1:0] = B'10: SAR fixed after transfer
DTC mode register B (MRB)	H'FFF90811	H'80	CHNE = 0: Chain transfer disabled CHNS = 0: No effect because chain transfer disabled DISEL = 0: Interrupt request to CPU after specified number of transfers complete DTS = 0: No effect because normal transfer mode disabled DM[1:0] = B'00: Incremented at DAR
DTC source address register (SAR)	H'FFF90814	SCRDR_1	Transfer source address setting Receive data register (SCRDR)
DTC destination address register (DAR)	H'FFF90818	—	Transfer destination address setting Start address of buffer area allocated in on-chip RAM (DTC_RX_ADD)
DTC transfer count register A (CRA)	H'FFF9081C	H'20	Transfer count setting 32
DTC transfer count register B (CRB)	H'FFF9081E	H'00	No effect because normal transfer mode disabled
DTC enable register E (DTCERE)	H'FFFE6008	H'2000	Selection of interrupt source to activate DTC RXI1 of SCI1 (DTCERE13)

2.4.5 Serial Communication Interface 1 (SCI1)

Table 10 lists the SCI (channel 1) register settings used in the sample program.

Table 10 SCI1 (Channel 1) Register Settings

Register	Address	Setting value	Description
Serial mode register (SCSMR_1)	H'FFFF8800	H'80	C/A = 1: Clock synchronous mode CHR = 0: 8-bit data CKS[1:0] =B'00: Pϕ clock
Bit rate register (SCBRR_1)	H'FFFF8802	D'124	Asynchronous mode Bit rate: 100 k (bps)
Serial control register (SCSCR_1)	H'FFFF8804	H'00	Initial settings TIE = 0: Transmit data empty interrupt (TXI) requests disabled RIE = 0: Receive data full interrupt (RXI) requests and receive error interrupt (ERI) requests disabled TE = 0: Transmit operation disabled RE = 0: Receive operation disabled
			When making settings Clock synchronous mode CEK[1:0] = B'00: Internal clock/SCK pin sync clock output
		H'F0	When transmit/receive enabled TIE = 1: Transmit data empty interrupt (TXI) requests enabled RIE = 1: Receive data full interrupt (RXI) requests and receive error interrupt (ERI) requests enabled TE = 1: Transmit operation enabled RE = 1: Receive operation enabled
Serial status register (SCSSR_1)	H'FFFF8808	H'84	Initial settings TDRE = 1: Transmit data register empty flag TEND = 1: Transmit end flag
		H'04	When making settings Clear TDRE flag.

3. Reference Documents

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Hardware Manual
  SH7216 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)

Website and Support

Renesas Electronics Website
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Inquiries
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Apr.27.10	—	First edition issued
1.01	Jun.25.10	—	Modifications to source project due to change in FRQCR setting method

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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