SH7216 Group

Ethernet PHY Board Design Guide

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Summary

This application note is intended to assist customers in designing the Ethernet board to connect the SH7214/SH7216 Microcomputer (MCU) with an Ethernet PHY-LSI.

Target Device

SH7214/SH7216

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1. Interface

1.1 Overview

1.1.1 Media Independent Interface (MII)

The Media Independent Interface (MII) is a standard interface used to connect a network controller chip (MAC) with the media interface chip (PHY). Figure 1 shows the MII signal connection.

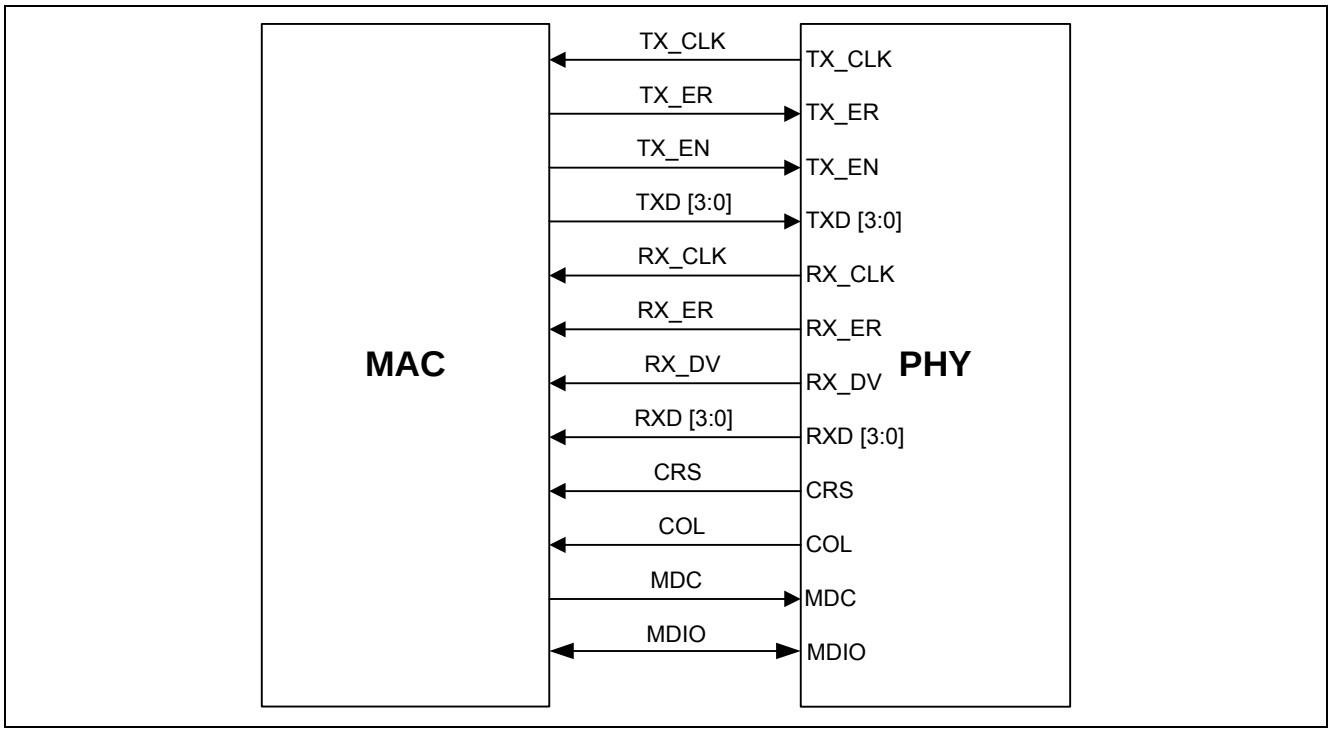

Figure 1 MII Signal Connection

1.1.2 Media Dependent Interface (MDI)

The Media Dependent Interface (MDI) is an interface used to connect the media interface chip (PHY) with the pulse transformer or RJ45 connector. Figure 2 shows the MDI signal connection.

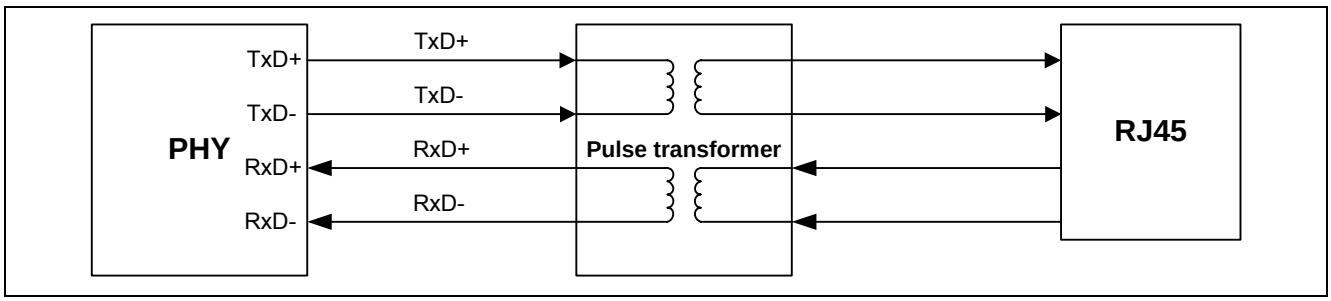

Figure 2 MDI Signal Connection

1.2 Interface Pins Functions

1.2.1 Media Independent Interface (MII)

Table 1 lists the pin functions of the Media Independent Interface (MII).

Table 1 Media Independent Interface (MII) Pin Functions

Signal Name	Function	I/O (MAC)	I/O (PHY)	Remarks
TX_CLK	Transmit clock	I	O	TX_EN, TXD [3:0] and TX_ER timing clocks 10Base-T: 2.5 MHz 100Base-TX: 25 MHz
TX_ER	Transmit error	O	I	
TX_EN	Transmit enable	O	I	
TXD0	Transmit data	O	I	
TXD1	Transmit data	O	I	
TXD2	Transmit data	O	I	
TXD3	Transmit data	O	I	RX_DV, RXD [3:0], and TX_ER timing clocks 10Base-T: 2.5 MHz 100Base-T: 25 MHz
RX_CLK	Receive clock	I	O	
RX_ER	Receive error	I	O	
RX_DV	Receive data invalid	I	O	
RXD0	Receive data	I	O	
RXD1	Receive data	I	O	
RXD2	Receive data	I	O	
RXD3	Receive data	I	O	
CRS	Carrier detection	I	O	
COL	Collision detection	I	O	
MDC	Administrative data clock	O	I	
MDIO	Administrative data I/O	I/O	I/O	

1.2.2 Media Dependent Interface (MDI)

Table 2 lists the pin functions of the Media Dependent Interface (MDI).

Table 2 Media Dependent Interface (MDI) Pin Functions

Signal Name	Function	I/O (PHY)	Remarks
TXD+	Transmit output+	O	Differential signal transmit output
TXD−	Transmit output−	O	
RXD+	Receive input+	I	Differential signal receive input
RXD−	Receive input−	I	

2. Transmission Line

2.1 MII

When designing the MII wiring pattern, note the following:

- MII transmission line must be designed as the high-frequency circuit.
- Place the MII transmission line on the layer adjacent to GND plane.
- Place the MII transmission line as short as possible.
- Do not allocate other signal lines close to the MII transmission line.
- Avoid using vias on the MII transmission line.
- MII transmission line must be wired with straight lines. If you cannot avoid doing so, the line must be bent gently in an arc or up to 135 degrees.
- Add the series resistors on all transceiver MII outputs.
- Impedance must be controlled on the MDC pin transmission line. The characteristic impedance required for the MDC pin transmission line is the differential impedance 50 Ω ± 15%. The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more information.
- Install a resistor of 2.0 kΩ ± 5% on the MDIO pin transmission line.

Figure 3 shows the guideline for the wiring corner angle. Figure 4 shows the MII layout example.

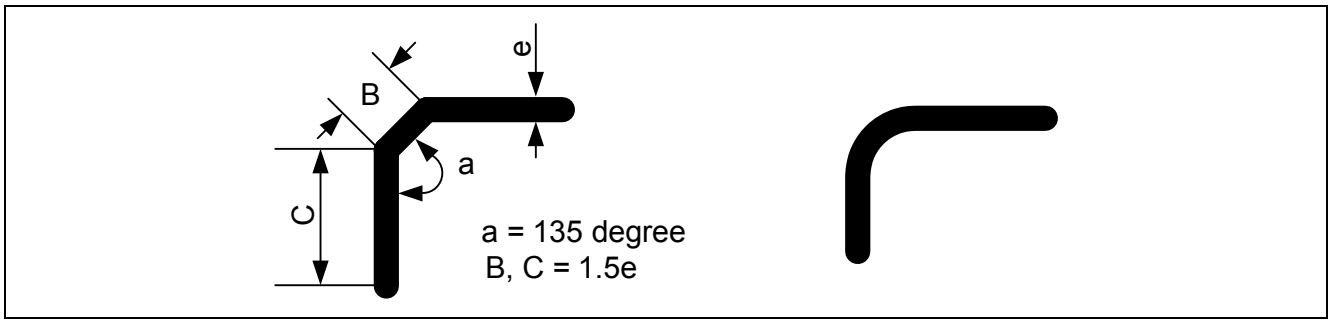

Figure 3 Wiring Corner Angle

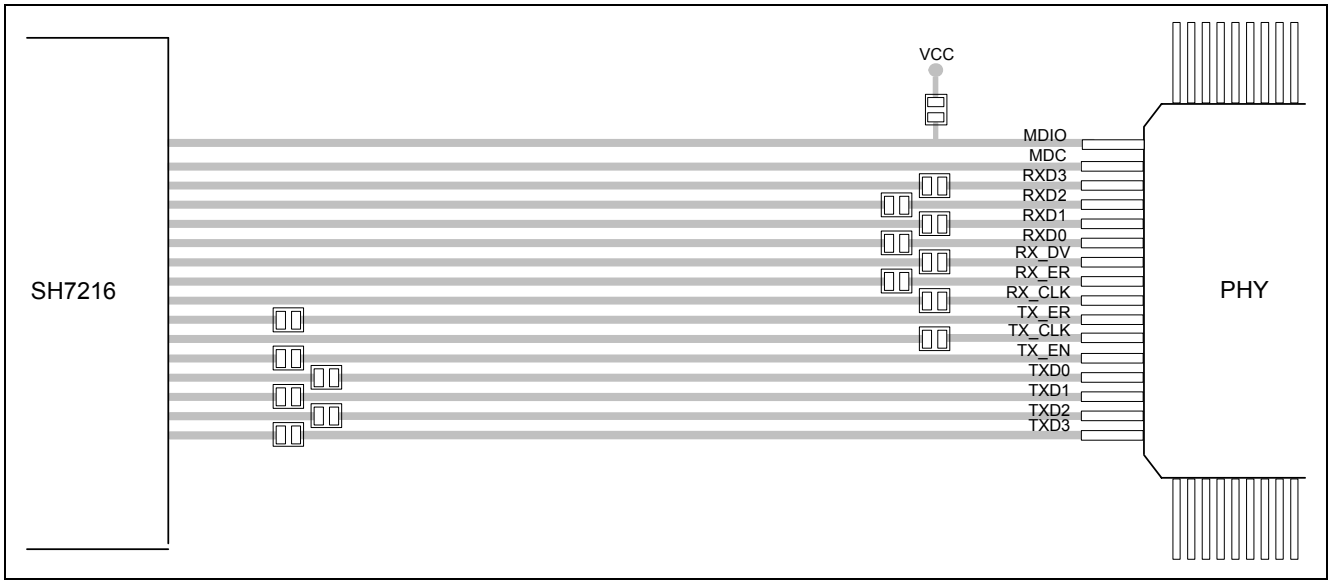

Figure 4 MII Layout

2.2 MDI

MDI transmission line must be designed as the high-frequency circuit. Impedance must be controlled on the line.

Refer to the datasheet of PHY when designing the wiring pattern, and termination pattern of the MDI transmission line.

3. Power Supply, Ground

Use a multi-layer PCB with the inner layers dedicated to GND and VCC.

3.1 MII

When designing the MII power supply and ground pattern, note the following:

- VCC and GND planes must be designed as wide as possible.
- Use low inductance, ceramic surface mount decoupling capacitors.
- As the ESR (Equivalent Series Resistor) of the aluminum electrolytic capacitor and tantalum capacitor are generally high which may affect the jitter value, these capacitors should be thoroughly designed and tested before use.
- Locate these decoupling capacitors as close as possible to the VCC and GND pins of the PHY.
- Connect the decoupling capacitor to the VCC and GND planes to achieve the lowest possible inductance.
- All decoupling capacitor and PHY VCC and GND connections should tie immediately to a VCC or GND plane via with minimum trace inductance.

3.2 MDI

Refer to the datasheet of PHY when designing the MDI power supply and ground pattern.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.02.10	—	First edition issued
1.01	Dec.20.11	4	Changed a resistor value to 2.0 kΩ ± 5%.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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