SH7216 Group

A/D Converter Activation at MTU2 Channel 0 Compare-Match

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Introduction

This application note describes activation of the A/D converter at a compare-match (TGRE_0) in MTU2 channel 0 (ch0) of the SH7216. This function can be used to perform A/D conversion at a timing specified by the user.

Note that although the program code presented in this application note has been verified to work as intended, it should be checked in the actual operating environment before being put into actual use.

Target Device

SH7216

Contents

1. Preface

1.1 Specifications

In this sample task, MTU2 channel 0 (ch0) is used to activate the A/D converter, which performs A/D conversion of the voltage applied to the AN0 pin. The specifications of this sample task are listed below.

- MTU2 ch0 operates in PWM mode 1, outputting a PWM waveform from the TIOC0A pin.
- The A/D converter is activated at a compare-match with TGRE_0 in MTU2 ch0.
- The A/D conversion result is stored in the on-chip RAM.
- A/D converter operates in single mode.
- After A/D conversion is performed three times, MTU2 ch0 timer count operation stops.

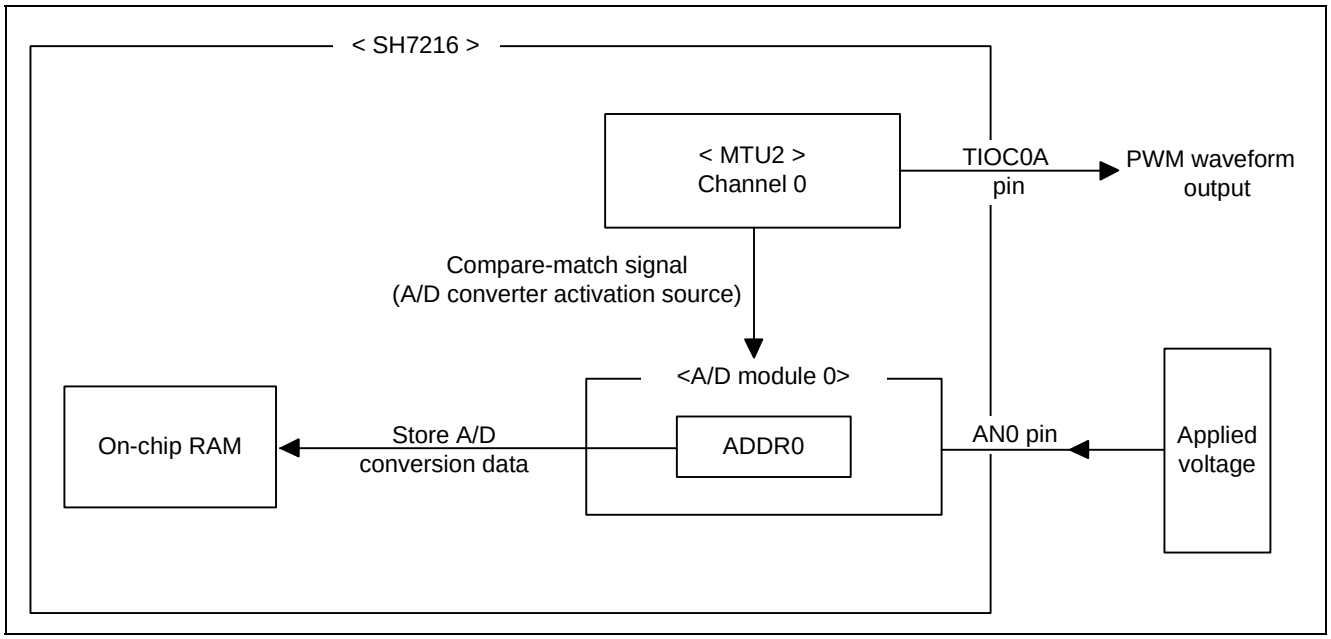


Figure 1 Block Diagram of A/D Conversion Using MTU2

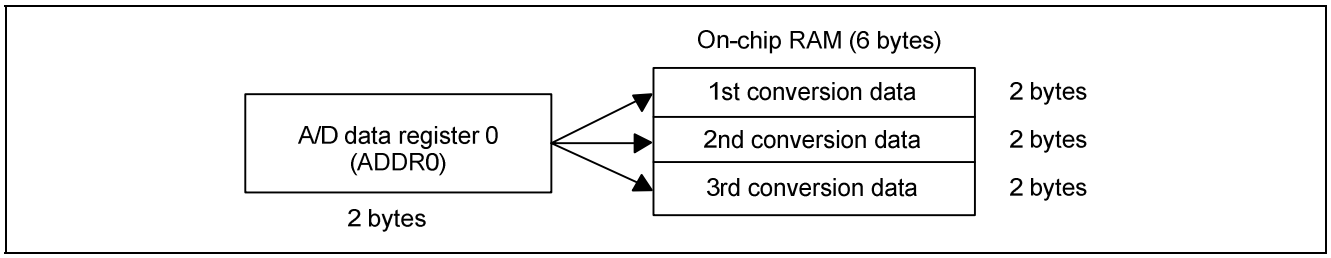


Figure 2 Storage of A/D Conversion Data in On-Chip RAM

1.2 Functions

- A/D converter (ADC)
- Multi-function timer pulse unit 2 (MTU2)
- Clock pulse generator (CPG)
- Pin function controller (PFC)
- Interrupt controller (INTC)

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz MTU2S clock: 100 MHz AD clock: 50 MHz
Integrated development environment	Renesas Electronics High-Performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC Engine Family C/C++ Compiler Package, Ver.9.03.00 Release02
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu -pic=1 –object="$(CONFIGDIR)\$(FILELEAF).obg" -debug –gbr=auto –chgincpath –errorpath –global_volatile=0 -opt_range=all –infinite_loop=0 –del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

Application notes related to this application note are listed below. Refer to them in conjunction with this application note.

- SH7216 Group Application Note: A/D Converter Activation Skipping Using MTU2
- SH7216 Group Application Note: Delayed Activation of A/D Converter by MTU2

2. Overview

The sample program activates the A/D converter (ADC) at a compare-match in ch0 of multi-function timer pulse unit 2 (MTU2).

2.1 Operation of Functions

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

Channel 0 of MTU2 uses PWM mode 1. Figure 3 is a block diagram of MTU2, and figure 4 is a block diagram of the functioning of ch0 of MTU2.

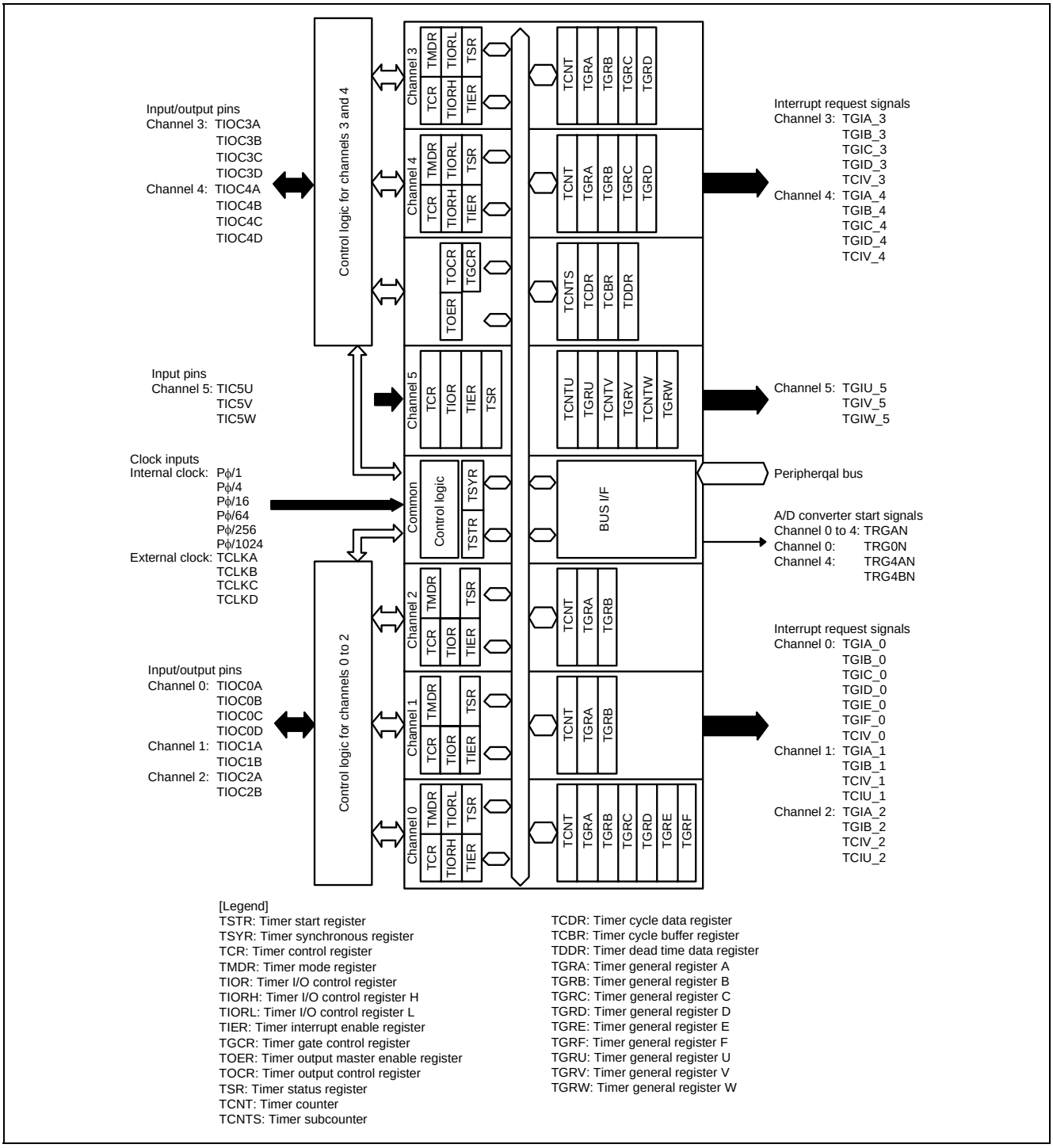


Figure 3 MTU2 Block Diagram

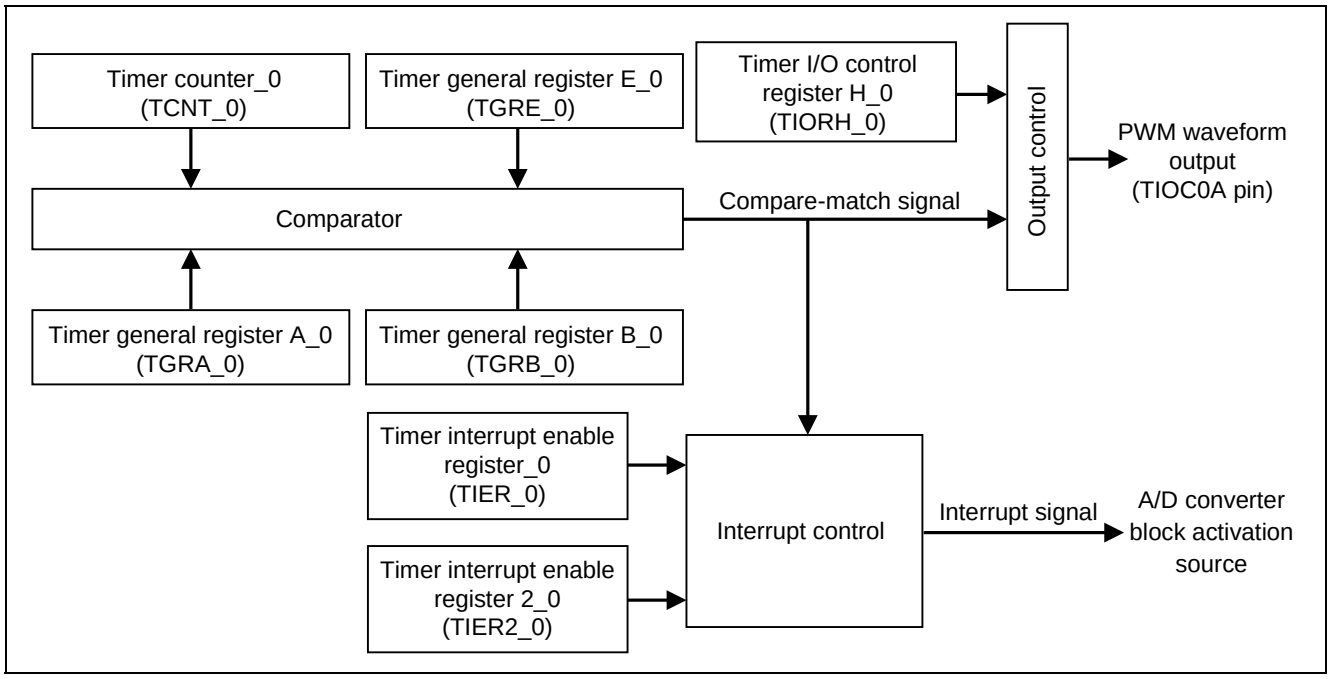


Figure 4 Block Diagram of MTU2 ch0

- Timer general register A_0 (TGRA_0) operates as a compare register. The PWM waveform cycle is set in TGRA_0.
- Timer general register B_0 (TGRB_0) operates as a compare register. The PWM waveform duty is set in TGRB_0.
- Timer general register E_0 (TGRE_0) operates as a compare register. The A/D conversion timing is set in TGRE_0.
- Timer counter 0 (TCNT_0) is a 16-bit readable/writable counter. The TCNT_0 counter is cleared when a compare-match with TGRA_0 occurs.
- Timer IO control register H_0 (TIORH_0) is an 8-bit readable/writable register. The functions of TGRA_0 and TGRB_0, and the output level of the TIOC0A pin, are set in TIORH_0.
- Timer interrupt enable register 0 (TIER_0) is an 8-bit readable/writable register. Enabling/disabling of interrupt requests is controlled by TIER_0.
- Timer interrupt enable register 2_0 (TIER2_0) is an 8-bit readable/writable register. Interrupt requests related to TGRE_0 and TGRF_0, and enabling/disabling of A/D converter activation by TGRE_0, are controlled by TIER2_0.

2.1.2 A/D Converter

In the sample task, A/D module 0 is activated by MTU2 at the A/D conversion start trigger, and A/D conversion takes place in single mode. Figure 5 is a block diagram of the A/D0 module, and its functions are described below.

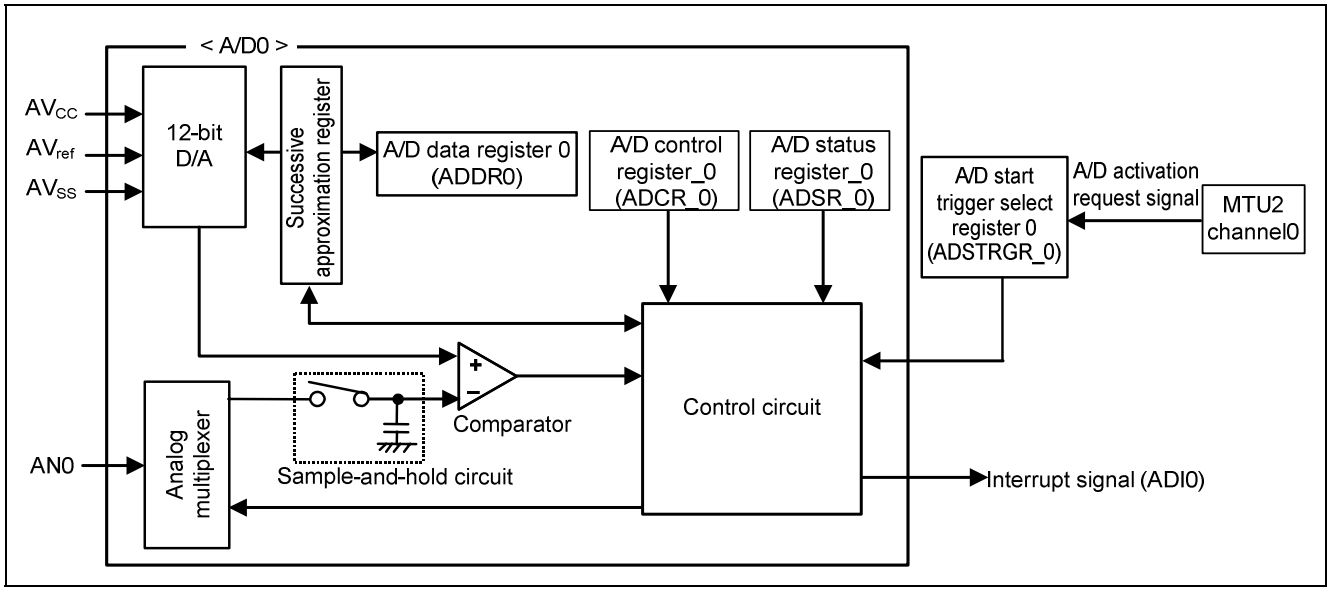


Figure 5 Block Diagram of A/D Module 0

- A/D data register 0 (ADDR0) is a 16-bit read-only register that stores the conversion result from analog input channel (AN0). The conversion data is stored in bits 15 to 6 of ADDR, and the value of the lower 6 bits is always 0.
- A/D control register 0 (ADCR_0) and A/D status register 0 (ADSR_0) control A/D conversion operation.
- A/D start trigger select register _0 (ADSTRGR_0) is set to external trigger for A/D conversion start requests.

3. Operation

Figure 6 illustrates the operation of the sample program, and table 1 lists the software and hardware processing steps.

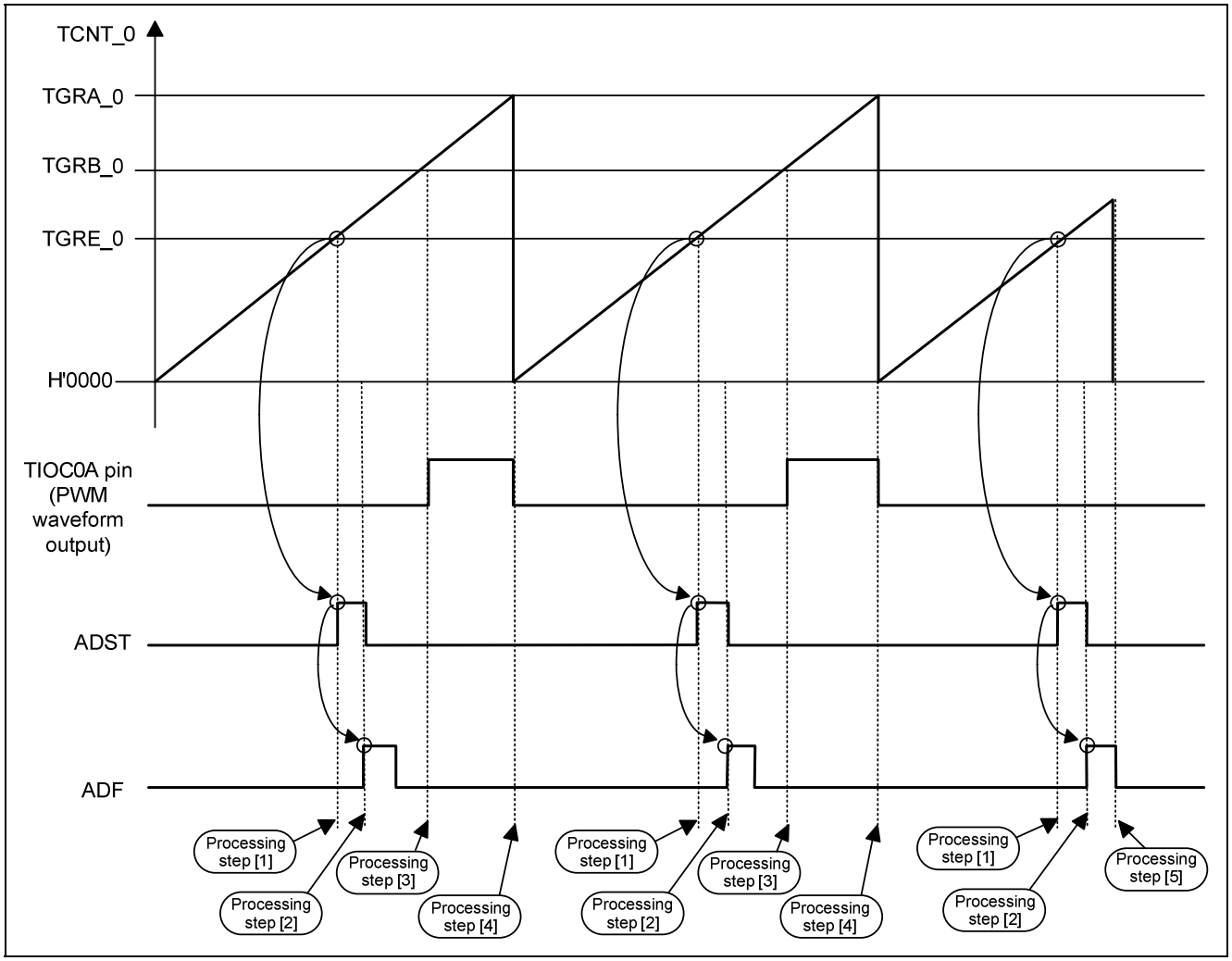


Figure 6 Operation

Table 1 Software And Hardware Processing

	Software Processing	Hardware Processing
Processing step [1]	—	• Activate A/D converter (A/D conversion start) at compare-match of TCNT_0 and TGRE_0.
Processing step [2]	• Clear ADF flag at A/D end interrupt. • Store A/D conversion result in on-chip RAM.	• At end of A/D conversion set ADF flag to 1. • Issue A/D end interrupt.
Processing step [3]	—	• Output H-level on TIOC0A pin at compare-match of TCNT_0 and TGRB_0.
Processing step [4]	• Clear TGFA_0 flag at TGRA_0 compare-match interrupt. • Change duty (TGRB_0) and A/D conversion timing (TGRE_0).	• Output L-level on TIOC0A pin at compare-match of TCNT_0 and TGRA_0. • Clear TCNT_0. • Issue TGRA_0 compare-match interrupt.
Processing step [5]	• Clear CTS0 bit in TSTR register to 0.	• Stop MTU2 ch0 timer count operation.

4. Software

4.1 Modules

Table 2 lists the modules of the sample task.

Table 2 Modules

Module	Label	Description
Main routine	main()	Performs initial settings for MTU2 and A/D module, and starts timer count.
TGRA_0 interrupt routine	int_tgia0()	Updates duty and A/D converter activation cycle.
A/D conversion end interrupt routine	int_ad0()	Stores A/D conversion result in on-chip RAM and stops timer count.

4.2 Internal Registers

Tables 3 to 6 list the registers used in the sample task. Note that the setting values shown are those used in the sample task and differ from the initial values.

Table 3 Internal Registers Used (1)

Register	Bit	Bit Name	Setting Value	Description
FRQCR			H'0241	Frequency control register Specifies the division ratios of the operating frequencies relative to the output frequency of the PLL circuit. When FRQCR = H'0241, the division ratios are as follows: Internal clock: ×1, bus clock: ×1/4, peripheral clock: ×1/4, MTU2S clock: ×1/2, MTU2 clock: ×1/2
STBCR3			H'BE	Standby control register 3
	5	MSTP35	0	Module stop bit 35 When MSTP22 = b'0, the clock is supplied to MTU2.
	2	MSTP32	0	Module stop bit 32 When MSTP16 = b'0, the clock is supplied to ADC_0.
PECRL1			H'0001	Port E control register L1
	15	—	0	Reserved bit
	14 13 12	PE3MD2 PE3MD1 PE3MD0	0 0 0	PE3 mode bits When PE3MD[2-0] = b'000, the pin function is set to PE3 (general I/O).
	11	—	0	Reserved bit
	10 9 8	PE2MD2 PE2MD1 PE2MD0	0 0 0	PE2 mode bits When PE2MD[2-0] = b'000, the pin function is set to PE2 (general I/O).
	7	—	0	Reserved bit
	6 5 4	PE1MD2 PE1MD1 PE1MD0	0 0 0	PE1 mode bits When PE1MD[2-0] = b'000, the pin function is set to PE1 (general I/O).
	3	—	0	Reserved bit
	2 1 0	PE0MD2 PE0MD1 PE0MD0	0 0 1	PE0 mode bits When PE0MD[2-0] = b'100, the pin function is set to TIOC0A.

Table 4 Internal Registers Used (2)

Register	Bit	Bit Name	Setting Value	Description
PEIORL			H'0001	Port E IO register L
	0	PE0IOR	1	When PE0IOR = b'1, the PE0 (TIOC0A) pin is set to output.
IPRD			H'A000	Interrupt priority register D Interrupt level of TGIA_0 in MTU2 is set to 10.
IPRK			H'A000	Interrupt priority register K Interrupt level of ADI_0 in A/D set to 10.
ADCR_0			H'12	A/D control register 0
	7	ADST	0	A/D start Standby state when cleared to 0
	6	ADCS	0	A/D continuous scan When ADCS = b'0, single-cycle scan is selected.
	5	ACE	0	Auto-clear enable When ACE = b'0, ADDR auto-clear by ADDR read is disabled.
	4	ADIE	1	A/D interrupt enable When ADIE = b'1, A/D conversion end interrupt is enabled.
	3, 2	—	0	Reserved bits
	1	TRGE	1	Trigger enable When TRGE = b'1, A/D conversion start at A/D conversion start trigger from MTU2/MTU2S is enabled.
	0	EXTRG	0	Trigger select When EXTRG = b'0, A/D converter is activated at A/D conversion start trigger from MTU2/MTU2S.
ADSR_0			H'01	A/D status register_0
	7 to 1	—	0	Reserved bits
	0	ADF	0	A/D end flag
ADSTRGR_0			H'08	A/D start trigger select register 0 The A/D module 0 A/D conversion start trigger is set to MTU2 ch0 compare-match (TRG0N).
TCR_0			H'21	Timer control register
	7 6 5	CCLR2 CCLR1 CCLR0	0 0 1	Counter clear 2 to 0 When CCLR[2-0] = b'001, the TCNT_0 counter clear source is set to AGRA_0 compare-match.
	4 3	CKEG1 CKEG0	0 0	Clock edge 1 and 0 When CKEG[1,0] = b'00, counting is at the rising edge of the internal clock signal.
	2 1 0	TPSC2 TPSC1 TPSC0	0 0 1	Timer prescaler When TPSC[2-0] = b'001, TCNT_0 counts at MPϕ/4.

Table 5 Internal Registers Used (3)

Register	Bit	Bit Name	Setting Value	Description
TMDR_0			H'02	Timer mode register_0
	7	—	0	Reserved bit
	6	BFE	0	Buffer operation E When BFE = b'0, TGRE_0 and TGRF_0 operate normally.
	5	BFB	0	Buffer operation B When BFB = b'0, TGRB_0 and TGRD_0 operate normally.
	4	BFA	0	Buffer operation A When BFA = b'0, TGRA_0 and TGRC_0 operate normally.
	3 2 1 0	MD3 MD2 MD1 MD0	0 0 1 0	Mode 3 to 0 When MD[3-0] = b'0010, the operation mode is PWM mode 1.
TIORH_0			H'21	Timer I/O control register
	7 6 5 4	IOB3 IOB2 IOB1 IOB0	0 0 1 0	I/O control B3 to B0 When IOB[3-0] = b'0010, the TIOC0A pin is set to initial output 0, output 1 at TGRB_0 compare-match.
	3 2 1 0	IOA3 IOA2 IOA1 IOA0	0 0 0 1	I/O control A3 to A0 When IOA[3-0] = b'0001, the TIOC0A pin is set to initial output 0, output 0 at TGRA_0 compare-match.
TIER_0			H'01	Timer interrupt enable register_0
	7	TTGE	0	A/D conversion start request enable When TTGE = b'0, A/D conversion start at TGRA_0 compare-match is disabled.
	6	—	0	Reserved bit
	5	—	0	Reserved bit
	4	TCIEV	0	Overflow interrupt enable When TCIEV = b'0, interrupt request by TCFV is disabled.
	3	TGIED	0	TGR interrupt enable D When TGIED = b'0, interrupt request by TGFD bit is disabled.
	2	TGIEC	0	TGR interrupt enable C When TGIEC = b'0, interrupt request by TGFC bit is disabled.
	1	TGIEB	0	TGR interrupt enable B When TGIEB = b'0, interrupt request by TGFB bit is disabled.
	0	TGIEA	1	TGR interrupt enable A When TGIEA = b'1, interrupt request by TGFA bit is enabled.
TIER2_0			H'80	Timer interrupt enable register 2_0
	7	TTGE2	1	A/D conversion start request enable 2 When TTGE = b'0, A/D conversion start request at TGRE_0 compare-match is enabled.
	6 to 2	—	0	Reserved bits
	1	TGIEF	0	TGR interrupt enable F When TGIEF = b'0, interrupt request by TGFF bit is disabled.
	0	TGIEE	0	TGR interrupt enable E When TGIEE = b'0, interrupt request by TGFE bit is disabled.

Table 6 Internal Registers Used (4)

Register	Bit	Bit Name	Setting Value	Description
TGRA_0			Pul_cyc	Timer general register A_0 Clears the counter and outputs 0 from the TIOC0A pin at compare-match of TCNT_0 and TGRA_0. Sets the PWM waveform cycle.
TGRB_0			Duty	Timer general register B_0 Outputs 1 from the TIOC0A pin at compare-match of TCNT_0 and TGRB_0. Sets the PWM waveform duty.
TGRE_0			Ad_start	Timer general register E_0 Activates the A/D converter at compare-match of TCNT_0 and TGRE_0. Sets the A/D converter activation timing.
TCNT_0			H'0000	Timer counter 0 Channel 0 timer counter
TSTR			H'01	Timer start register
	7	CTS4	0	Counter start 4 When CTS4 = b'0, TCNT_4 count operation stops.
	6	CTS3	0	Counter start 3 When CTS3 = b'0, TCNT_3 count operation stops.
	5	—	0	Reserved bit
	4	—	0	Reserved bit
	3	—	0	Reserved bit
	2	CTS2	0	Counter start 2 When CTS2 = b'0, TCNT_2 count operation stops.
	1	CTS1	0	Counter start 1 When CTS1 = b'0, TCNT_1 count operation stops.
	0	CTS0	1	Counter start 0 When CTS0 = b'1, TCNT_0 count operation starts.

4.3 Variables

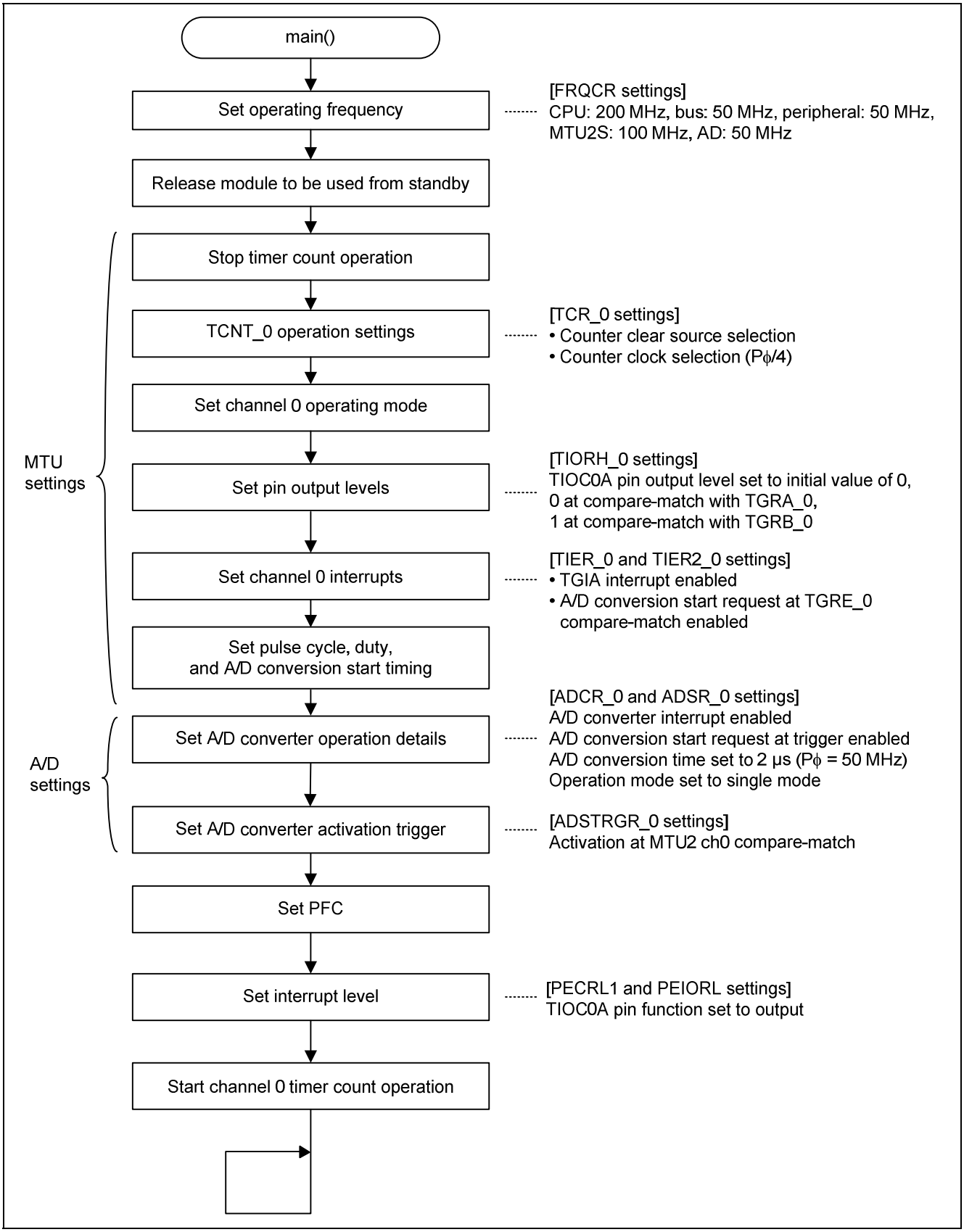
Table 7 lists the variables used in the sample task.

Table 7 Variables

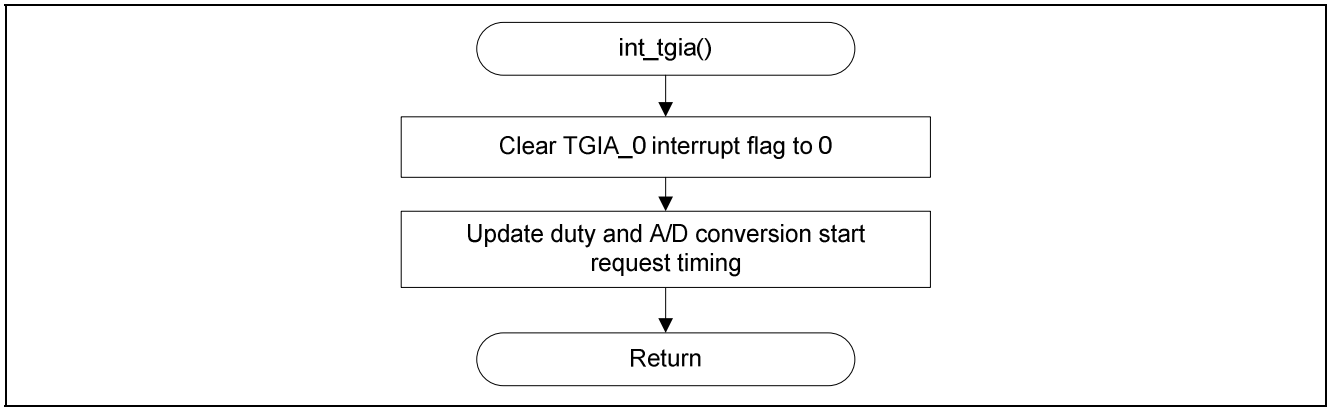
Label	Description	Module
Pul_cyc	PWM waveform cycle (set in TGRA_0)	Main routine
Duty	PWM waveform duty (set in TGRB_0)	TGRA_0 compare-match interrupt routine
Ad_start	A/D conversion start timing (set in TGRE_0)	
Ad_data[0-2]	Stores A/D conversion result	A/D conversion end interrupt routine
Ad_count	A/D conversion count	

5. Flowcharts

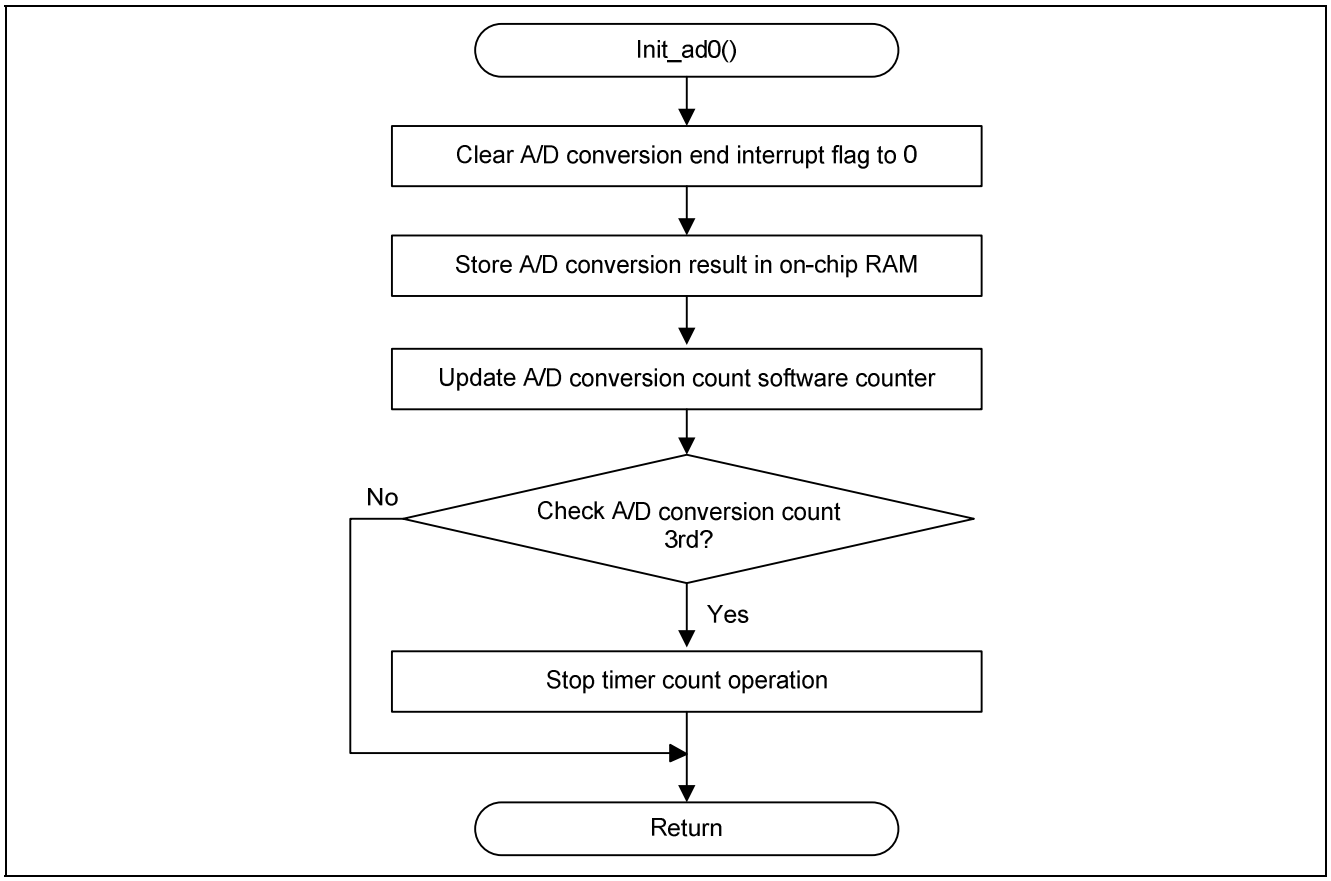
5.1 Main Routine



5.2 TGRA_0 Compare-Match Interrupt Routine



5.2.1 A/D Conversion End Interrupt Routine



6. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual [REJ09B0051]
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Hardware Manual
  SH7216 Group Hardware Manual [REJ09B0543]
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.23.10	—	First edition issued
1.10	Feb.28.11	—	Added read after FRQCR settings

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   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
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Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
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Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
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Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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