SH7216 Series

Digital Power Control for Boost

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Introduction

This application note describes the design of a step-up boost based on the Renesas SH7216 microcontrollers.

This step-up boost provide a reference design using Renesas SH7216 MCU, which has the fast processing core and I/O port for the controller needs.

Target Device

SuperH RISC engine Family SH7216 Series

Contents

1. System Architecture

The step-up boost consists of three main sections. These are:

- CPU Board.
- Three Batteries in series
- Step-Up Boost Board

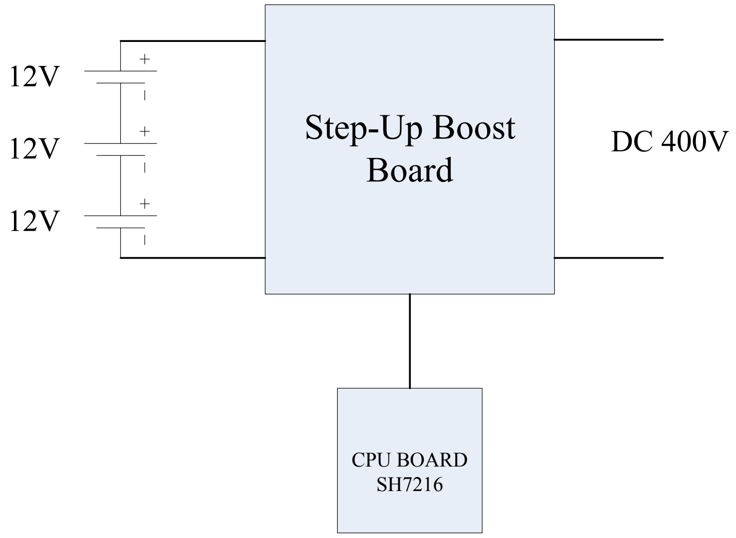

Figure 1 Block diagram

2. Specifications

The detail designed specifications of the power stage board are shown in TABLE 1.

Table 1 System specifications

	Boost
Input Voltage	DC 31.5~40.5 V
Output Voltage	DC 400 V
Output Waveform	DC
Type/Topology	H-Bridge
Max. Input Current	DC 44.4 A
Max. Output Current	DC 3.5 A
Max. Output Power	1.4 kW
Battery	12 V * 3

CPU Board:

- Renesas Microcontroller: SH7216

Battery:

- Three 12V 7.2Ah Battery in series

NOTE:

The use of high voltage power supplies is extremely dangerous. Only authorized personnel working in a controlled environment are allowed to change the system configuration, at their own risk.

The voltage supply in the standard configuration is 36Vdc.

Renesas does not assume any responsibility for any voluntary modification of the standard demonstration hardware as well as over any misuse of the proposed system.

2.1 CPU Boards

The CPU boards can be used to control the offline UPS. The microcontroller responsible for the following tasks:

1) Battery charging and regulation PI algorithm
2) Boost control
3) Inverter control
4) Relay management
5) MOSFET management.

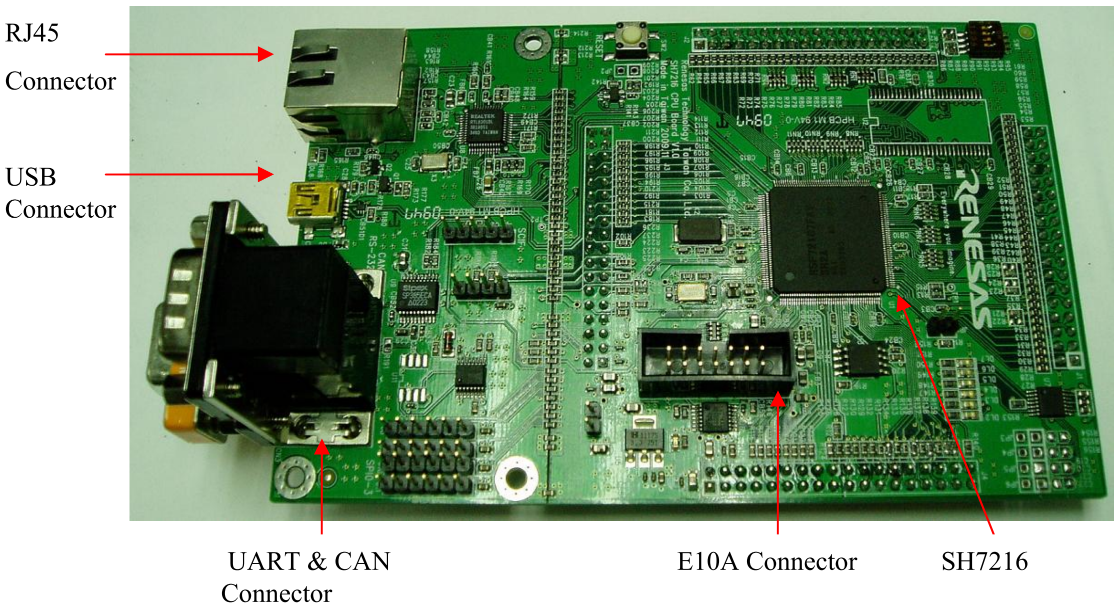

Figure 2 CPU Board

3. System configuration / control block diagram

The PI algorithm method is shown in Figure 3. The output voltage of charger is regulated at 27 V with 0.7 A current limit to prevent damaging of battery.

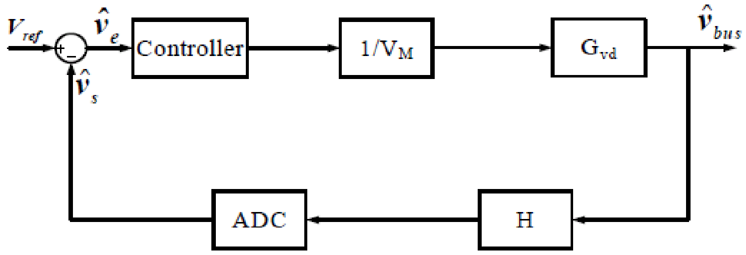

Figure 3 PI algorithm for boost

4. Hardware block diagram analysis

The purpose of H-Bridge boost converter is boosting the battery voltage into high DC voltage. The circuit of H-Bridge boost converter used in this system is shown in Figure 4. The basic topology is an H-Bridge converter with secondary bridge rectifier. Since the input current is large, the primary MOSFETs are connected in parallel.

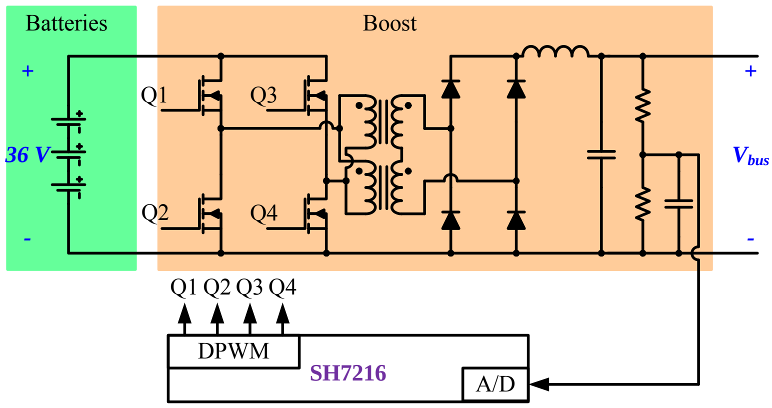

Figure 4 boost circuit

5. Software description

List and description of the software modules and functions

The main settings are:

io_set_cpg: performs the PLL initialization

```
WDT.WRITE.WTCSR = 0xa51e;        => WDT stop, WDT count clock setting
                                 => 1/4096 x P-clock (50MHz; 20.97msec)
WDT.WRITE.WTCNT = 0x5a85;        => Counter initial setting 10msec
CPG.FRQCR.WORD  = 0x0303;        => Clockin = 12.5MHz
                                 => I Clock = 200MHz, B Clock = 50MHz
                                 => P Clock = 50MHz
CPG.MCLKCR.BIT.MSDIVS = 1;       => MTU2S = 100MHz
CPG.ACLKCR.BIT.ASDIVS = 3;       => AD    =  50MHz
STB.CR3.BYTE = 0x02;             => Module Standby Clear
                                 => HIZ,MTU2S,MTU2,POE2,IIC3,ADC0,Reserve(1),FLASH
STB.CR4.BYTE = 0xE2;             => Module Standby Clear
                                 => SCIF3,Reserve(0),CMT,Reserve(1),EtherC
STB.CR5.BYTE = 0x12;             => Module Standby Clear
                                 => SCI0,SCI1,SCI2,SCI4,ADC1
```

boost_init: performs the MTU2 initialization

```
MTU21.TCR.BYTE = 0x20;            => CCLR = 0x1;
                                  => TCNT cleared by TGRA compare match/input capture
                                  => CKEG = 0x0;  Count at rising edge
                                  => TPSC = 0x0;  Internal clock: counts on Pφ/1
MTU21.TMDR.BIT.MD = 0x3;          => PWM mode 2
MTU21.TIOR.BIT.IOA = 0x00;
MTU21.TIOR.BIT.IOB = 0x05;        => Initial output is 1. 0 output at compare match

MTU21.TGRA = 0x1F4;
MTU21.TGRB = 0x001;
MTU21.TCNT = 0x0000;

MTU22.TCR.BYTE = 0x20;            => CCLR = 0x1;
                                  => TCNT cleared by TGRA compare match/input capture
                                  => CKEG = 0x0;  Count at rising edge
                                  => TPSC = 0x0;  Internal clock: counts on Pφ/1

MTU22.TMDR.BIT.MD = 0x3;          => PWM mode 2
MTU22.TIOR.BIT.IOA = 0x00;
MTU22.TIOR.BIT.IOB = 0x05;        => Initial output is 1. 0 output at compare match
MTU22.TGRA = 0x1F4;
MTU22.TGRB = 0x001;
MTU22.TCNT = 0x00FA;
ADC0.ADCR.BIT.ADCS=0x0;           => 0: Single-cycle scan
ADC0.ADANSR.BIT.ANS0=0x1;         => AD0 is used as analog input channel
ADC0.ADBYPSCR.BIT.SH=0x1;         => Turn on the sample and hold function
MTU21.TIER.BIT.TGIEA = 0x01;
MTU22.TIER.BIT.TGIEB = 0x01;
INTC.IPR09.WORD = 0x0010;         => Interrupt Priority
PFC.PCCRL3.BIT.PC11MD = 0x4;      => 100: TIOC1B I/O (MTU2)
PFC.PECRL2.BIT.PE7MD  = 0x4;      => 100: TIOC2B I/O (MTU2)
```

The figure 5 shows the flow chart of the operations performed by the software.

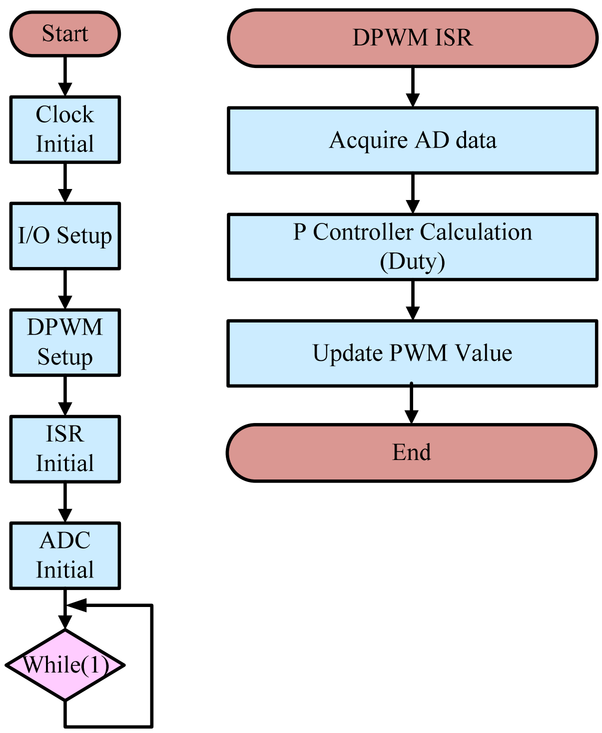

Figure 5 Flow chart for Step-Up Boost

6. Experimental Results

Figure 6 and Figure 7 show the experimental results at full load and half load

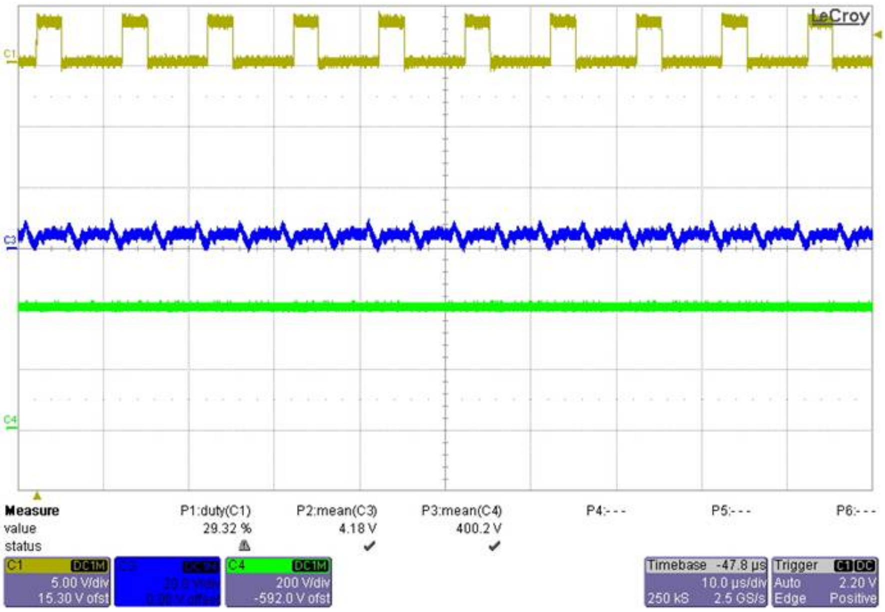

Figure 6 Output power is 108 W at 0.25 A

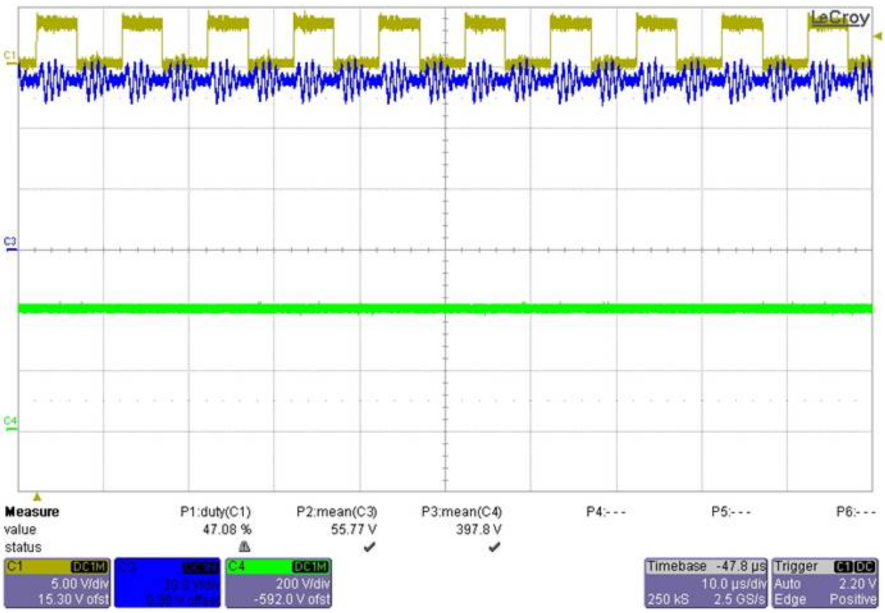

Figure 7 Output power is 1400 W at 3.5 A

Ch1 : Gate signal (5 V/div)

Ch3 : Input current(20 A/div)

Ch4 : *Vbus* (200 V/div)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.30.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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