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SH7145 Group

A/D Conversion in Single Mode

Introduction

A/D conversion (single mode) is performed on the signal on analog input channel 0 (AN0). The converted data is stored to RAM.

Target Device

SH7145F

Contents

1. Specifications

The A/D converter of the SH7145 is used to perform A/D conversion in single mode.

As shown in figure 1, A/D conversion is performed three times using analog input channel 0 (AN0), and the converted data are stored to RAM.

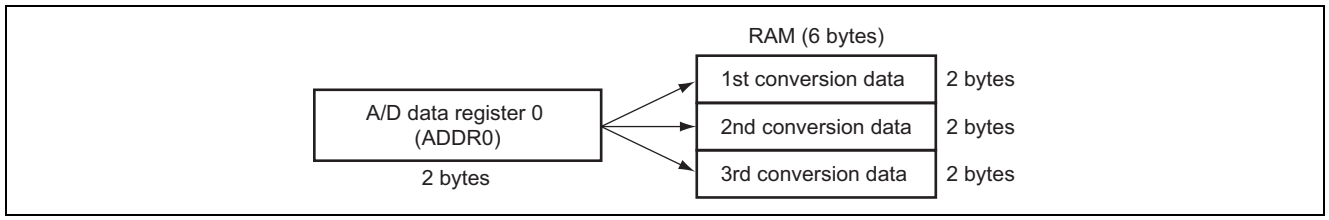


Figure 1 Storage of A/D-Converted Data

2. Description of Functions

In this sample task, channel 0 (ch0) of the A/D converter is used to perform A/D conversion.

2.1 A/D Converter

This is a 10-bit successive approximation A/D converter. Figure 2 shows a block diagram of the A/D converter; below, the converter functions are explained.

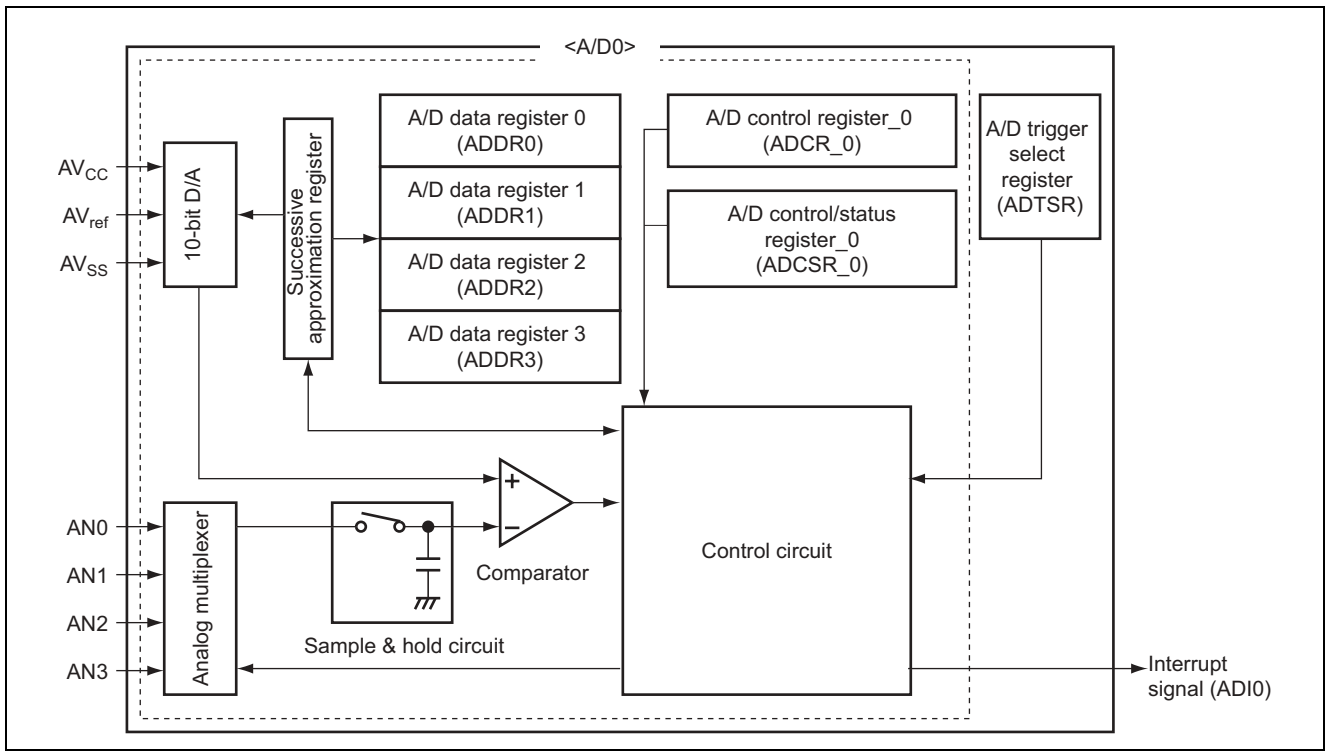


Figure 2 Block Diagram of A/D Converter (ch0)

- The A/D data registers (ADDR0 to ADDR3) are 16-bit read-only registers which store the results of conversion for the corresponding analog input channels. The converted data is stored in bits 15 to 6 of ADDR, and the lowermost 6 bits are always 0.
- The A/D control register_0 (ADCR_0) controls starting of A/D conversion and selects the operating clock.
- The A/D control/status register_0 (ADCSR_0) controls A/D conversion operation.
- The A/D trigger select register (ADTSR) enables starting of A/D conversion by an external trigger.

3. Principles of Operation

Figure 3 shows the A/D conversion timing in single mode and table 1 shows the A/D conversion times. Table 2 describes the software and hardware processing performed for A/D conversion.

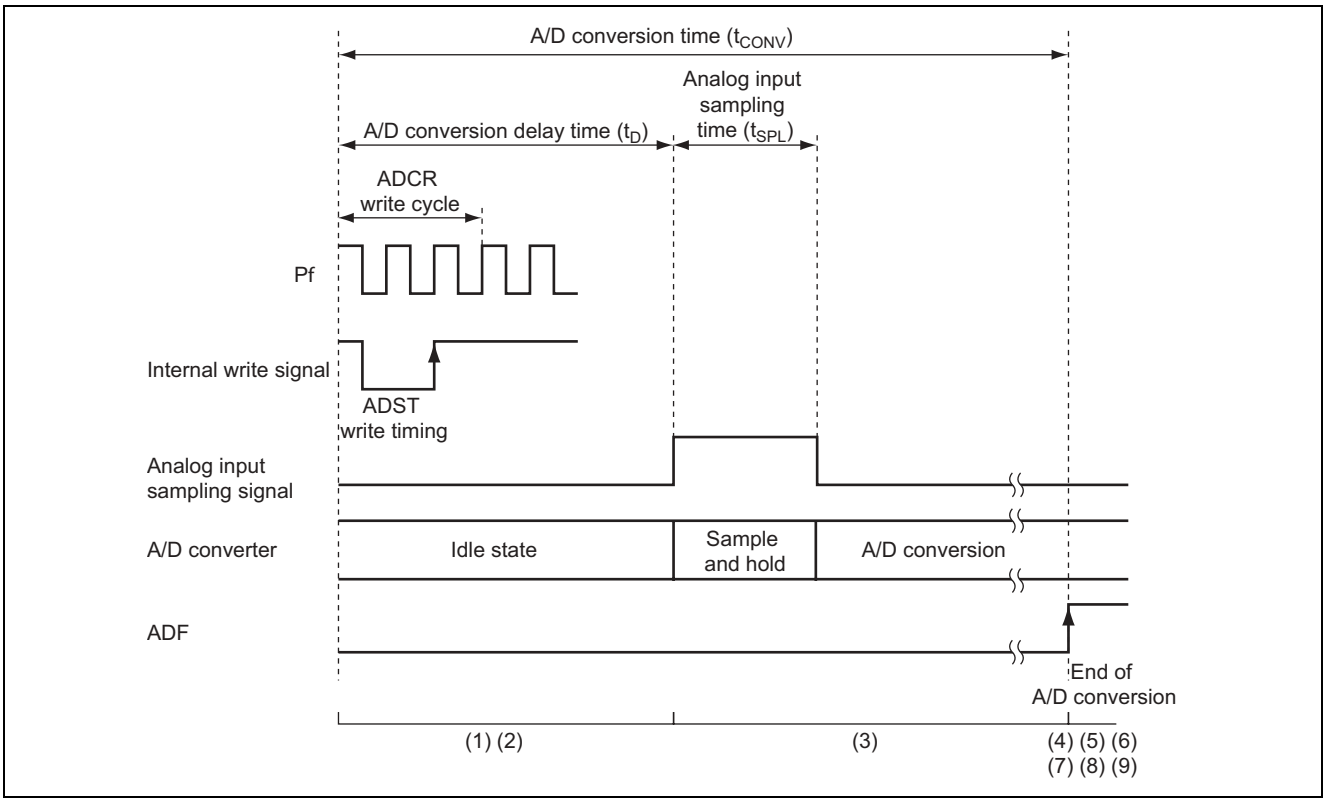


Figure 3 A/D Conversion Timing

Table 1 A/D Conversion Time

		CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**min**	**Typ**	**max**	**min**	**Typ**	**max**	**min**	**Typ**	**max**	**min**	**Typ**	**max**
A/D-conversion-start delay time	t_D	34	—	65	18	—	33	10	—	17	6	—	9
Input sampling time	t_{SPL}	—	256	—	—	128	—	—	64	—	—	32	—
A/D conversion time	t_{CONV}	1024	—	1055	515	—	530	259	—	266	131	—	134

Note: The values in the table are the number of Pϕ clock cycles.

Table 2 Description of Processing

No.	Software Processing	Hardware Processing
(1)	Set ADCSR_0 and ADSR_0 to select a mode, channel, clock, etc.	—
(2)	Set the ADST bit in ADCR_0 to 1.	Start A/D conversion on the specified input channel
(3)	—	Sample the analog input signal and execute A/D conversion.
(4)	—	Set ADF flag in ADCSR_0 to 1 after completion of A/D conversion.
(5)	Store the data in ADDR0 to RAM.	—
(6)	Clear the ADF flag in ADCSR_0 to 0.	—
(7)	Set the ADST bit in ADCR_0 to 1	Start A/D conversion on the specified input channel.
(8)	Repeat steps (3) through (7) above.	Repeat steps (3) through (7) above.

4. Description of Software

4.1 Modules

Table 3 describes the modules used in this sample task.

Table 3 Description of Modules

Module Name	Label Name	Function
Main routine	main	Initializes A/D0 and calls A/D conversion routine.
A/D conversion routine	ad_conv	Starts A/D conversion and stores the results of conversion to RAM.

4.2 Internal Registers

Table 4 describes the internal registers used in this sample task. The setting values are the values used in this sample task and differ from the initial values.

Table 4 Description of Internal Registers

Register Name	Bit	Bit Name	Setting	Function
MSTCR2				Module standby control register 2
	4	MSTP4	0	A/D0 Standby Control When MSTP4 = 0, the standby state of A/D0 is cancelled.
ADCSR_0				A/D control/status register 0
	7	ADF	*[1]	A/D End Flag Set to 1 when A/D conversion ends.
	6	ADIE	0	A/D Interrupt Enable When ADIE = 1, A/D conversion end interrupt is enabled.
	5	—	0	Reserved
	4	ADM	0	A/D Mode Select When ADM = 0, A/D converter operates in single mode.
	3	—	1	Reserved
	2	—	0	Reserved
	1	CH1	0	Channel Select 1, 0
	0	CH0	0	Select analog input channel for A/D conversion.

Register Name	Bit	Bit Name	Setting	Function
ADCR_0				A/D control register_0
	7	TRGE	0	Trigger Enable When TRGE = 0, A/D conversion triggering is disabled.
	6	CKS1	0	Clock Select 1, 0
	5	CKS0	0	Set A/D conversion time (in this sample task, Pϕ/32).
	4	ADST	*2	A/D Start Setting ADST to 1 starts A/D conversion.
	3	ADCS	1	A/D Continuous Scan This bit is invalid in this sample task because A/D conversion is performed in single scan mode.
	2	—	1	Reserved
	1		1	
	0		1	
ADDR0			—	A/D data register 0 Stores the results of A/D conversion.

Notes: 1. Only 0 can be written to this bit for clearing; this bit is automatically set by hardware.
2. This bit is automatically cleared to 0 when A/D conversion ends.

4.3 RAM Usage

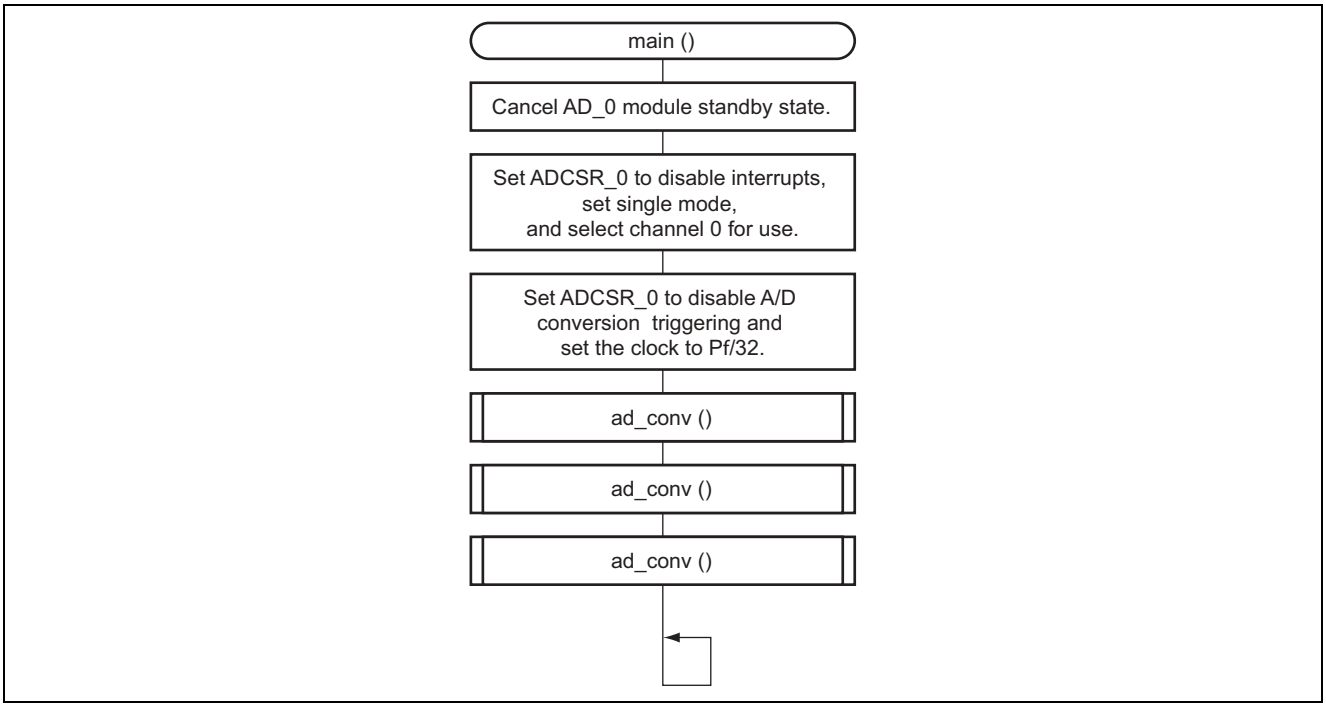
Table 5 describes the RAM usage in this sample task.

Table 5 Description of RAM

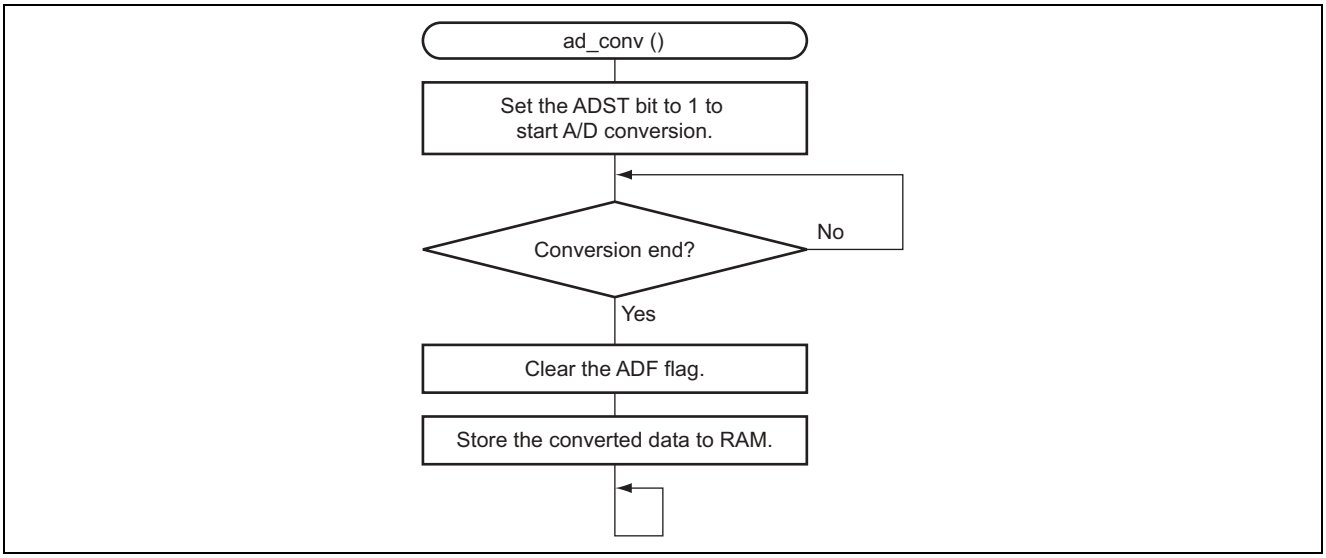
Label Name	Function	Address	Used in
Ad_data[0-2]	Array for storing A/D converted data (2 bytes/data)	On-chip RAM	A/D conversion routine

5. Flowchart

5.1 Main Routine



5.2 A/D Conversion Routine



6. Program Listing

```
/************************************************************************************************/
/* SH7145F Application Note                                                                     */
/*                                                                                              */
/* Function                                                                                     */
/*    :AD0(Single Mode)                                                                         */
/*                                                                                              */
/* External input clock         :12.5MHz                                                        */
/* Internal CPU clock           :50MHz                                                          */
/* Internal peripheral clock    :25MHz                                                          */
/*                                                                                              */
/* Written        2003/10        Rev.1.0                                                        */
/************************************************************************************************/

#include "iodefine.h"
#include <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
#define AD_COUNT 3

/************************************************************************************************/
/*  Function Define                                                                             */
/************************************************************************************************/
void main(void);
void ad_conv(void);

void dummy_f(void);

/************************************************************************************************/
/*  RAM Allocation Definition                                                                   */
/************************************************************************************************/
unsigned short Ad_data[AD_COUNT];
unsigned char count;
```

```
/*****************************************************************************************************/
/*  Main Program                                                                                     */
/*****************************************************************************************************/
void main(void)
{
    count = 0;

    P_STBY.MSTCR2.BIT.MSTP4 = 0;                    /* Disable AD0 standby mode                 */
    P_AD.ADCSR_0.BYTE |= 0x08;                      /* Set ADCSR_0                              */
                //[7]  = 0;ADF
                //[6]  = 0;A/D interrupt disable
                //[5]  = 0;reserve
                //[4]  = 0;single mode
                //[3]  = 1;reserve
                //[2]  = 0;reserve
                //[1]  = 0
                //[0]  = 0;channel select AN0

    P_AD.ADCR_0.BYTE |= 0x00;                       /* Set ADCR_0                               */
                //[7]  = 0;trigger disable
                //[6]  = 0
                //[5]  = 0;clock PƒÓ/32
                //[4]  = 0;wait conversion
                //[3]  = 0;single mode
                //[2]  = 1;reserve
                //[1]  = 1;reserve
                //[0]  = 1;reserve

    ad_conv();
    ad_conv();
    ad_conv();

    while(1);                                       /* LOOP                                     */
}
```

```
/*****************************************************************************************/
/* Functon Name                : ad_conv                                                 */
/* Operation of the function   : Sets ADST (to start A/D conversion),                    */
/*                               clears ADF flag, and stores converted data to RAM       */
/* Arguments                   : None                                                    */
/* Return value                : None                                                    */
/*****************************************************************************************/
/*****************************************************************************************/
void ad_conv(void)
{
    P_AD.ADCR_0.BIT.ADST = 1;                   /* Start AD converter                    */

    while(P_AD.ADCSR_0.BIT.ADF == 0);           /* Waits till a conversion end           */

    P_AD.ADCSR_0.BIT.ADF = 0;                   /* Clear ADF flag                        */

    Ad_data[count] = P_AD.ADDR0.WORD;           /* Store AD(AN0) data                    */
    count++;
}
/*****************************************************************************************/
/*  Interruption Program                                                                 */
/*****************************************************************************************/
#pragma interrupt(dummy_f)
void dummy_f(void)
{
    /* Other Interrupt */
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.16.04	—	First edition issued

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