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H8/300L SLP Series

Setting Up Module-Standby Mode (H8/3867)

Introduction

Setting method: The module standby is a function to stop supplying a system clock to modules, and to stop module functions. Module standby mode can be set for each peripheral function. All incorporated peripheral modules can be set to module standby mode.

Target Device

H8/3867

Contents

1. Functions used: Module standby mode

Setting method: The module standby is a function to stop supplying a system clock to modules, and to stop module functions. Module standby mode can be set for each peripheral function. All incorporated peripheral modules can be set to module standby mode.

1.1 Setting of Module Standby Mode

The module standby mode is set by setting each bit in both the clock stop register 1 (CKSTPR1) and the clock stop register 2 (CKSTPR2) to 0.

1.2 Cancellation of Module Standby Mode

The module standby mode is cancelled by setting each bit in the clock stop register 1 (CKSTPR1) and the clock stop register 2 (CKSTPR2) to 1.

Note that immediately after being reset, both CKSTPR1 and CKSTPR2 are initialized to H'FF.

1.3 Register Descriptions of CKSTPR1 and CKSTPR2

Table 1.1 shows register descriptions of CKSTPR1 and CKSTPR2.

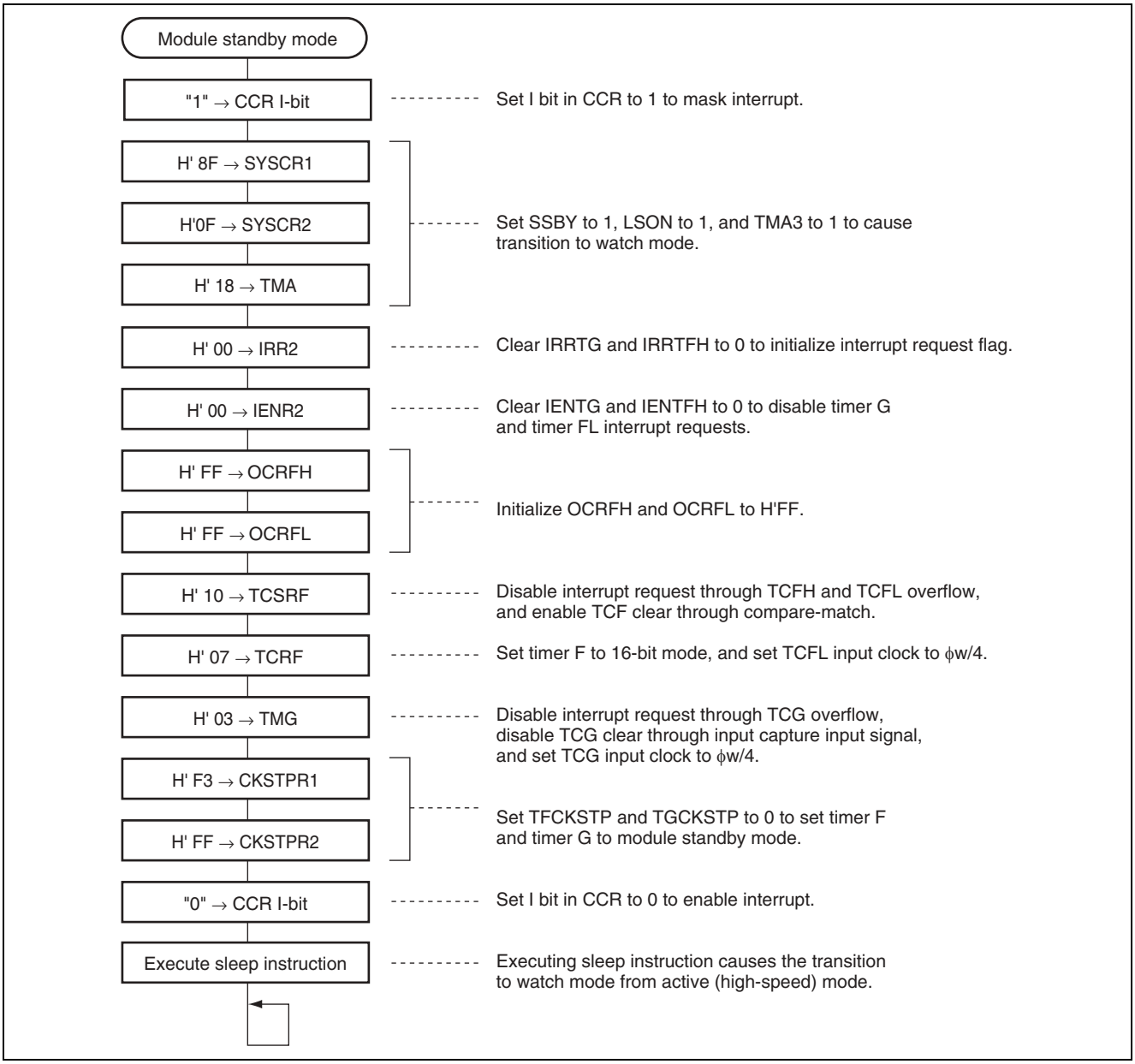
Table 1.1 Register Descriptions of CKSTPR1 and CKSTPR2

Register Name	Bit	Bit Name	Setting	Description
CKSTPR1	Bit 6	S31CKSTP	0	Set SCI3 to SCI1 to module standby mode
			1	Cancel SCI3 to SCI1module standby mode
	Bit 5	S32CKSTP	0	Set SCI3 and SCI2 to module standby mode
			1	Cancel SCI3 and SCI2module standby mode
	Bit 4	ADCKSTP	0	Set A/D converter to module standby mode
			1	Cancel A/D converter module standby mode
	Bit 3	TGCKSTP	0	Set timer G to module standby mode
			1	Cancel timer G module standby mode of
	Bit 2	TFCKSTP	0	Set timer F to module standby mode
			1	Cancel timer F module standby mode
	Bit 1	TCCKSTP	0	Set timer C to module standby mode
			1	Cancel timer C module standby mode
	Bit 0	TACKSTP	0	Set timer A to module standby mode
			1	Cancel timer A module standby mode
CKSTPR2	Bit 3	AECKSTP	0	Set AEC to module standby mode
			1	Cancel AEC module standby mode
	Bit 2	WDCKSTP	0	Set WDT to module standby mode
			1	Cancel WDT module standby mode
	Bit 1	PWCKSTP	0	Set PWM to module standby mode
			1	Cancel PWM module standby mode
	Bit 0	LDCKSTP	0	Set LCD to module standby mode
			1	Cancel LCD module standby mode

1.4 Module Standby Mode Setting Example

1. Function
   This is an example for setting the timer F and the timer G to module standby mode during active (high-speed) mode and causing a transition to watch mode.
2. Cautions
   A. Only when an external clock is selected as an input clock for the timer F and the timer G, or when ϕw/4 is selected as an internal clock, this LSI operates even in watch mode. When any other clocks are selected, this LSI stops its operation in watch mode. Accordingly, in this setting, setting ϕw/4 as the input clock for the timer F and timer G followed by setting the timer F and timer G to module standby mode allows transition to watch mode.
   B. Since all interrupt requests are prohibited in this setting example, when transiting to watch mode, the watch mode can be cancelled only through a RES pin input.

2 Flowchart


Module standby mode
"1" → CCR I-bit
Set I bit in CCR to 1 to mask interrupt.
H' 8F → SYSCR1
H'0F → SYSCR2
H' 18 → TMA
Set SSBY to 1, LSON to 1, and TMA3 to 1 to cause transition to watch mode.
H' 00 → IRR2
Clear IRRTG and IRRTFH to 0 to initialize interrupt request flag.
H' 00 → IENR2
Clear IENTG and IENTFH to 0 to disable timer G and timer FL interrupt requests.
H' FF → OCRFH
H' FF → OCRFL
Initialize OCRFH and OCRFL to H'FF.
H' 10 → TCSRF
Disable interrupt request through TCFH and TCFL overflow, and enable TCF clear through compare-match.
H' 07 → TCRF
Set timer F to 16-bit mode, and set TCFL input clock to ϕw/4.
H' 03 → TMG
Disable interrupt request through TCG overflow, disable TCG clear through input capture input signal, and set TCG input clock to ϕw/4.
H' F3 → CKSTPR1
H' FF → CKSTPR2
Set TFCKSTP and TGCKSTP to 0 to set timer F and timer G to module standby mode.
"0" → CCR I-bit
Set I bit in CCR to 0 to enable interrupt.
Execute sleep instruction
Executing sleep instruction causes the transition to watch mode from active (high-speed) mode.

3. Program listing

```
;*****************************************************************************
;*     H8/3867 Application Note                                              *
;*                                                                           *
;*    'Module Standby Mode                                                   *
;*    -In Watch Mode, Timer F&G Module Standby Mode Set                      *
;*                                                                           *
;*     Function : Module Standby Mode                                        *
;*                                                                           *
;*     External Clock : 6MHz                                                 *
;*     Internal Clock : 3MHz                                                 *
;*     Sub Clock      : 32.768kHz                                            *
;*****************************************************************************
;
          .cpu         300L
;
;*****************************************************************************
;*  Symbol Defnition                                                         *
;*****************************************************************************
;
TMA       .equ         h'ffb0        ;Timer Mode Register A
TCRF      .equ         h'ffb6        ;Timer Control Register F
TCSRF     .equ         h'ffb7        ;Timer Control/Status Register F
OCRFH     .equ         h'ffba        ;Output Compare Register FH
OCRFL     .equ         h'ffbb        ;Output Compare Register FL
TMG       .equ         h'ffbc        ;Timer Mode Register G
SYSCR1    .equ         h'fff0        ;System Control Register 1
SYSCR2    .equ         h'fff1        ;System Control Register 2
IENR2     .equ         h'fff4        ;Interrupt Enable Register 2
IRR2      .equ         h'fff7        ;Interrupt Request Register 2
CKSTPR1   .equ         h'fffa        ;Clock Stop Register 1
CKSTPR2   .equ         h'fffb        ;Clock Stop Register 2
;
;*****************************************************************************
;*  Vector Address                                                           *
;*****************************************************************************
;
          .org         h'0000
          .data.w      MAIN          ;No.0 Reset Interrupt(H'0000-H'0001)
;
          .org         h'0008
          .data.w      MAIN          ;No.4 _IRQ0 Interrupt(H'0008-H'0009)
          .data.w      MAIN          ;No.5 _IRQ1 Interrupt(H'000A-H'000B)
          .data.w      MAIN          ;No.6 _IRQ2 Interrupt(H'000C-H'000D)
          .data.w      MAIN          ;No.7 _IRQ3 Interrupt(H'000E-H'000F)
          .data.w      MAIN          ;No.8 _IRQ4 Interrupt(H'0010-H'0011)
          .data.w      MAIN          ;No.9 _WKP0-_WKP7 Interrupt(H'0012-H'0013)
;
          .org         h'0016
          .data.w      MAIN          ;No.11 Timer A Interrupt(H'0016-H'0017)
          .data.w      MAIN          ;No.12 AEC Interrupt(H'0018-H'0019)
          .data.w      MAIN          ;No.13 Timer C Interrupt(H'001A-H'001B)
          .data.w      MAIN          ;No.14 Timer FL Interrupt(H'001C-H'001D)
          .data.w      MAIN          ;No.15 Timer FH Interrupt(H'001E-H'001F)
          .data.w      MAIN          ;No.16 Timer G Interrupt(H'0020-H'0021)
          .data.w      MAIN          ;No.17 SCI31 Interrupt(H'0022-H'0023)
          .data.w      MAIN          ;No.18 SCI32 Interrupt(H'0024-H'0025)
```

```
          .data.w     MAIN          ;No.19 A/D Converter Interrupt(H'0026-H'0028)
          .data.w     MAIN          ;No.20 Direct Transfer Interrupt(H'0028-H'0029)
;
;*************************************************************************************
;*  MAIN : Main Routine                                                              *
;*************************************************************************************
;
          .org        h'1000
;
MAIN:     .equ        $
          mov.w       #h'ff80,sp    ;Initialize Stack Pointer
          orc         #h'80,ccr     ;Interrupt Disable
;
          mov.w       #h'8ff0,r0    ;Initialize System Control Regsiter
          mov.b       r0h,@SYSCR1
          mov.b       r0l,@SYSCR2
          mov.b       #h'18,r0l     ;Initialize Timer Mode Register
          mov.b       r0l,@TMA
;
          sub.b       r0l,r0l       ;Initialize Timer F
          mov.b       r0l,@IRR2
          mov.b       r0l,@IENR2
          mov.b       #h'ff,r0l
          mov.b       r0l,@OCRFH
          mov.b       r0l,@OCRFL
          mov.b       #h'10,r0l
          mov.b       r0l,@TCSRF
          mov.b       #h'07,r0l
          mov.b       r0l,@TCRF
;
          mov.b       #h'03,r0l     ;Initialize Timer G
          mov.b       r0l,@TMG
;
          mov.w       #h'f3ff,r0    ;Timer F & G Module Standby Mode ON
          mov.b       r0h,@CKSTPR1
          mov.b       r0l,@CKSTPR2
;
          andc        #h'7f,ccr     ;Interrupt Enable
;
          sleep                     ;Transfer to Watch Mode
          nop
;
EXIT:     bra         EXIT
;
          .end
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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