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R32C/100 Series

Serial Interface Operation (Transmitting in Asynchronous Serial Interface Mode)

1. Abstract

This document describes an example of the setting procedure for transmitting in the asynchronous serial interface mode (UART mode) using an arbitrary bit rate and data format.

2. Introduction

The application example described in this document applies to the following MCU:

•MCU: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/111 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

This section describes how to transmit data at a bit rate of 9600bps (Xin = 16 MHz, PLL clock = 100 MHz and actual bit rate = 9586bps) using asynchronous serial interface mode.
Table 3.1 lists specifications of asynchronous serial interface mode.

Table 3.1 Setting Conditions for Transmiting Data Using Asynchronous Serial Interface Mode

Item	Setting
Bit rate	9600bps
Character length	8 bit-length
Parity	Odd
Stop bit length	1 bit-length
Transmit/receive clock	Internal clock
Receive control	CTS
Bit order	LSB first
Transmit interrupt request generating timing	When transmission is complete

The following is the formula for calculating the actual bit rate.

$$\text{Actual bit rate} = \frac{\text{UiBRG register (i = 0 to 6) count source}}{16 \times (\text{UiBRG register value} + 1)}$$

Table 3.2 lists examples of bit rate settings.

Table 3.2 Bit Rate Setting Examples

Target Bit Rate (bps)	Count Source of UiBRG	PLL Clock: 96 MHz		PLL Clock: 100 MHz		PLL Clock: 120 MHz		PLL Clock: 128 MHz	
		Peripheral Clock: 24 MHz		Peripheral Clock: 25 MHz		Peripheral Clock: 30 MHz		Peripheral Clock: 32 MHz	
		Setting value of UiBRG	Actual bit rate (bps)	Setting value of UiBRG	Actual bit rate (bps)	Setting value of UiBRG	Actual bit rate (bps)	Setting value of UiBRG	Actual bit rate (bps)
1200	f8	155(9Bh)	1202	162(A2h)	1198	194(C2h)	1202	207(CFh)	1202
2400	f8	77(4Dh)	2404	80(50h)	2411	97(61h)	2392	103(67h)	2404
4800	f8	38(26h)	4808	40(28h)	4764	48(30h)	4783	51(33h)	4808
9600	f1	155(9Bh)	9615	162(A2h)	9586	194(C2h)	9615	207(CFh)	9615
14400	f1	103(67h)	14423	108(6Ch)	14335	129(81h)	14423	138(8Ah)	14388
19200	f1	77(4Dh)	19231	80(50h)	19290	97(61h)	19133	103(67h)	19231
28800	f1	51(33h)	28846	53(35h)	28935	64(40h)	28846	68(44h)	28986
31250	f1	47(2Fh)	31250	49(31h)	31250	59(3Bh)	31250	63(3Fh)	31250
38400	f1	38(26h)	38462	40(28h)	38109	48(30h)	38265	51(33h)	38462
51200	f1	28(1Ch)	51724	30(1Eh)	50403	36(24h)	50676	38(26h)	51282

In this application note, the TXD output is used for transmitting data. To output the TXD in the R32C/111 Group, set the direction bits and the function select registers for the TXD pin.
Table 3.3 lists the TXD Pin, Port Direction Bit and Function Select Register Settings.

Table 3.3 TXD Pin, Port Direction Bit and Function Select Register Settings

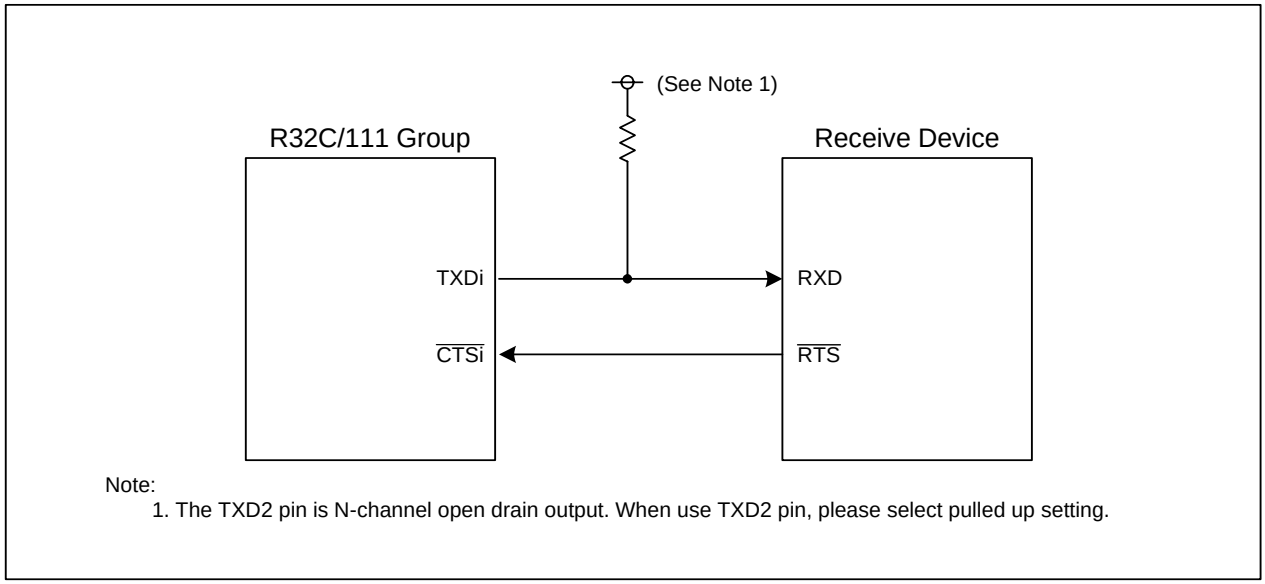
Channel	Pin	Port	Port Direction Bit	Setting Value	Function Select Register	Setting Value
UART0	TXD0	P6_3	PD6_3	1	P6_3S	03h
UART1	TXD1	P6_7	PD6_7	1	P6_7S	03h
UART2	TXD2	P7_0 (1)	PD7_0	1	P7_0S	03h
UART3	TXD3	P4_3	PD4_3	1	P4_3S	03h
UART4	TXD4	P9_6	PD9_6 (2)	1	P9_6S(2)	03h
UART5	TXD5	P7_6	PD7_6	1	P7_6S	03h
UART6	TXD6	P4_7	PD4_7	1	P4_7S	03h

Notes:
1. N-channel open drain output.
2. Set the PRC2 bit in the PRCR register to 1 (write enabled) just before rewriting this register. Do not generate any interrupts or DMA transfers between setting the PRC2 bit to 1 and rewriting this register.

3.1 Data Transmission in Asynchronous Serial Interface Mode

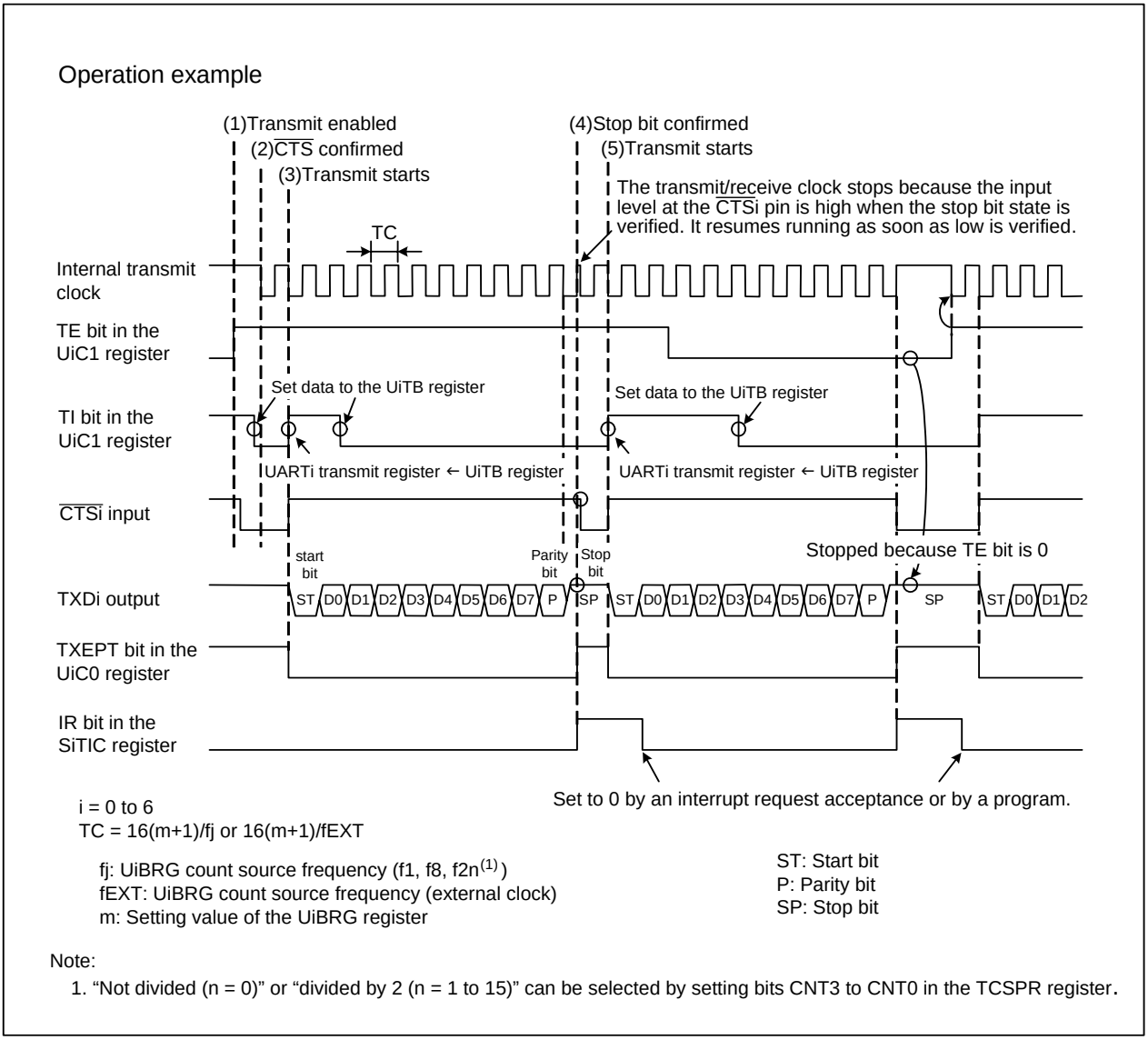
1)When transmit data is written to the UiTB register (i = 0 to 6) after setting the TE bit in the UiC1 register to 1 (transmission enabled), a transmission wait state is entered.
2)Transmission starts when the input signal to the $\overline{\text{CTSi}}$ pin goes low. (The input signal to the $\overline{\text{CTSi}}$ pin is controlled by a device on the receive side.
3)The transmit data written in the UiTB register is transferred to the UARTi transmit register. Simultaneously, the first bit of transmit data (start bit) is transmitted from the TXDi pin. Then the remaining data is transmitted bit by bit in the following order: data bit (LSB) through data bit (MSB), parity bit and stop bit.
4)After the stop bit has been transmitted, the TXEPT bit in the UiC0 register becomes 1 (no data held in the transmit shift register), indicating that the transmission is completed. Simultaneously, IR bit in the SiTIC register becomes 1 (interrupt requested).
5)If the next data transmission conditions are satisfied after transmission is completed, the next data is transmitted after the stop bit .

Figure 3.1 shows a Connection Example for Transmission, and Figure 3.2 shows the Transmit Operation Timing.



Note:
1. The TXD2 pin is N-channel open drain output. When use TXD2 pin, please select pulled up setting.

Figure 3.1 Connection Example for Transmission



Note:
1. “Not divided (n = 0)” or “divided by 2 (n = 1 to 15)” can be selected by setting bits CNT3 to CNT0 in the TCSPR register.

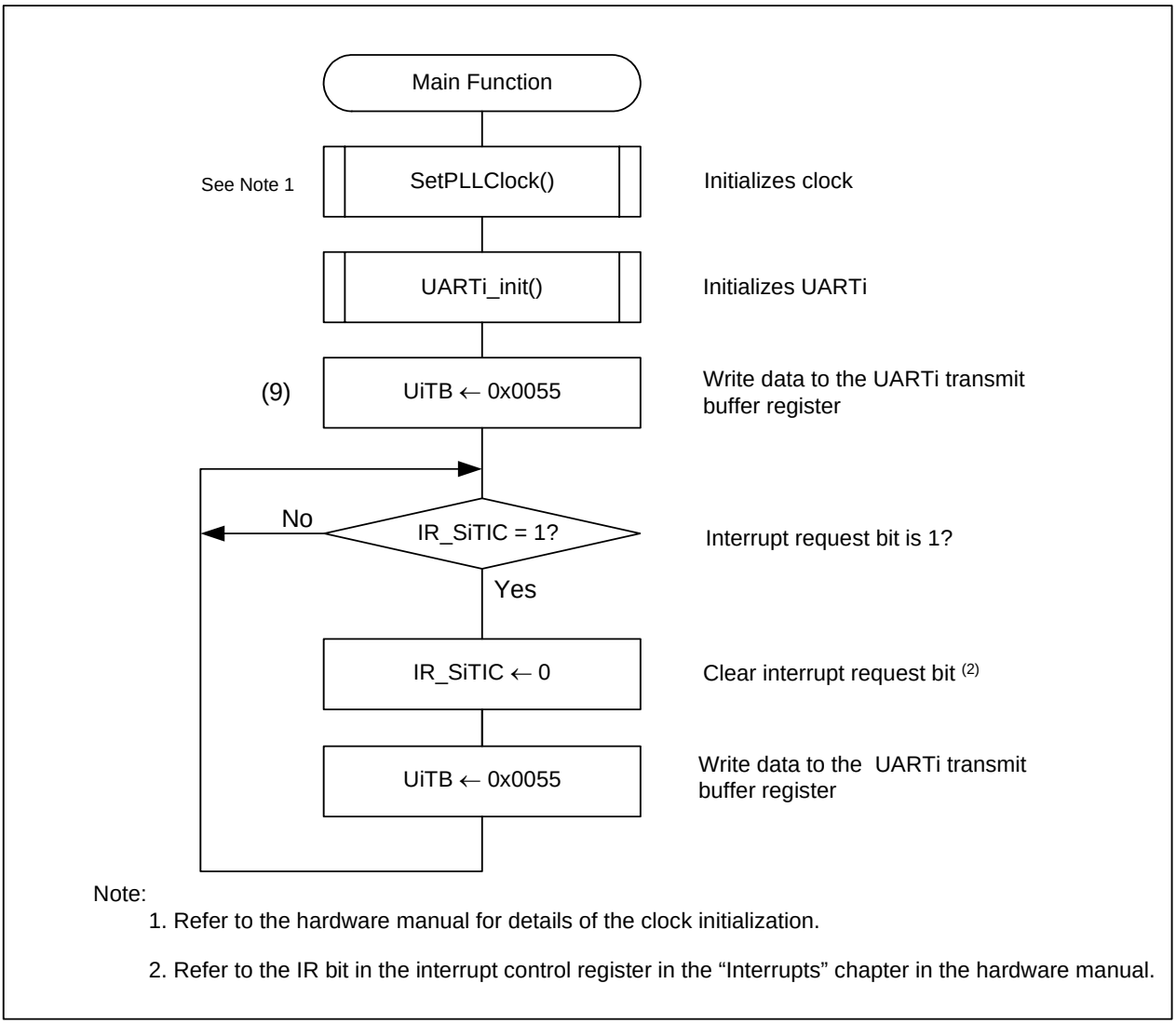
Figure 3.2 Transmit Operation Timing

3.2 Settings

This section describes the procedure and values to execute the examples shown in section 3.1 “Data Transmission in Asynchronous Serial Interface Mode”. For details on each register, refer to hardware manual.

In the sample program, data can be transmitted by initializing the UARTi (i = 0 to 6). Transmission starts by writing the transmit data to the UARTi transmit buffer register. When the program detects that the UARTi transmit interrupt interrupt-request bit becomes 1 (interrupt requested), set the interrupt request bit to 0 and write the next transmit data in the transmit buffer register.

Figure 3.3 shows the main Processing Transmission Flowchart (i = 0 to 6) and Figure 3.4 shows the UARTi Initialization Process Flowchart (i = 0 to 6).



Note:

1. Refer to the hardware manual for details of the clock initialization.
2. Refer to the IR bit in the interrupt control register in the “Interrupts” chapter in the hardware manual.

Figure 3.3 main Processing Transmission Flowchart (i = 0 to 6)

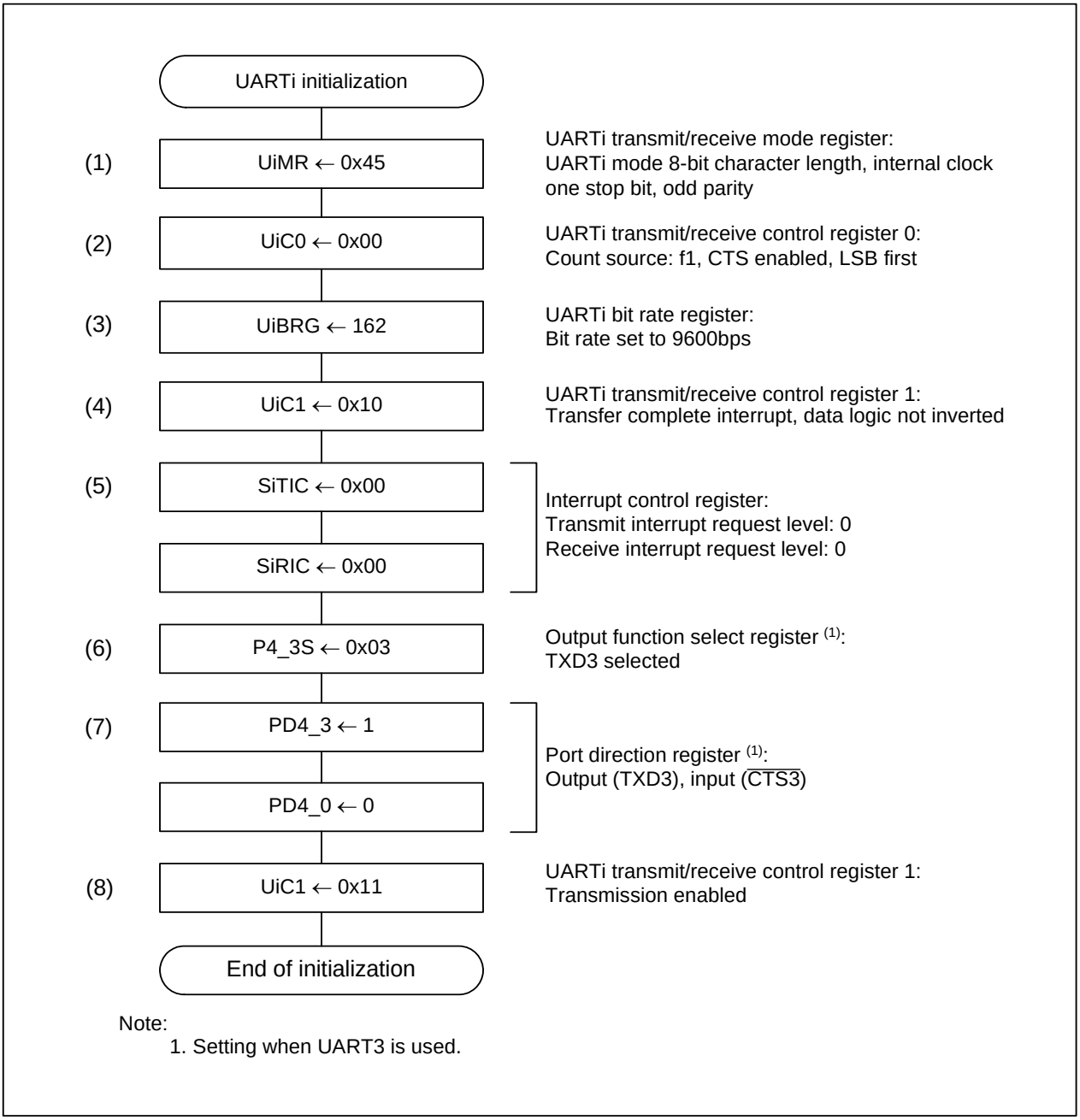
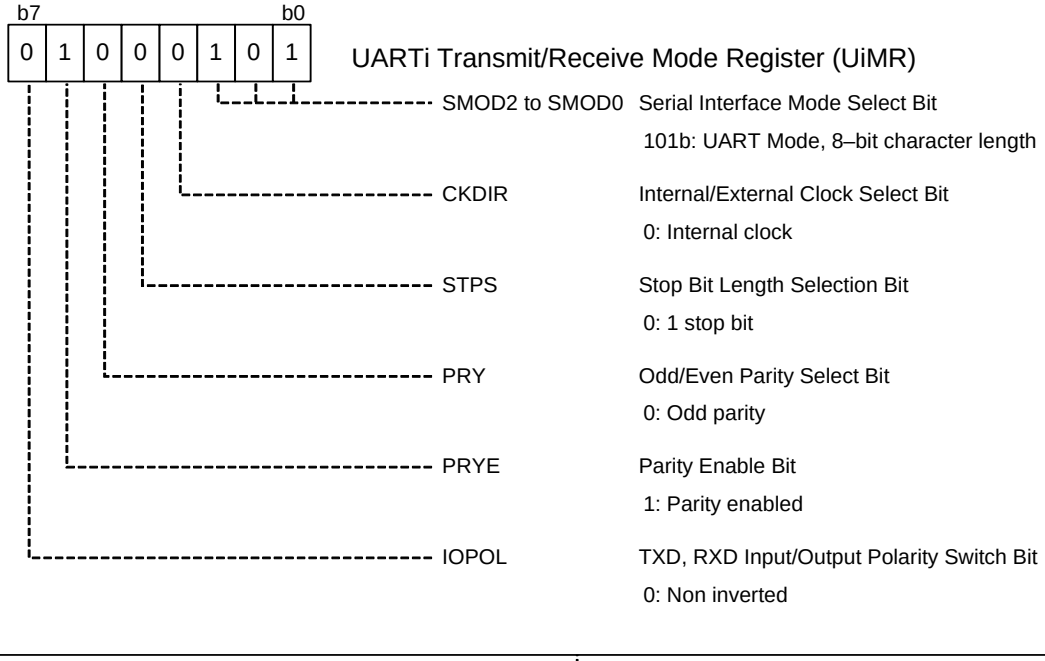


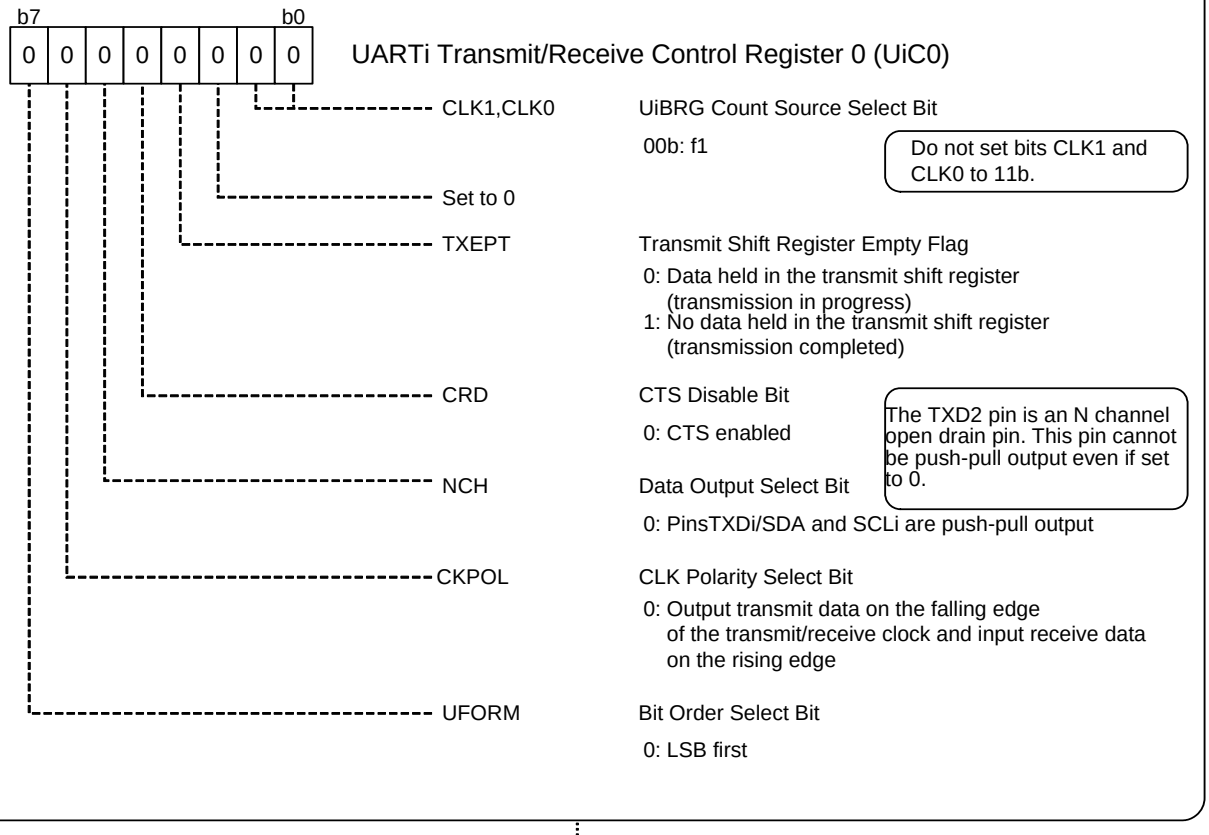
Figure 3.4 UARTi Initialization Process Flowchart (i = 0 to 6)

3.3 Detailed Settings

Set the UARTi transmit/receive mode register (i = 0 to 6).



Set the UARTi transmit/receive control register 0.



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Set UARTi bit rate register (i = 0 to 6).

b7							b0
162							

UARTi bit rate register (UiBRG)

The UiBRG register divides the count source by n+1 (n = setting value)

162: Divided-by-163

Set UARTi transmit/receive control register 1.

b7							b0
0	0	0	1	0	0	0	0

UARTi Transmit/Receive Control Register 1 (UiC1)

TE — Transmit Enable Bit
0: Transmission disabled

TI — Transmit Buffer Empty Flag
0: Data held in the UiTB register
1: No data held in the UiTB register

RE — Receive Enable Bit
0: Reception disabled

RI — Receive Complete Flag
0: No data held in the UiRB register
1: Data held in the UiRB register

UiIRS — UARTi Transmit Interrupt Source Selection Bit
1: Transmission is completed (TXEPT = 1)

UiRRM — UARTi Continuous Receive Mode Enable Bit
0: Continuous receive mode disabled

UiLCH — Logical Inversion Select Bit
0: Data non logic-inverted

Set to 0

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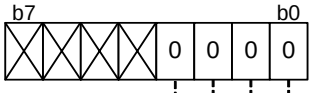
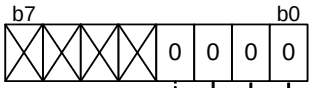
Set the interrupt control register (i = 0 to 6).



UARTi Transmit Interrupt Control Register (SiTIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bits	
	000b: Level 0 (Interrupt disabled)	
IR	Interrupt Request Bit	
	0: No interrupt requested	

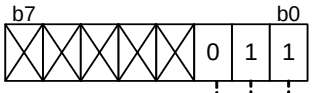


UARTi Receive Interrupt Control Register (SiRIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bits	
	000b: Level 0 (Interrupt disabled)	
IR	Interrupt Request Bit	
	0: No interrupt requested	

Set the function select register

These are the settings when using UART3.

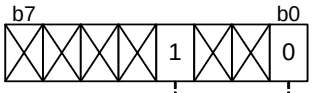


Port P4_3 Function Select Register (P4_3S)

PSEL2 to PSEL0	Port P4_3 Output Function Select Bits	
	011b: TXD3 output	

Set the port direction register .

These are the settings when using UART3.



Port P4 Direction Register (PD4)

PD4_0	Port P4_0 Direction Bit	
	0: Input	
PD4_3	Port P4_3 Direction Bit	
	1: Output	

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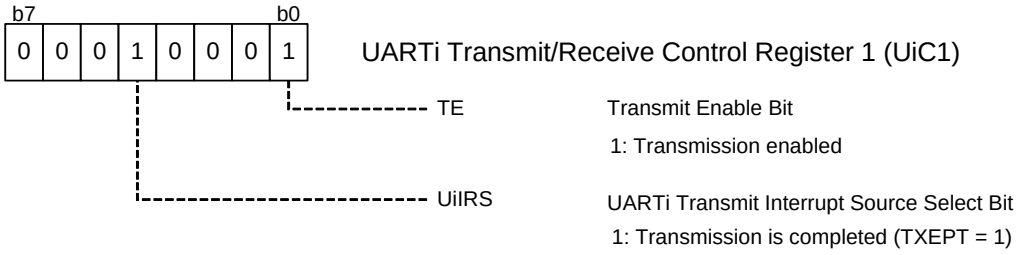
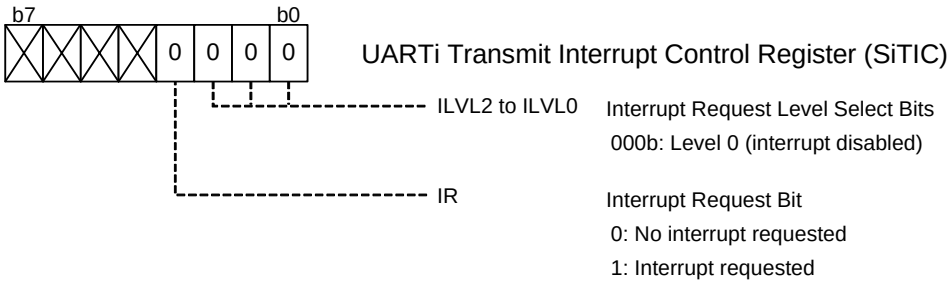
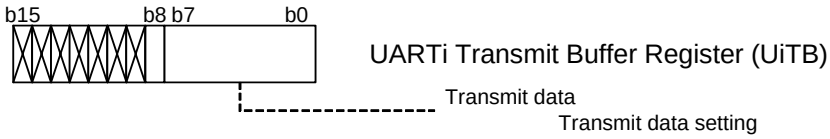
Set the UARTi transmit/receive control register 1 (i = 0 to 6).



Read the interrupt request bit and set the interrupt control register.



Write the transmit data.



4. Sample Programs

A sample program can be downloaded from the Renesas Technology website.

5. Reference Documents

Hardware Manual
R32C/111 Group Hardware Manual Rev.1.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.1.00
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