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R32C/100 Series

Serial Interface Operation (Transmission in Clock Synchronized Serial Interface Mode)

1. Summary

This document describes the procedure and an application example for sending data to external devices synchronized with the transmit/receive clock using clock-synchronized serial interface mode.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

- MCU: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/111 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

This section describes how to transmit data at a bit rate of 500 kbps (XIN = 16 MHz, PLL clock = 100 MHz) using synchronous serial interface mode.

The following shows the formula to calculate the communication rate.

$$\text{Communication rate} = \frac{\text{Transmit/receive clock count source}}{2 \times (\text{UiBRG register setting value} + 1)}$$

Table 3.1 lists specifications of synchronous serious interface mode.

Table 3.1 Setting Conditions for Sending Data in Synchronous Serious Interface Mode

Item	Setting
Character length	8-bit
Transmit/receive clock	Internal clock
Transmit control	CTS function
Bit order	LSB first
Transmit interrupt request generating timing	When data is transferred from the UiTB register to the UARTi transmit register (when transmission has started)
CLK polarity	Transmit data is output on the falling edge of the transmit/ receive clock and receive data is input on the rising edge.
TXD, RXD input/output polarity switch bit	Non inverted

In this application note, CLK and TXD outputs are used for data transmission. To output CLK and TXD in the R32C/111 Group, set the direction bits and the function select registers for the ports corresponding pins CLK and TXD. Table 3.2 lists the Port Direction Bit and Function Select Register Settings for Pins CLK and TXD.

Table 3.2 Port Direction Bit and Function Select Register Settings for Pins CLK and TXD

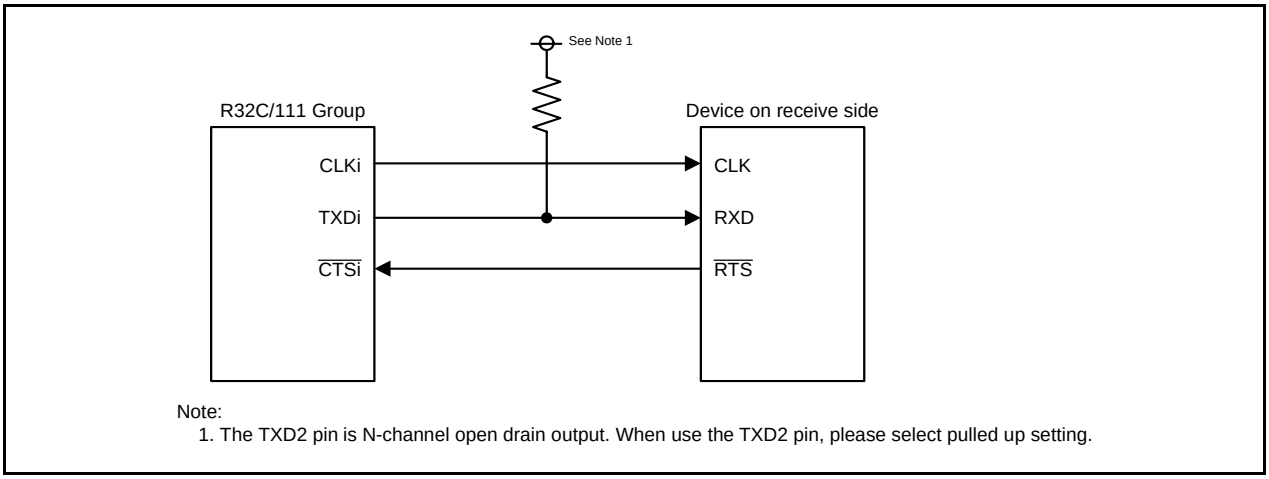
Channel	Pin	Port	Port Direction Bit	Setting Value	Function Select Register	Setting Value
UART0	CLK0	P6_1	PD6_1	1	P6_1S	03h
	TXD0	P6_3	PD6_3	1	P6_3S	03h
UART1	CLK1	P6_5	PD6_5	1	P6_5S	03h
	TXD1	P6_7	PD6_7	1	P6_7S	03h
UART2	CLK2	P7_2	PD7_2	1	P7_2S	03h
	TXD2	P7_0 (1)	PD7_0	1	P7_0S	03h
UART3	CLK3	P4_1	PD4_1	1	P4_1S	03h
	TXD3	P4_3	PD4_3	1	P4_3S	03h
UART4	CLK4	P9_5	PD9_5 (2)	1	P9_5S (2)	03h
	TXD4	P9_6	PD9_6 (2)	1	P9_6S (2)	03h
UART5	CLK5	P7_7	PD7_7	1	P7_7S	03h
	TXD5	P7_6	PD7_6	1	P7_6S	03h
UART6	CLK6	P4_5	PD4_5	1	P4_5S	03h
	TXD6	P4_7	PD4_7	1	P4_7S	03h

Notes:
1. N-channel open drain output
2. Set the PRC2 bit in the PRCR register to 1 (write enabled) just before rewriting this register. Do not generate any interrupts or DMA transfers between setting the PRC2 bit to 1 and rewriting this register.

3.1 Data Transmission in Synchronous Serial Interface Mode

(1) When transmit data is written to the UiTB register (i = 0 to 6) after setting the TE bit in the UiC1 register to 1 (transmission enabled), a transmission wait state is entered.
(2) Transmission starts when the input signal to the $\overline{\text{CTSi}}$ pin goes low. (The input signal to the $\overline{\text{CTSi}}$ pin is controlled by a device on the receive side.)
(3) Synchronously with the first falling edge of transmit/receive clock, the transmit data written to the UiTB register is transferred to the UARTi transmit register. At the same time, the IR bit in the SiTIC register becomes 1 (interrupt requested).
The first low-order of the transmit data is transmitted from the TXDi pin. Then, the second and subsequent bits are transmitted synchronously with the falling edges of the transmit/receive clock.
(4) After 1-byte of data has been transmitted, the TXEPT bit in the UiC0 register becomes 1 (transmission complete), indicating that the transmission is completed.
The transmit/receive clock stops at the high level.
(5) If the UiTB register has the next data loaded in it before the eighth bit of the preceding data is output, transmission is performed continually.

Figure 3.1 shows a Connection Example for Transmission. Figure 3.2 shows the Transmit Operation Timing.



Note:
1. The TXD2 pin is N-channel open drain output. When use the TXD2 pin, please select pulled up setting.

Figure 3.1 Connection Example for Transmission

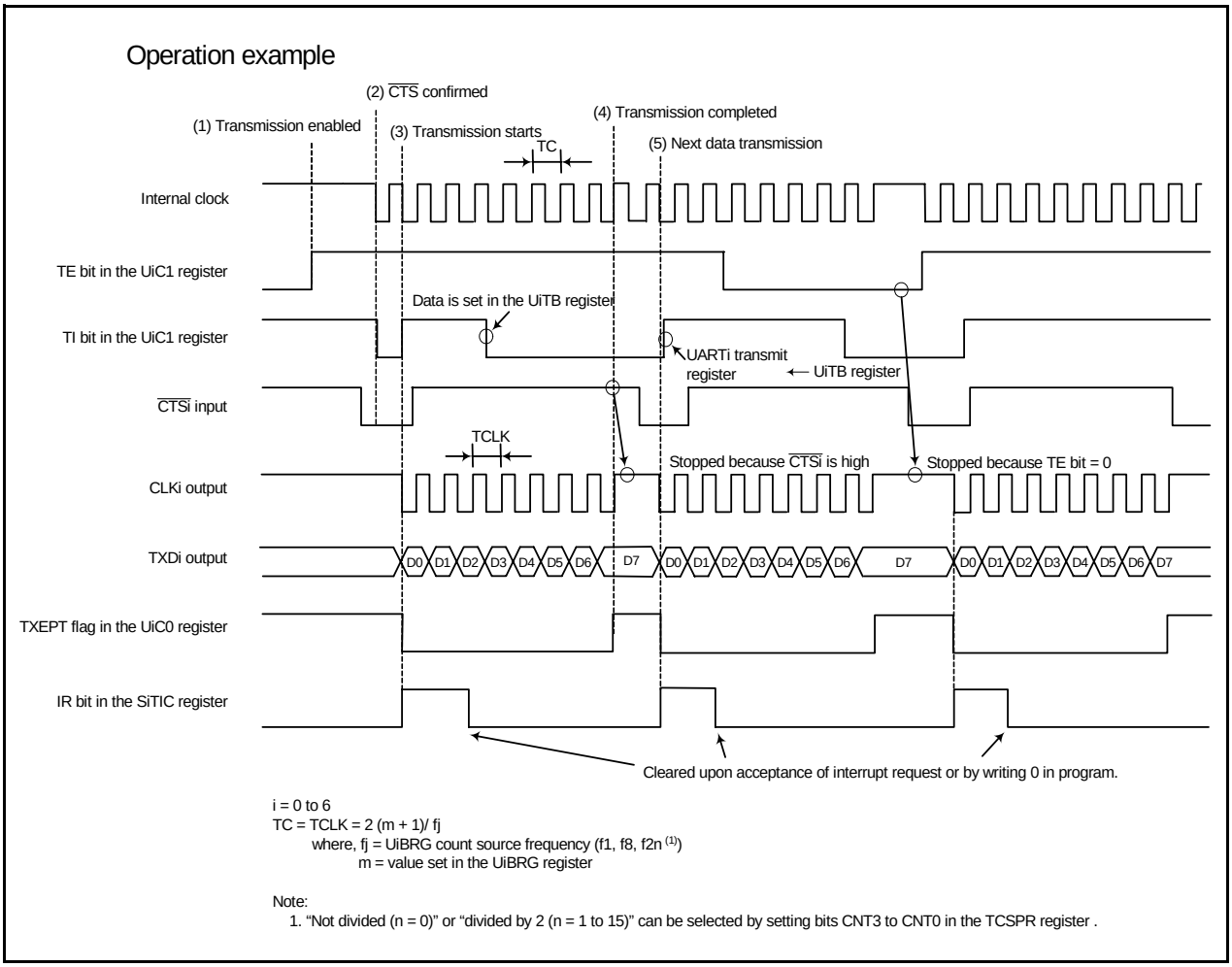


Figure 3.2 Transmit Operation Timing

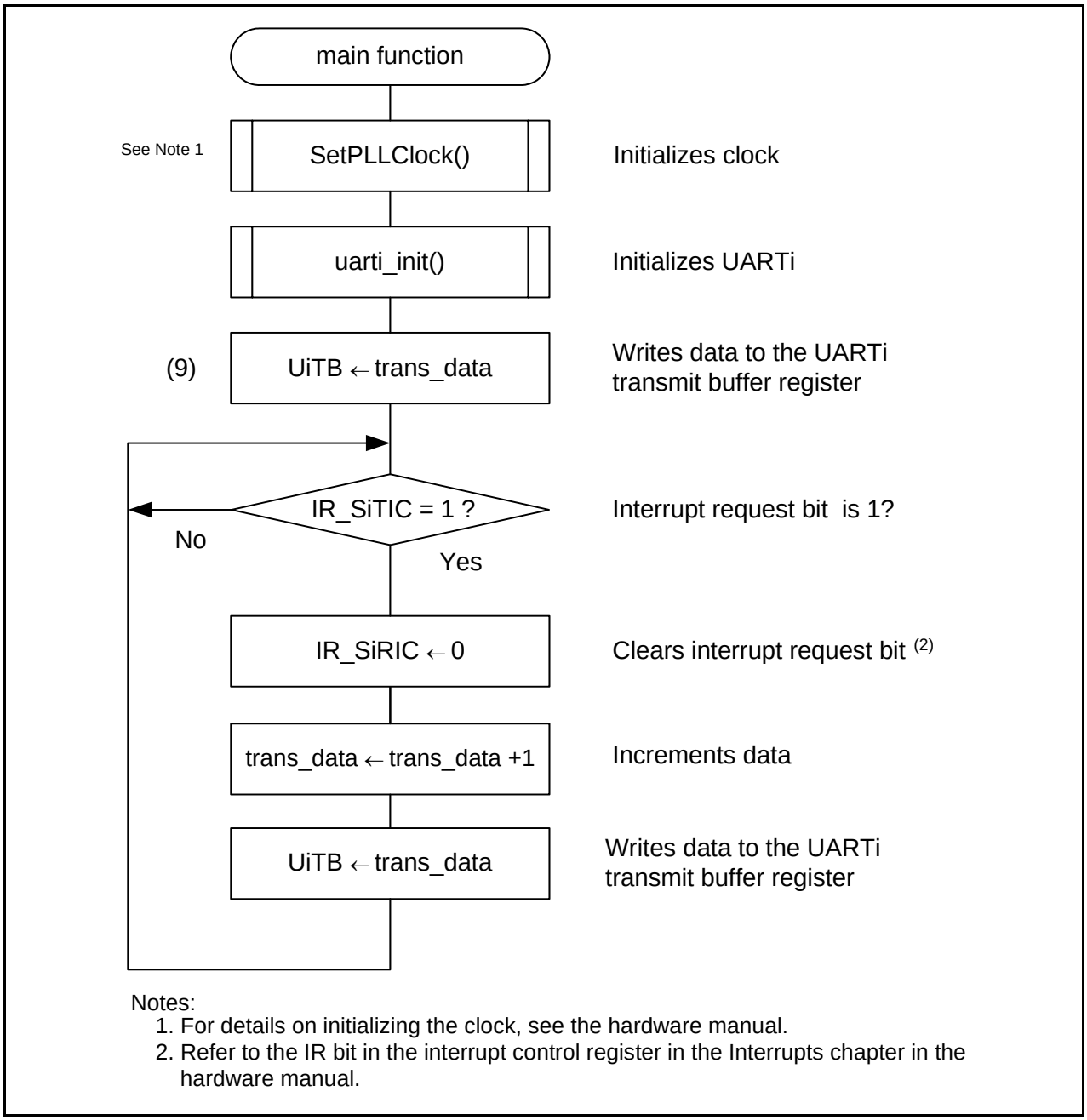
3.2 Settings

This section describes the procedure and values to execute the examples shown in example 3.1 “Data Transmission in Synchronous Serial Interface Mode”. For details on each register, refer to hardware manual.

In the sample program, transmission starts by writing transmit data to the UARTi transmit buffer register (i = 0 to 6).

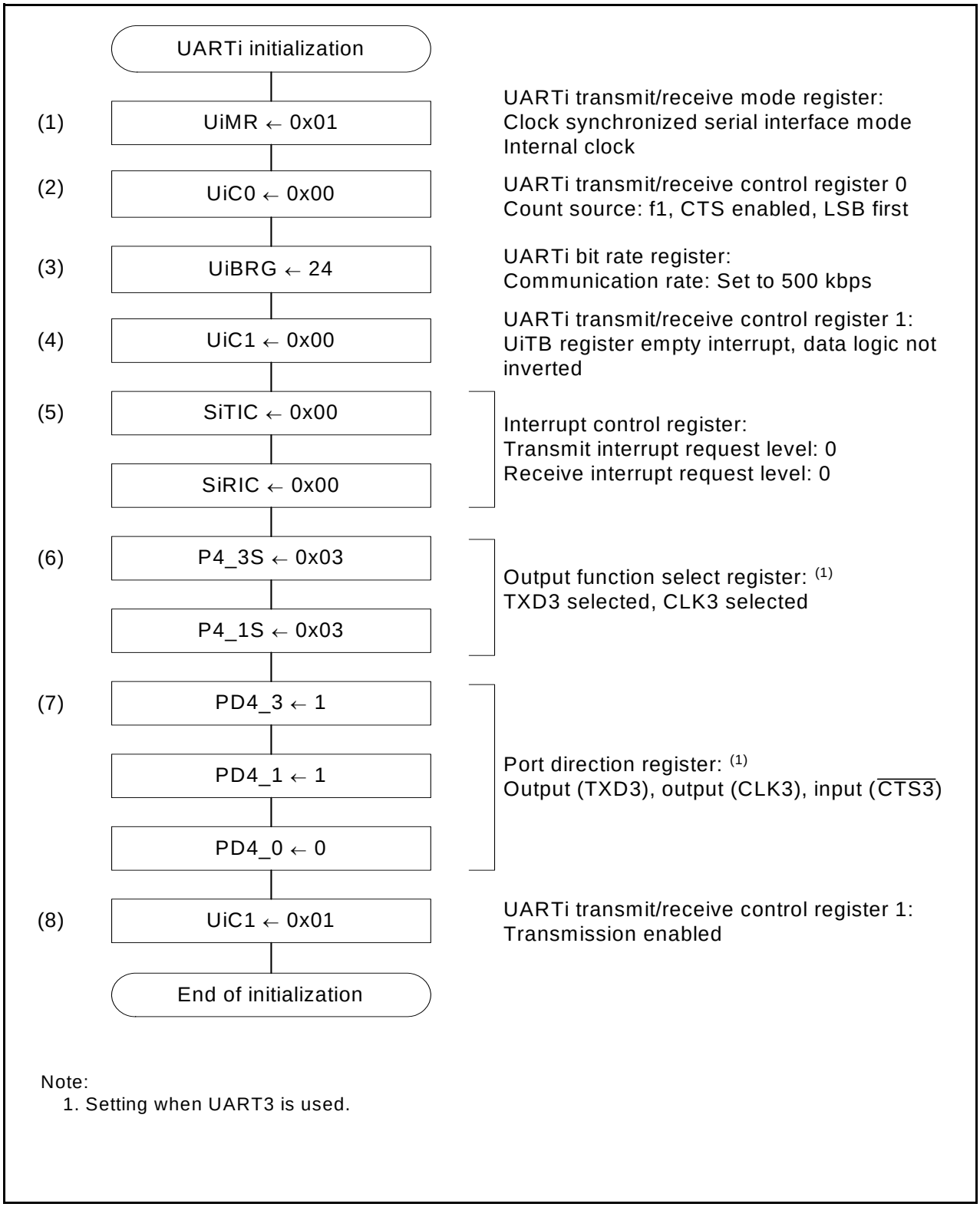
When the program detects that the interrupt request bit in the UARTi transmit interrupt becomes 1 (interrupt requested), write transmit data to the transmit buffer register after incrementing the transmit data.

Figure 3.3 shows the main Processing Flowchart (i = 0 to 6). Figure 3.4 shows the UARTi Initialization Process Flowchart (i = 0 to 6).



Notes:
1. For details on initializing the clock, see the hardware manual.
2. Refer to the IR bit in the interrupt control register in the Interrupts chapter in the hardware manual.

Figure 3.3 main Processing Flowchart (i = 0 to 6)



Note:
1. Setting when UART3 is used.

Figure 3.4 UARTi Initialization Process Flowchart (i = 0 to 6)

3.3 Setting Procedure

(1) Set the UARTi transmit/receive mode register.

b7 b0

0	0	0	0	0	0	0	1

UARTi Transmit/Receive Mode Register (UiMR)

- SMD2 to SMD0 Serial Interface Mode Select Bit
  001b: Synchronous serial interface mode
- CKDIR Internal/External Clock Select Bit
  0: Internal clock
- Set these bits to 0.
- IOPOL TXD, RXD Input/Output Polarity Switch Bit
  0: Non inverted

(2) Set the UARTi transmit/receive control register 0.

b7 b0

0	0	0	0	0	0	0	0

UARTi Transmit/Receive Control Register 0 (UiC0)

- CLK1 to CLK0 UiBRG Count Source Select Bits
  00b: f1
  Do not set 11b to bits CLK1 to CLK0
- Set this bit to 0.
- TXEPT Transmit Shift Register Empty Flag
  0: Data held in the transmit shift register (transmission in progress)
  1: No data held in the transmit shift register (transmission completed)
- CRD CTS Disable Bit
  0: CTS enabled
- NCH Data Output Select Bit
  0: Pins TXDi/SDAi and SCLi are push-pull output
- CKPOL CLK Polarity Select Bit
  0: Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge.
- UFORM Bit Order Select Bit
  0: LSB first

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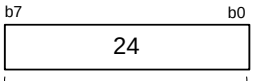
(3) Set the UARTi bit rate register (i = 0 to 6).

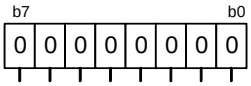


UARTi Bit Rate Register (UiBRG)

Divides the count source by divide-by- n+1 (n = setting value)

24: Divide-by-25

(4) Set the UARTi transmit/receive control register 1



UARTi Transmit/Receive Control Register 1 (UiC1)

TE Transmit Enable Bit
0: Transmission disabled

TI Transmit Buffer Empty Flag
0: Data held in the UiTB register
1: No data held in the UiTB register

RE Receive Enable Bit
0: Reception disabled

RI Receive Complete Flag
0: Data held in the UiRB register
1: No data held in the UiRB register

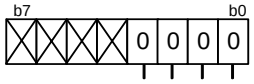
UiIRS UARTi Transmit Interrupt Source Select Bit
0: UiTB register is empty (TI = 1)

UiRRM UARTi Continuous Receive Mode Enable Bit
0: Continuous receive mode disabled

UiLCH Logical Inversion Select Bit
0: Data non logic-inverted

Set this bit to 0.

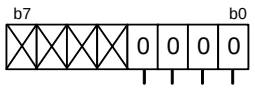
(5) Set the interrupt control register (i = 0 to 6).



UARTi Transmit Interrupt Control Register (SiTIC)

ILVL2 to ILVL0 Interrupt Request Level Select Bit
000b: Level 0 (interrupt disabled)

IR Interrupt Request Flag
0: No interrupt requested



UARTi Receive Interrupt Control Register (SiRIC)

ILVL2 to ILVL0 Interrupt Request Level Select Bit
000b: Level 0 (interrupt disabled)

IR Interrupt Request Flag
0: No interrupt requested

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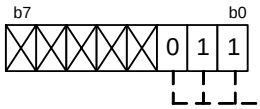
(6) Set the function select register.

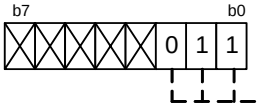
Setting when UART3 is used.



Port P4_3 Function Select Register (P4_3S)

PSEL2 to PSEL0 Port P4_3 Output Function Select Bit

011b: TXD3 output



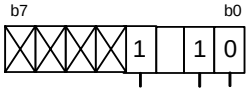
Port P4_1 Function Select Register (P4_1S)

PSEL2 to PSEL0 Port P4_1 Output Function Select Bit

011b: CLK3 output

(7) Set the port direction register.

Setting when UART3 is used.



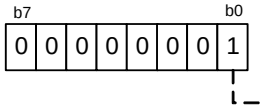
Port Direction Register (PD4)

PD4_0 Port P4_0 Direction Bit
0: Input mode

PD4_1 Port P4_1 Direction Bit
1: Output mode

PD4_3 Port P4_3 Direction Bit
1: Output mode

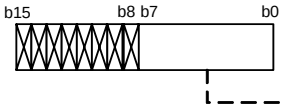
(8) Set the UARTi transmit/receive control register 1 (i = 0 to 6).



UARTi Transmit/Receive Control Register 1 (UiC0)

TE Transmit Enable Bit
1: Transmission enabled

(9) Write the transmit data.



UARTi Transmit Buffer Register (UiTB)

Transmit Data
Transmit data setting

Continued on next page

4. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5. Reference Documents

Hardware Manual
R32C/111 Group Hardware Manual Rev.1.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual
R32C/100 Family C Compiler Package V.1.02 C compiler user manual Rev.1.00
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		Page	Summary
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