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# SH7137 Group

# Sample Application for the CAN Module (Remote Frame Reception)

#### Introduction

This application note describes the controller area network module (RCAN-ET) and provides an example of its application to remote frame reception.

## **Target Devices**

SH7137

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#### 1. Preface

## 1.1 Specifications

• Transfer rate: 500 kbps

Mailbox for transmission: Mailbox 1

• Mailbox for reception: Mailbox 0

• Remote frame for reception is as follows.

ID: 0 (standard format) and data length code (DLC): 2

• Data frame for transmission is as follows.

ID: 0 (standard format), data length code (DLC): 2, and data: H'C1C2

#### 1.2 Module Used

• Controller area network (RCAN-ET)

## 1.3 Applicable Conditions

• MCU SH7137

• Operating frequency Internal clock: 80 MHz

Bus clock: 40 MHz Peripheral clock: 40 MHz

C compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01 Release01

from Renesas Technology

• Compiler options: Default settings of the High-performance Embedded Workshop

 $(-cpu = sh2 - debug - gbr = auto - global\_volatile = 0 - opt\_range = all - infinite\_loop = 0$ 

 $-del_vacant_loop = 0 - struct_alloc = 1)$ 

## 1.4 Related Application Note

None



## 2. Description of the Sample Application

This sample program employs the RCAN-ET module to receive a remote frame (ID: 0 and DLC: 2) and transmit a data frame (DLC: 2 and data: H'C1C2) in standard format (ID: 0).

## 2.1 Overview of Operations by the Module Used

The SH7137 CPU has an internal RCAN-ET module that support CAN2.0B and comply with ISO-11898.

The RCAN-ET module has 15 programmable transmit/receive mailboxes and one receive-only mailbox, each supporting a programmable reception filter mask, providing for highly flexible communications. Figure 1 shows the structure of the RCAN-ET module. For details on the module, refer to the section on the controller area network in the SH7137 Group Hardware Manual.

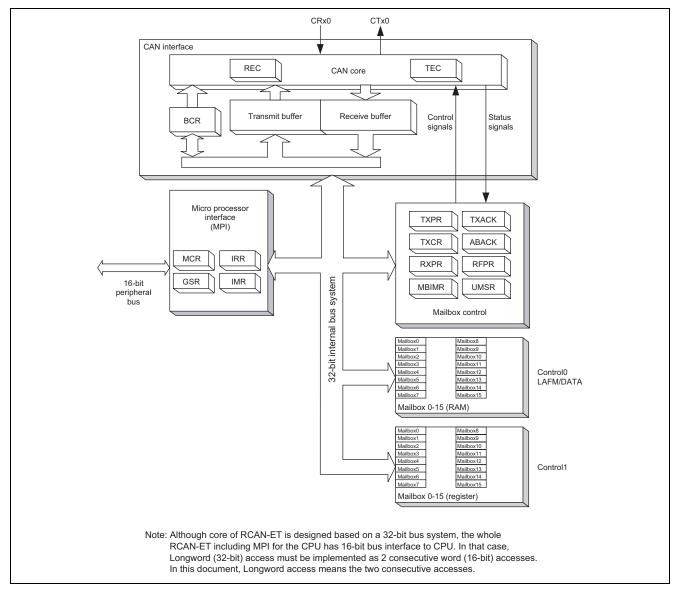


Figure 1 Structure of the RCAN-ET Module



## 2.2 Procedure for Setting the Module Used

This section describes initial settings for the reception of remote frames by the RCAN-ET module.

Initial settings of the module are made in reset mode (configuration mode). On subsequent release from reset mode, the RCAN-ET module participates in CAN-bus activity. Figures 2 and 3 show examples of the flow of initialization for the RCAN-ET module. For details on the settings made to individual registers, refer to the *SH7137 Group Hardware Manual*.

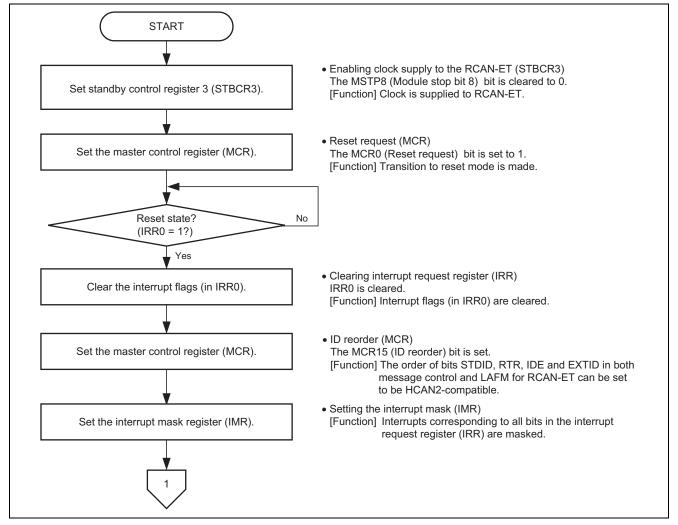


Figure 2 Example of Initialization Flow for the RCAN-ET Module (1)



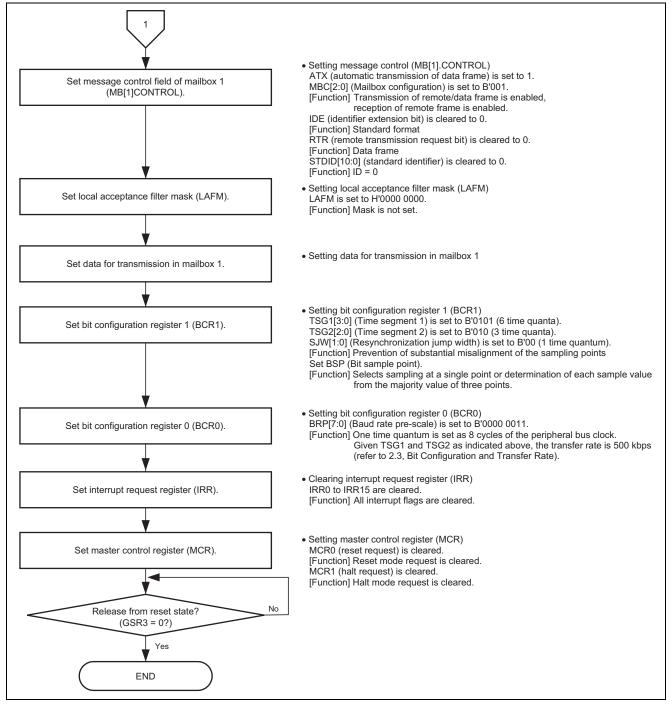


Figure 3 Example of Initialization Flow for the RCAN-ET Module (2)



## 2.3 Bit Configuration and Transfer Rate

One-bit time for the CAN module has the four segments indicated below.

- (1) Synchronization segment (SS)
- (2) Propagation time segment (PRSEG)
- (3) Phase buffer segment 1 (PHSEG1)
- (4) Phase buffer segment 2 (PHSEG2)

Furthermore, the individual segments are structured in units of a base time called the time quantum (Tq). Figure 4 shows an example of the configuration of a bit in the case where SS = 1Tq, PRSEG = 3Tq, PHSEG1 = 3Tq, and PHSEG2 = 3Tq.

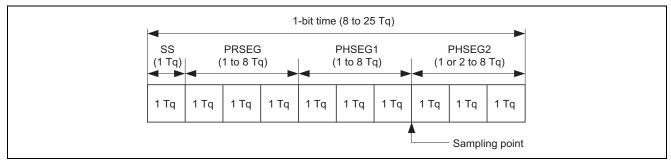


Figure 4 Configuration of One-Bit Time

In the RCAN-ET, the Tq of PRSEG + PHSEG1 is set to TSG1[3:0] in bit configuration register 1 (BCR1) and the Tq of PHSEG2 is set to TSG2[2:0] (Tq = set value + 1). Additionally, the number of cycles of the peripheral-bus clock corresponding to 1Tq is set in BRP[7:0] of bit configuration register 0 (BCR0).

In the following description, BRP[7:0], TSG1[3:0] and TSG2[2:0] indicate the register settings, and BRP, TSEG1, TSEG2, and SJW indicate the values that correspond to these register settings. For the values corresponding to the values set in registers, refer to the section on the controller area network in the SH7137 Group Hardware Manual.

By definition, Tq for the RCAN-ET module is  $1Tq = 2 \times (BRP[7:0] + 1)/peripheral bus clock, and the transfer rate is calculated as follows.$ 

Transfer rate = peripheral bus clock/ $(2 \times (BRP[7:0] + 1) \times the number of Tq in 1-bit time) = peripheral bus clock/<math>(2 \times (BRP[7:0] + 1) \times ((TSG1[3:0] + 1) + (TSG2[2:0] + 1) + 1)$ 

The following restrictions apply to settings of the bit-configuration registers.

TSEG1 (Min) > TSEG2  $\geq$  SJW (Max) (SJW = 1 to 4)

SJW: Jump width for resynchronization. This segment is used to correct phase errors by extending phase buffer segment 1 or shortening phase buffer segment 2.

 $8 \le TSEG1 + TSEG2 + 1 \le 25$  time quanta  $TSEG2 \ge 2$ 

Since the settings in this sample program are as follows: peripheral bus clock = 40 MHz, BRP = 3, TSG1 = 5, TSG2 = 2, the transfer rate is calculated with the following formula.

Transfer rate (bps) = 40 M  $(2 \times (3 + 1) \times ((5 + 1) + (2 + 1) + 1) = 500 \text{ k}$ 



#### 2.4 Operation of the Sample Program

In this sample program, a remote frame (DLC: 2) in standard format (ID: 0) is received in mailbox 0 and a data frame (DLC: 2 and data: H'C1C2) in standard format (ID: 0) is transmitted from mailbox 1 at a transfer rate of 500 kbps. Figure 5 shows the waveform for remote frame reception.

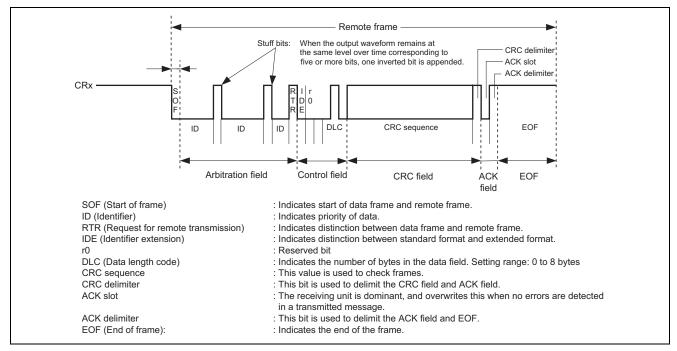


Figure 5 Waveform for Remote Frame Reception by the RCAN-ET



## 2.5 Procedure of Processing by the Sample Program

Table 1 gives an example of the settings for the controller area network (RCAN-ET). Figure 6 shows an example of the flow of processing by this sample program.

Table 1 Register Settings for Controller Area Network (RCAN-ET)

Register Name	Address	Setting Value	Description
Standby control register 3 (STBCR3)	H'FFFF E806	H'F6	MSTP8 = 0: RCAN-ET runs
Master control register (MCR)	H'FFFF D800	H'0001	MCR0 = 1: Reset mode transition request
		H'1001	<ul> <li>MCR15 = 1: RCAN-ET is not the same as HCAN2</li> </ul>
		H'1000	MCR0 = 0: Release from reset mode
Interrupt mask register (IMR)	H'FFFF D80A	H'FFFF	Disables all interrupts of RCAN
Bit configuration register 1 (BCR1)	H'FFFF D804	H'5200	<ul> <li>TSG1[3:0] = 0101:         PRSEG + PHSEG1 = 6 Tq</li> <li>TSG2[2:0] = 010: PHSEG2 = 3 Tq</li> <li>SJW[1:0] = 00: SJW = 1 Tq</li> <li>BSP = 0: Bit sampling at one point</li> </ul>
Bit configuration register 0 (BCR0)	H'FFFF D806	H'0003	• BRP[7:0] = 3: 1 Tq = $8 \times P\phi$
Message control field (MB[1].CONTROL1H)	H'FFFF D942	H'1100	<ul> <li>ATX = 1:         Automatic transmission of data frame</li> <li>MBC[2:0] = 001:         Enables transmission of data frames and remote frames, and reception of remote frames</li> </ul>
Message control field (MB[1].CONTROL0H)	H'FFFF D920	H'0000 0000	<ul> <li>IDE = 0: Standard format</li> <li>RTR = 0: Data frame</li> <li>STDID[10:0] = 0: Standard ID = 0</li> </ul>
Local acceptance filter mask (MB[0].LAFM)	H'FFFF D904	H'0000 0000	Clear: MASK is not set
Remote frame receive pending register 0 (RFPR0)	H'FFFF D84A	H'0000 0002	Clears the remote frame receive pending flag
Transmit acknowledge register 0 (TXACK0)	H'FFFF D832	H'0002	Clears the transmit acknowledge flag



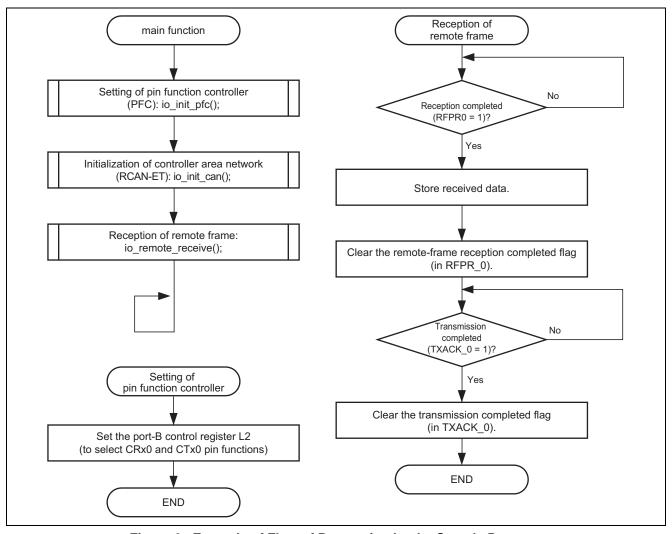


Figure 6 Example of Flow of Processing by the Sample Program



## 3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```
2
 3
            System Name : SH7137 Sample Program
 4
            File Name : main.c
            Contents : CAN Module Application (Remote Frame Receive)
                     : 1.00.00
            Version
                     : M3A-HS37
           CPU
                      : SH7137
           Compiler : SHC9.1.1.0
9
            note
10
                     : CAN bus speed 500 kbps
11
                        The mailbox 1 in CAN1 receives the remote frame (ID=0,DLC=2, standard format)
                        to write the received frame in RAM.
12
13
                        After receiving the remote frame, the data frame is automatically
14
                        transmitted from the mailbox 1.
15
16
                    <Caution>
17
                    This sample program is for reference
18
                    and its operation is not guaranteed.
19
                    Customers should use this sample program for technical reference
20
                    in software development.
21
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29
30
           history : 2008.03.24 ver.1.00.00
31
    32
    #include "iodefine.h"
                           /* SH7137 iodefine */
33
34
     /* ---- prototype declaration ---- */
35
     void main(void);
     void io_init_pfc(void);
37
     void io_init_can(void);
38
    void io_remote_receive(void);
39
    /* ---- symbol definition ---- */
41
    #define CAN_GSR3 0x0008
42
   #define CAN_IRR0 0x0001
43
   #define CAN_MB0 0x0001
44
    #define CAN_MB1 0x0002
    #define CAN_MB01 0x00000002
46
47
     /* ---- RAM allocation variable declaration ---- */
48
    unsigned char nIDE = 0;  /* ide */
49
    unsigned char nRTR = 0;
                                    /* rtr */
50
    unsigned char nDLC = 0;
                                    /* dlc */
51
   unsigned int nSID = 0;
                                    /* sid */
52
                                    /* eid */
    unsigned int nEID = 0;
53
    unsigned char gSnd_data[8] = {0xc1, 0xc2, 0xc3, 0xc4, 0xc5, 0xc6, 0xc7, 0xc8};
```



#### 2. Sample Program Listing: main.c (2)

```
55
56
     * Outline : Sample program main
    *_____
58
     * Include : non
     *-----
59
60
     * Declaration : void main(void);
     * Function : Sample program main
63
     *_____
     * Argument : non
65
66
    * Return Value: non
67
     * Notice : non
68
    69
70
    void main(void)
71
72
       /* ==== Setting of PFC ==== */
73
      io_init_pfc();
74
75
      /* ==== Initializing CAN module ==== */
76
      io_init_can();
77
78
      /* ==== CAN remote frame reception ==== */
79
      io_remote_receive();
80
81
      while(1){
          /* loop */
82
83
84
   }
    87
    * Outline : PFC setting
88
89
     * Include : #include "iodefine.h"
     *----
     * Declaration : void io_init_pfc(void);
     *_____
     * Function : Pin function controller (PFC) setting
93
     * Argument : non
95
96
     *_____
97
     * Return Value: non
98
99
     * Notice : non
    100
101
    void io_init_pfc(void)
102
      /* ==== Setting of PFC ==== */
103
      /* ---- Port B control register L2 ---- */
104
105
      PFC.PBCRL2.BIT.PB7MD = 0x6; /* Set CRx0 */
      PFC.PBCRL2.BIT.PB6MD = 0x6; /* Set CTx0 */
106
      PFC.PBIORL.BIT.B7 = 0; /* PB7(CRX0) input */
PFC.PBIORL.BIT.B6 = 1; /* PB6(CTX0) output */
107
108
109
110
```



#### 3. Sample Program Listing: main.c (3)

```
111
      * Outline : RCAN setting
113
      *_____
114
      * Include : #include "iodefine.h"
      *----
115
116
      * Declaration : void io_init_can(void);
117
118
      * Function : Controller area network (RCAN) setting
119
      *_____
      * Argument : non
120
121
122
      * Return Value: non
123
      *_____
      * Notice : non
124
      125
126
     void io init can(void)
127
     {
128
        int i;
        int j;
129
130
131
       /* ==== Setting of power down mode(RCAN) ==== */
        STB.CR3.BYTE = 0xF6;
                                   /* Module Standby Clear */
132
                                   /* RCAN */
133
        /* ==== Initializing CAN module ==== */
134
        RCANET.MCR.WORD |= 0x0001; /* CAN Interface reset mode */
135
        while((RCANET.IRR.WORD & CAN_IRR0) != CAN_IRR0){
136
137
              /* Reset state waiting */
138
        /* ==== IRR = 1, GSR = 1 (Auto SET) ==== */
139
140
       /* ---- Clear IRRO ---- */
141
142
       RCANET.IRR.WORD = 0 \times 0001;
143
        /* ---- RCAN mode selection(MCR15) ---- */
144
145
        RCANET.MCR.WORD = 0 \times 8000;
                              /* RCAN-ET is not same as HCAN2 */
146
       /* ---- Disable all can interrupt ---- */
147
        RCANET.IMR.WORD = 0xFFFF;
148
149
        /* ---- All mailbox init ---- */
150
151
        for(i = 0; i < 16; i++)
152
              RCANET.MB[i].CTRLO.LONG = 0 \times 000000000;
              RCANET.MB[i].LAFM.LONG = 0 \times 0000000000;
153
154
              for(j = 0; j < 8; j++){
155
                       RCANET.MB[i].MSG_DATA[j] = 0 \times 00;
156
        }
157
158
159
        /* ---- Config mailbox1 as transmission/reception slot ---- */
       RCANET.MB[1].CTRL1.WORD = 0x1100; /* Auto dataframe transmission,
160
161
                                         Can send data or remote frame,
162
                                         receive remote frame, dlc=0 */
        RCANET.MB[1].CTRL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
163
164
        RCANET.MB[1].LAFM.LONG = 0 \times 0000000000;
165
        for(i = 0; i < 8; i++){
                                       /* send data */
              RCANET.MB[1].MSG_DATA[i] = gSnd_data[i];
166
167
        }
168
```



#### 4. Sample Program Listing: main.c (4)

```
/* ---- Config baudrate ---- */
169
170
        RCANET.BCR1.WORD = 0x5200; /* tsg1=5(6 bits), tsg2=2(3 bits),sjw = 0(1 bit),bsp=0 */
        RCANET.BCR0.WORD = 0x0003; /* 500 kbps */
171
    // RCANET.BCR0.WORD = 0x0007; /* 250 kbps */
172
    // RCANET.BCR0.WORD = 0x000F; /* 125 kbps */
173
174
175
         /* ---- Clear interrupt flags ---- */
176
        RCANET.IRR.WORD = 0xffff;
177
        /* ---- Clear reset and halt ---- */
178
179
        RCANET.MCR.WORD &= 0xf8fc;
180
        while( (RCANET.GSR.WORD & CAN_GSR3) != 0x0000 ){
181
               /* reset state is end */
182
183
    }
184
     185
186
      * Outline : Remote frame receive
187
      * Include : #include "iodefine.h"
188
189
      * Declaration : void io_remote_receive(void);
190
191
192
      193
194
      * Argument : non
195
      * Return Value: non
196
      *-----
197
198
      * Notice
              : non
      199
200
     void io_remote_receive(void)
201
         /* ---- Reception completion waiting ---- */
202
203
        while((RCANET.RFPR0.WORD & CAN_MB1) != CAN_MB1){
204
205
        /* ---- Receive data storage ---- */
206
207
        nIDE = RCANET.MB[0].CTRL0.BIT.IDE;
208
       nRTR = RCANET.MB[0].CTRL0.BIT.RTR;
209
       nDLC = RCANET.MB[0].CTRL1.BIT.DLC;
210
       nSID = RCANET.MB[0].CTRL0.BIT.STDID;
        nEID = RCANET.MB[0].CTRL0.BIT.EXDID;
211
212
        /* ---- Reception completion flag clear ---- */
213
        RCANET.RXPR0.WORD = CAN_MB1;
214
215
        /* ---- Transmission completion waiting ---- */
216
217
        while((RCANET.TXACK0.WORD & CAN_MB1) != CAN_MB1){
218
219
        /* ---- Transmission completion flag clear ---- */
220
221
        RCANET.TXACKO.WORD = CAN_MB1;
222
223
     /* End of File */
224
```



#### 4. Documents for Reference

• Software Manual

SH-1/SH2/SH-DSP Software Manual (REJ09B0171)

The most up-to-date version of this document is available on the Renesas Technology Website.

• Hardware Manuals

SH7137 Group Hardware Manual (REJ09B0402)

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