RZ/T1 Group

FIFO Integrated Serial Communication Interface (SCIFA)

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Introduction

This application note describes a sample program that uses asynchronous communications of the serial communications interface with integrated FIFO (SCIFA) that RZ/T1 incorporates.

The major feature of the program is given below.

- Connecting to a PC and using terminal software enables communications with PC.

Target Devices

RZ/T1 Group

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

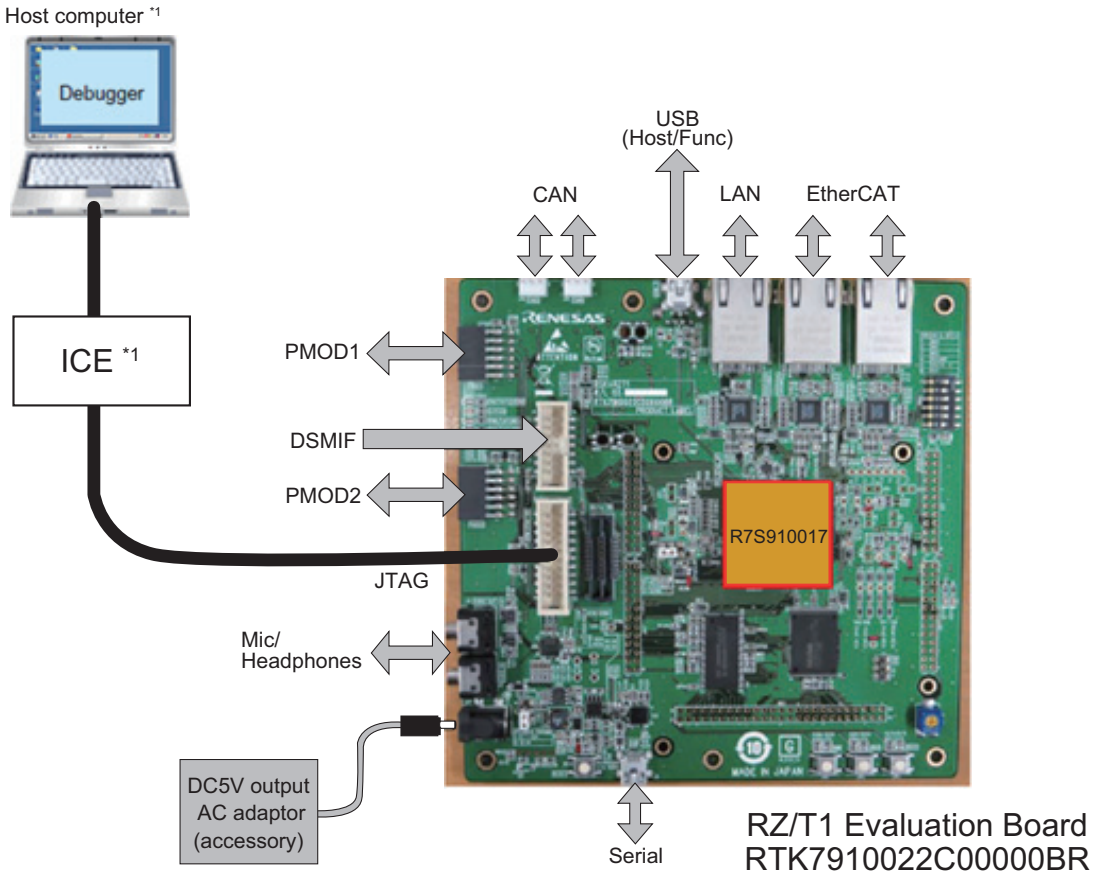
Table of Contents

1. Specifications

Table 1.1 lists the peripheral functions to be used and their applications and Figure 1.1 shows the operating environment.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Clock Pulse Generator (CPG)	The CPG produces the CPU clock and low-speed on-chip oscillator clock signals
FIFO integrated serial communication interface (SCIFA)	Asynchronous communications of the SCIFA is used for COM port communications by using an RS-232C interface
Error control module (ECM)	The ECM is used to initialize the ERROROUT# pin.



Note 1. Indicates the device that the user needs to prepare.

Figure 1.1 Operating Environment

2. Operating Environment

The sample code covered in this application note is for the environment below.

Table 2.1 Operating Environment

Item	Description
Microcomputer	RZ/T1 Group
Operating frequency	CPUCLK = 450 MHz
Operating voltage	3.3 V
Integrated Development Environment	Manufactured by IAR Systems Embedded Workbench® for Arm Version 8.20.2 Manufactured by Arm DS-5™ 5.26.2 Manufactured by RENESAS e2studio 6.1.0
Operating modes	SPI boot mode 16-bit bus boot mode
Communication setting of the terminal software	• Communication speed: 115200 bps • Date length: 8 bits • Parity: N/A • Stop bit length: 1 bit • Flow control: N/A
Board	RZ/T1 Evaluation board (RTK7910022C00000BR)
Devices (functions to be used on the board)	• Serial interface (USB-Mini B connector J8) • NOR flash memory (connected to CS0/CS1 space) Manufacturer: Macronix International Co. Ltd. Model: MX29GL512FLT2I-10Q • SDRAM (connected to CS2/CS3 space) Manufacturer: Integrated Silicon Solution Inc. Model: IS42S16320D-7TL • Serial flash memory Manufacturer: Macronix International Co. Ltd. Model: MX25L51245G
USB serial port driver for PC	• For RTK7910018C00000BE • For RTK7910022C00000BR

3. Related Documents

The application note related to this application note is listed below for reference.

- RZ/T1 Group Initial Settings

4. Peripheral Functions

For the basics of the clock pulse generator (CPG), FIFO integrated serial communication interface (SCIFA), and error control module (ECM), refer to the RZ/T1 Group User's Manual: Hardware.

5. Hardware

5.1 Example of Hardware Configuration

Figure 5.1 shows an example of the hardware configuration.

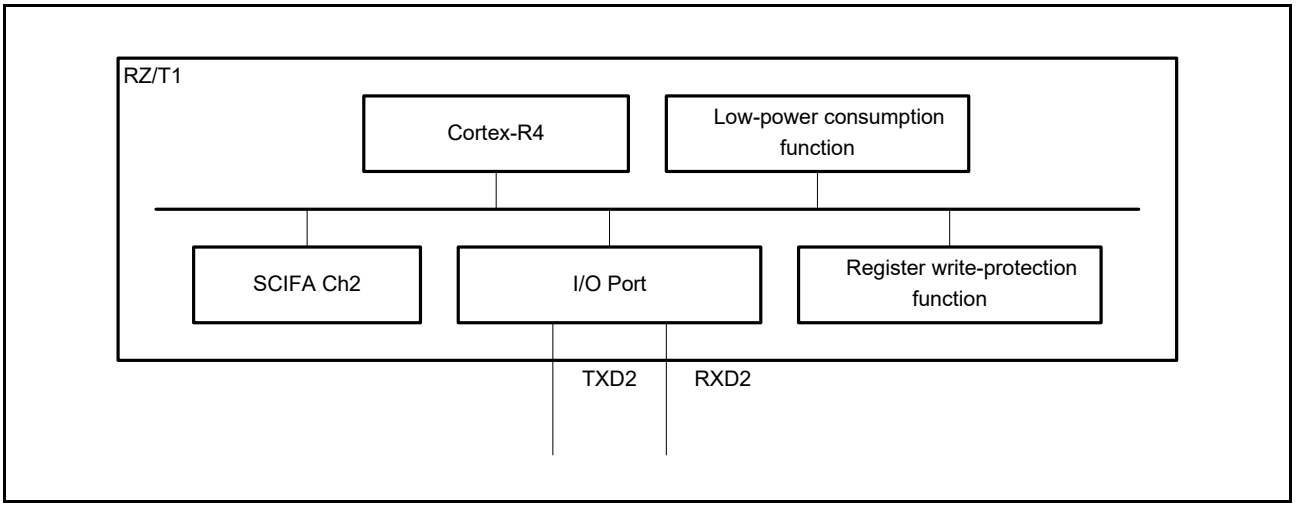


Figure 5.1 Example of Hardware Configuration

5.2 Pins

Table 5.1 lists pins to be used and their functions.

Table 5.1 Pins and Functions

Pin Name	I/O	Function
MD0	Input	Selection of operating modes MD0 = L, MD1 = L, MD2 = L (SPI boot mode) MD0 = L, MD1 = H, MD2 = L (16-bit bus boot mode)
MD1	Input	
MD2	Input	
TXD2	Output	Serial transmission data signal
RXD2	Input	Serial reception data signal

6. Software

6.1 Operation Overview

The sample program makes the settings required for COM port communications between a host PC and an RS-232 interface set up by using asynchronous communications through the serial communication interface with FIFO (SCIFA). After the settings are complete, the software responds to keyboard input from the host PC.

The functional overview of this sample program is shown below.

Table 6.1 Functional Overview

Function	Description
Channel	Channel 2 (SCIFA2)
Serial communication method	Asynchronous
Clock	SERICLK = 150 MHz
Transmission/reception	Serial data transmission/reception LSB first
Transfer speed	115200 bps
Character length	8 bits
Stop bit length	1 bit
Parity	N/A
Hardware flow control	N/A
Interrupts	BRIF2 prohibited RXIF2 prohibited TXIF2 prohibited DRIF2 prohibited

6.1.1 Project Settings

For the project settings of the development environment on the EWARM, refer to the Application Note: RZ/T1 Group Initial Settings.

6.1.2 Preparations

This sample program uses communication with a PC. The following preparations are required for PC communication.

(1) Start the terminal software on a host PC and set the PC as follows.
When COM4 is used for Tera Term:

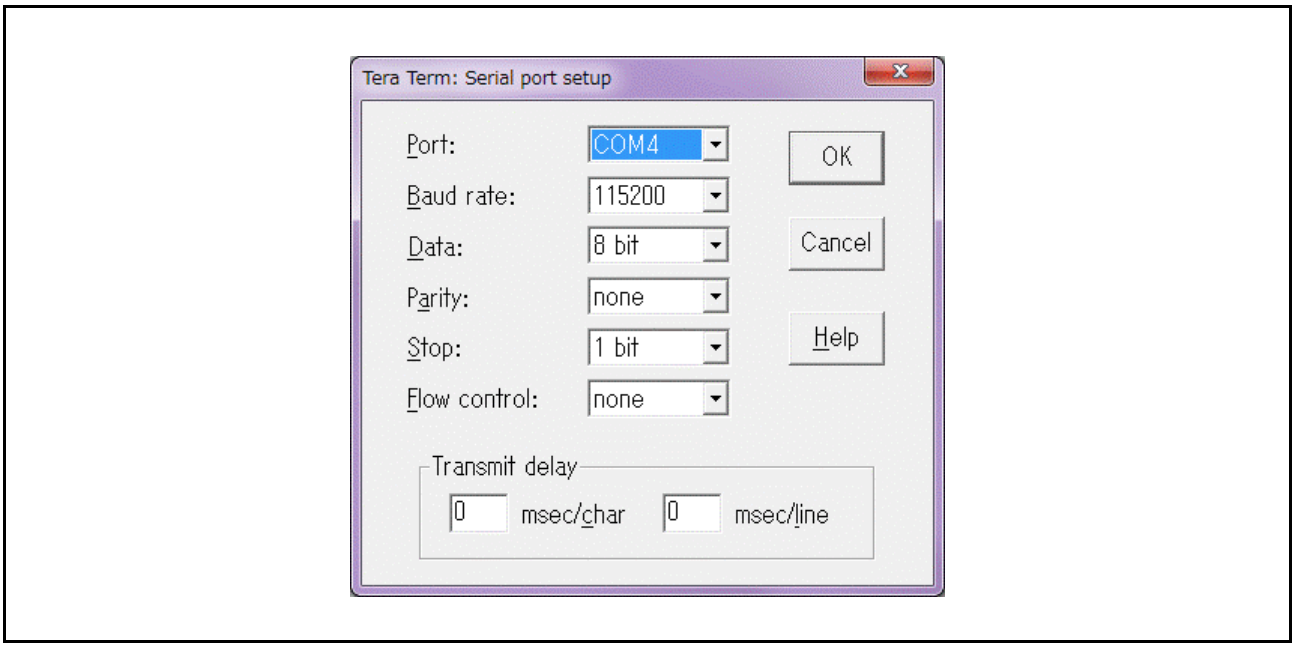


Figure 6.1 Settings of Serial Port

(2) When communications are enabled after executing the sample program, the data received from the sample program is displayed on the terminal software as shown below.

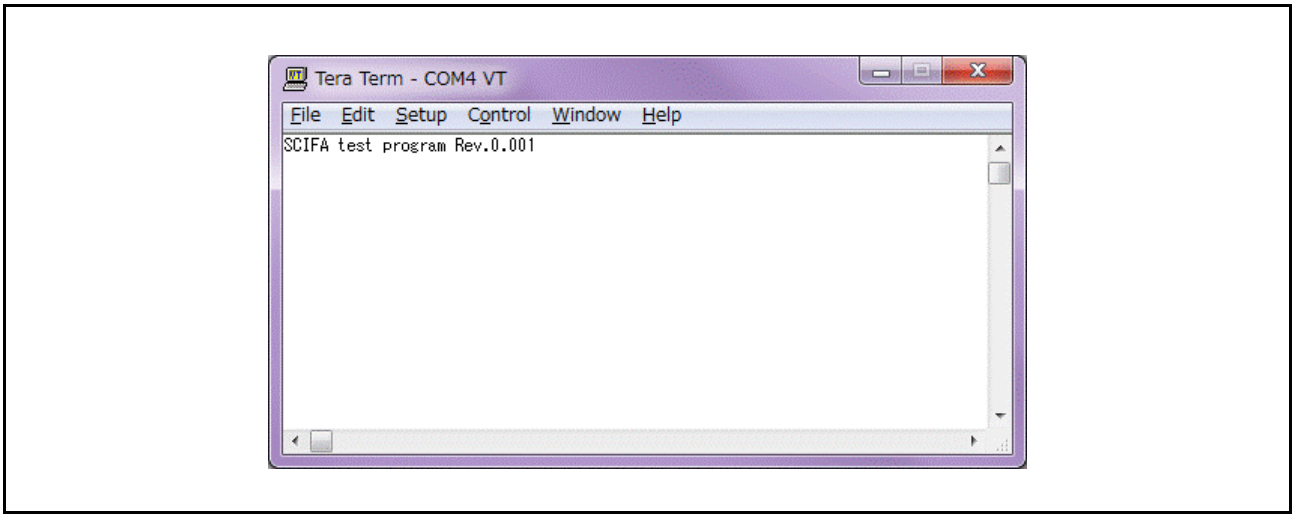


Figure 6.2 Display on Terminal Software after SCIFA Settings

(3) When typing and inputting alphanumeric characters from the keyboard of the host PC and then pressing the enter key, the response from the sample program is confirmed on the terminal software as shown below (input = 1234567890).

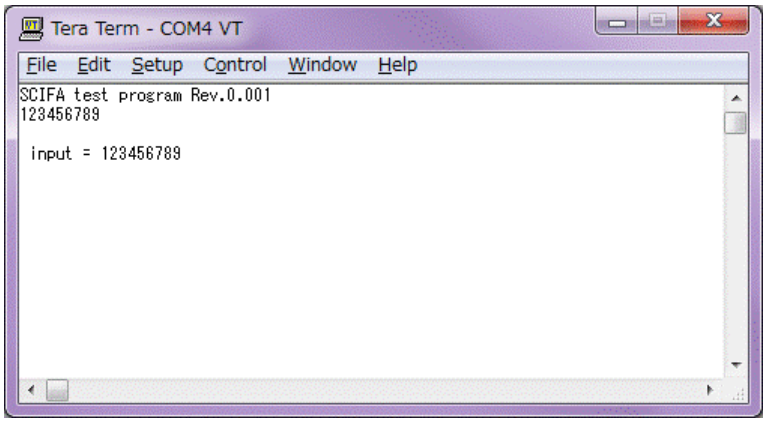


Figure 6.3 Display of Terminal Software after Keyboard Input

6.2 Memory Map

For the address space of the RZ/T1 Group and a memory map of the RZ/T1 evaluation board, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2.1 Assignment to Sections of Sample Program

Refer to the Application Note: RZ/T1 Group Initial Settings for the sections to be used in the program, assignment to sections (loading view) of the sample program in its initial state, and assignment to sections of the sample program following the application of scatter loading (execution view).

6.2.2 MPU Settings

For MPU settings, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2.3 Exception Processing Vector Table

For the vector table for exception processing, refer to the Application Note: RZ/T1 Group Initial Settings.

6.3 Fixed-Width Integer Types

Table 6.2 shows fixed width integers to be used in the sample program.

Table 6.2 Fixed-Width Integers for Sample Program

Symbol	Description
int8_t	8-bit signed integer (defined in the standard library)
int16_t	16-bit signed integer (defined in the standard library)
int32_t	32-bit signed integer (defined in the standard library)
int64_t	64-bit signed integer (defined in the standard library)
uint8_t	8-bit unsigned integer (defined in the standard library)
uint16_t	16-bit unsigned integer (defined in the standard library)
uint32_t	32-bit unsigned integer (defined in the standard library)
uint64_t	64-bit unsigned integer (defined in the standard library)

6.4 Constants/Error Codes

Table 6.3 lists constants of the sample program and Table 6.4 lists error codes of the program.

Table 6.3 Constants for Sample Program

Constant	Setting Value	Description
SCIFA_UART_CH_TOTAL	(5)	Number of SCIFA channel
SCIFA_UART_CH_0	(0)	is used to identify SCIFA channel 0
SCIFA_UART_CH_1	(1)	is used to identify SCIFA channel 1
SCIFA_UART_CH_2	(2)	is used to identify SCIFA channel 2
SCIFA_UART_CH_3	(3)	is used to identify SCIFA channel 3
SCIFA_UART_CH_4	(4)	is used to identify SCIFA channel 4
SCIFA_UART_MODE_R	(1)	is used to use the SCIFA in reception mode: This constant is used for the SCIFA channel initialization function and the argument of the SCIFA channel open function
SCIFA_UART_MODE_W	(2)	is used to use the SCIFA in transmission mode: This constant is used for the SCIFA channel initialization function and the argument of the SCIFA channel open function.
SCIFA_UART_MODE_RW	(3)	is used to use the SCIFA in transmission/reception mode: This constant is used for the SCIFA channel initialization function and the argument of the SCIFA channel open function.
SCIFA_UART_CKS_DIVISION_1	(0)	is used to set the clock source of the SCIFA baud rate generator in clock SERICLK and used for the argument of the SCIFA channel initialization function.
SCIFA_UART_CKS_DIVISION_4	(1)	is used to set the clock source of the SCIFA baud rate generator in clock SERICLK/4 and used for the argument of the SCIFA channel initialization function.
SCIFA_UART_CKS_DIVISION_16	(2)	is used to set the clock source of the SCIFA baud rate generator in clock SERICLK/16 and used for the argument of the SCIFA channel initialization function.
SCIFA_UART_CKS_DIVISION_64	(3)	is used to set the clock source of the SCIFA baud rate generator in clock SERICLK/64 and used for the argument of the SCIFA channel initialization function.

Table 6.4 Error Codes of Sample Program

Constant	Setting Value	Description
SCIFA_UART_SUCCESS	(0)	is used for the return value of the API function related to the SCIFA: This constant indicates that execution of the function is completed successfully.
SCIFA_UART_ERR	(-1)	is used for the return value of the API function related to the SCIFA: This constant indicates that execution of the function failed.
SCIFA_UART_ERR_RECEIVE	(-2)	is used for the return value of the API function related to the SCIFA: This constant indicates that execution of the data receiving function failed.

6.5 Global Variables

Table 6.5 shows global variables.

Table 6.5 Global Variables

Model	Variable	Description	Function
char	gbuff[16]	Received data from the terminal software	main

6.6 Functions

Table 6.6 lists the functions to be used.

Table 6.6 Functions

Function	Page Number
main	14
IoInitScifa2	14
R_SCIFA_UART_Init	15
R_SCIFA_UART_Open	15
R_SCIFA_UART_Send	16
R_SCIFA_UART_Receive	16
userdef_scifa2_uart_init	17
userdef_scifa2_uart_open	17
userdef_scifa2_uart_send	17
userdef_scifa2_uart_receive	18

6.7 Specifications of Functions

6.7.1 main

main	
Synopsis	Main processing
Declaration	int main (void)
Description	This function initializes the ECM and SCIFA, and transmits the data indicating that the SCIFA test program is to start. Afterwards, it loops the data that are input from the PC keyboard until the data are received and transmits the received data when they are received.
Arguments	None
Return value	None
Supplement	None

6.7.2 IoInitScifa2

IoInitScifa2	
Synopsis	Initialization of SCIFA Channel 2
Declaration	void IoInitScifa2 (void)
Description	This function initializes Channel 2 of the SCIFA in UART mode and then enables transmission/reception to start communications.
Arguments	None
Return value	None
Supplement	None

6.7.3 R_SCIFA_UART_Init

R_SCIFA_UART_Init	
Synopsis	SCIFA initial settings
Header	r_scifa_uart.h
Declaration	nt32_t R_SCIFA_UART_Init (uint32_t channel, uint32_t mode, uint16_t cks, uint8_t brr)
Description	This function initializes the SCIFA in asynchronous communication mode and sets the ports to be used in the SCIFA.
Arguments	uint32_t channel : Specifies SCIFA channel to be initialized Setting range (0 to 4)
	uint32_t mode : Specifies the operating modes of the SCIFA SCIFA_UART_MODE_R: reception mode SCIFA_UART_MODE_W: transmission mode SCIFA_UART_MODE_RW: transmission/reception mode
	uint16_t cks : Selects a clock source of the SCIFA baud rate generator SCIFA_UART_CKS_DIVISION_1: SERICLK SCIFA_UART_CKS_DIVISION_4: SERICLK / 4 SCIFA_UART_CKS_DIVISION_16: SERICLK / 16 SCIFA_UART_CKS_DIVISION_64: SERICLK / 64
	uint8_t brr : Specifies the values to be set in the SCIFA bit rate register (BRR). Setting range (See the user's manual: hardware)
Return value	SCIFA_UART_SUCCESS: Initialization successful SCIFA_UART_ERR: Error in argument
Supplement	• Only available for SCIFA Channel 2, but unavailable for Channel 1, 3, and 4 • The pins to be used on the SCIFA Channel 2 are listed below. TXD2: P91 RXD2: P92

6.7.4 R_SCIFA_UART_Open

R_SCIFA_UART_Open	
Synopsis	Starting SCIFA
Header	r_scifa_uart.h
Declaration	int32_t R_SCIFA_UART_Open (uint32_t channel, uint32_t mode)
Description	This function starts up the SCIFA in operating mode (transmission, reception, transmission/reception) specified by the argument and starts asynchronous communications.
Arguments	uint32_t channel : Specifies the SCIFA channel to be initialized. Setting range (0 to 4)
	uint32_t mode : Specifies operating mode of the SCIFA SCIFA_UART_MODE_R: reception mode SCIFA_UART_MODE_W: transmission mode SCIFA_UART_MODE_RW: reception/transmission mode
Return value	SCIFA_UART_SUCCESS: Startup successful SCIFA_UART_ERR: Error in argument
Supplement	• Only available for SCIFA channel 2, but unavailable for channel 1, 3, and 4.

6.7.5 R_SCIFA_UART_Send

R_SCIFA_UART_Send	
Synopsis	Transmitting data
Header	r_scifa_uart.h
Declaration	int32_t R_SCIFA_UART_Send (uint32_t channel, uint8_t data)
Description	This function transmits 1-byte data in the COM port communication via an RS-232C interface.
Arguments	uint32_t channel : Specifies the SCIFA channel to be initialized Setting range (0 to 4)
	uint8_t data : Specifies transmitting data.
Return value	SCIFA_UART_SUCCESS: Transmission successful SCIFA_UART_ERR: Error in argument
Supplement	• Only available for SCIFA channel 2, but unavailable for channel 1, 3, and 4.

6.7.6 R_SCIFA_UART_Receive

R_SCIFA_UART_Receive	
Synopsis	Receiving data
Header	r_scifa_uart.h
Declaration	int32_t R_SCIFA_UART_Receive (uint32_t channel, uint8_t *data)
Description	This function transmits 1-byte data in the COM port communication via an RS-232C interface.
Arguments	uint32_t channel : Specifies the SCIFA channel to be initialized Setting range (0 to 4)
	uint8_t *data : Specifies the area that stores the received data
Return value	SCIFA_UART_SUCCESS: Reception successful SCIFA_UART_ERR: Error in argument SCIFA_UART_ERR_RECEIVE: Error in reception
Supplement	• Only available for SCIFA channel 2, but unavailable for channels 1, 3, and 4.

6.7.7 userdef_scifa2_uart_init

userdef_scifa2_uart_init		
Synopsis	Initializing SCIFA channel 2 in UART mode (user defined)	
Declaration	void userdef_scifa2_uart_init (uint32_t mode, uint16_t cks, uint8_t brr)	
Description		
Arguments	uint32_t mode	: Specifies operating modes of the SCIFA SCIFA_UART_MODE_R: Reception mode SCIFA_UART_MODE_W: Transmission mode SCIFA_UART_MODE_RW: Transmission/reception mode
	uint16_t cks	: Selects a clock source of the SCIFA baud rate generator SCIFA_UART_CKS_DIVISION_1: SERICLK SCIFA_UART_CKS_DIVISION_4: SERICLK / 4 SCIFA_UART_CKS_DIVISION_16: SERICLK / 16 SCIFA_UART_CKS_DIVISION_64: SERICLK / 64
	uint8_t brr	: Specifies values to be set in the SCIFA bit rate register (BRR) Setting range (See the user's manual: hardware.)
Return value	None	
Supplement	None	

6.7.8 userdef_scifa2_uart_open

userdef_scifa2_uart_open		
Synopsis	Starting SCIFA channel 2 in UART mode (user defined)	
Declaration	void userdef_scifa2_uart_open (uint32_t mode)	
Description	This function enables transmission and/or reception according to the mode argument.	
Arguments	uint32_t mode	: Specifies operating modes of the SCIFA SCIFA_UART_MODE_R: Reception mode SCIFA_UART_MODE_W: Transmission mode SCIFA_UART_MODE_RW: Transmission/reception mode
Return value	None	
Supplement	None	

6.7.9 userdef_scifa2_uart_send

userdef_scifa2_uart_send		
Synopsis	Transmitting data of SCIFA channel 2 (user defined)	
Declaration	void userdef_scifa2_uart_send (uint8_t data)	
Description	This function transmits the data specified by the argument.	
Arguments	uint8_t data	: Specifies the data to be transmitted.
Return value	None	
Supplement	None	

6.7.10 userdef_scifa2_uart_receive

userdef_scifa2_uart_receive	
Synopsis	Receiving data of SCIFA channel 2
Declaration	int32_t userdef_scifa2_uart_receive (uint8_t *data)
Description	This function clears the reception error state flag and returns the value indicating an error in reception when an error in reception occurs. When received data is acquired, it stores the received data in the area specified by the argument.
Arguments	uint8_t *data : Specifies the area that stores the received data
Return value	SCIFA_UART_SUCCESS: Reception successful SCIFA_UART_ERR_RECEIVE: Error in reception
Supplement	None

6.8 Flowcharts

6.8.1 Main Processing

Figure 6.4 show a flowchart of main processing.

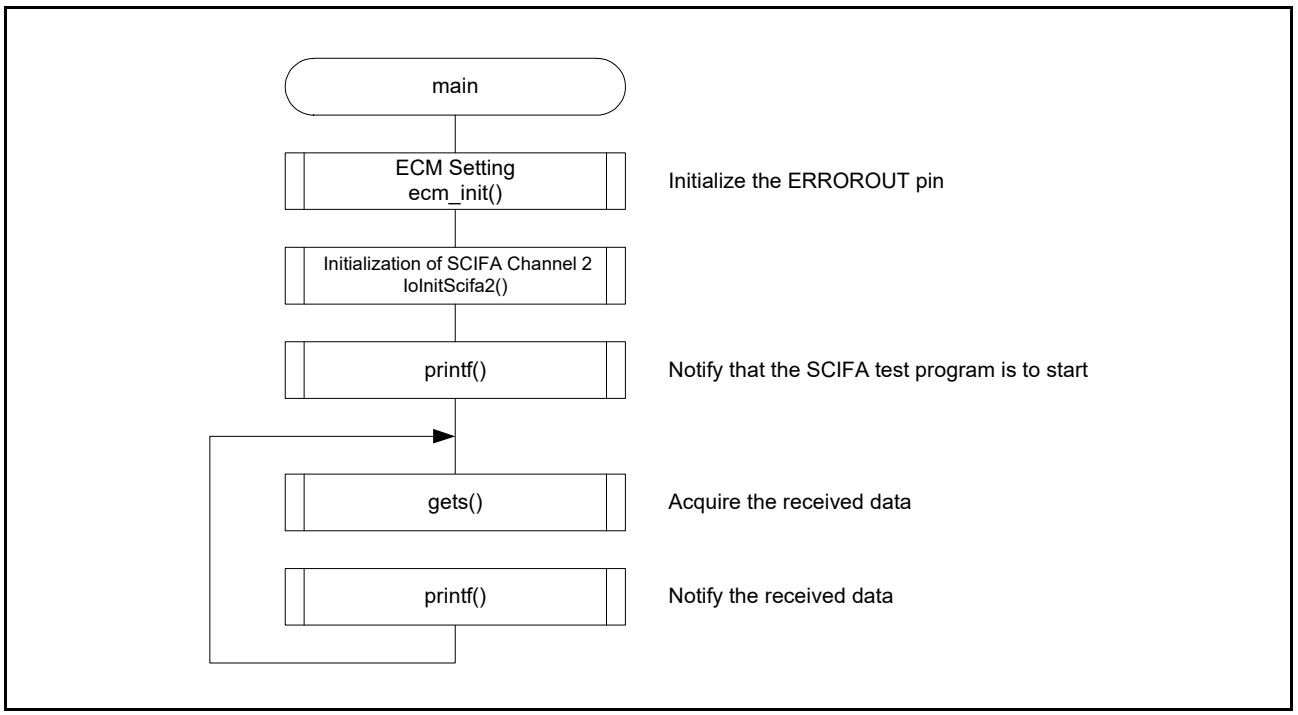


Figure 6.4 Main Processing

6.8.2 Initialization of SCIFA Channel 2

Figure 6.5 shows a flowchart of processing of Initialization of SCIFA Channel 2.

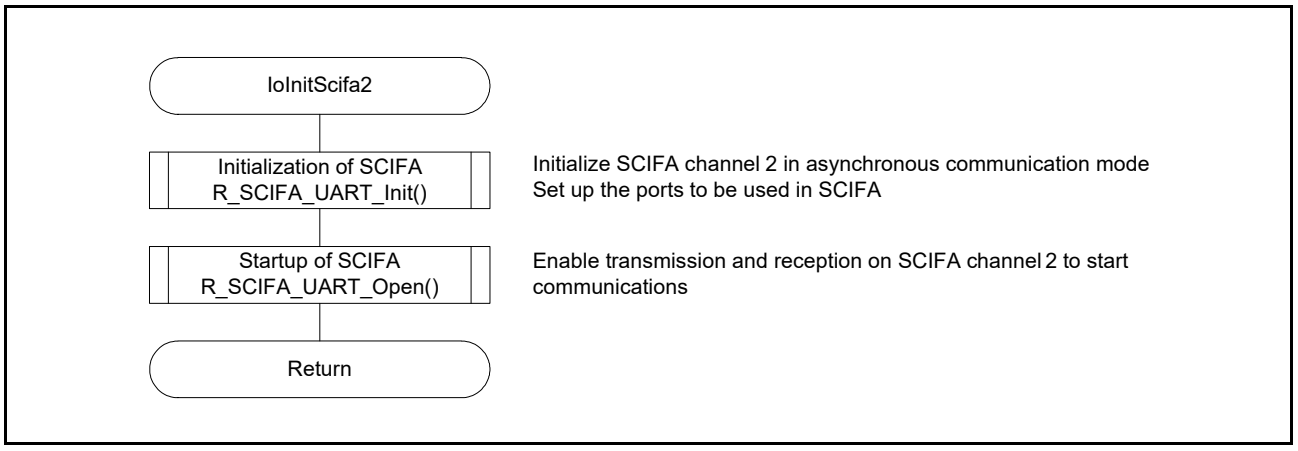
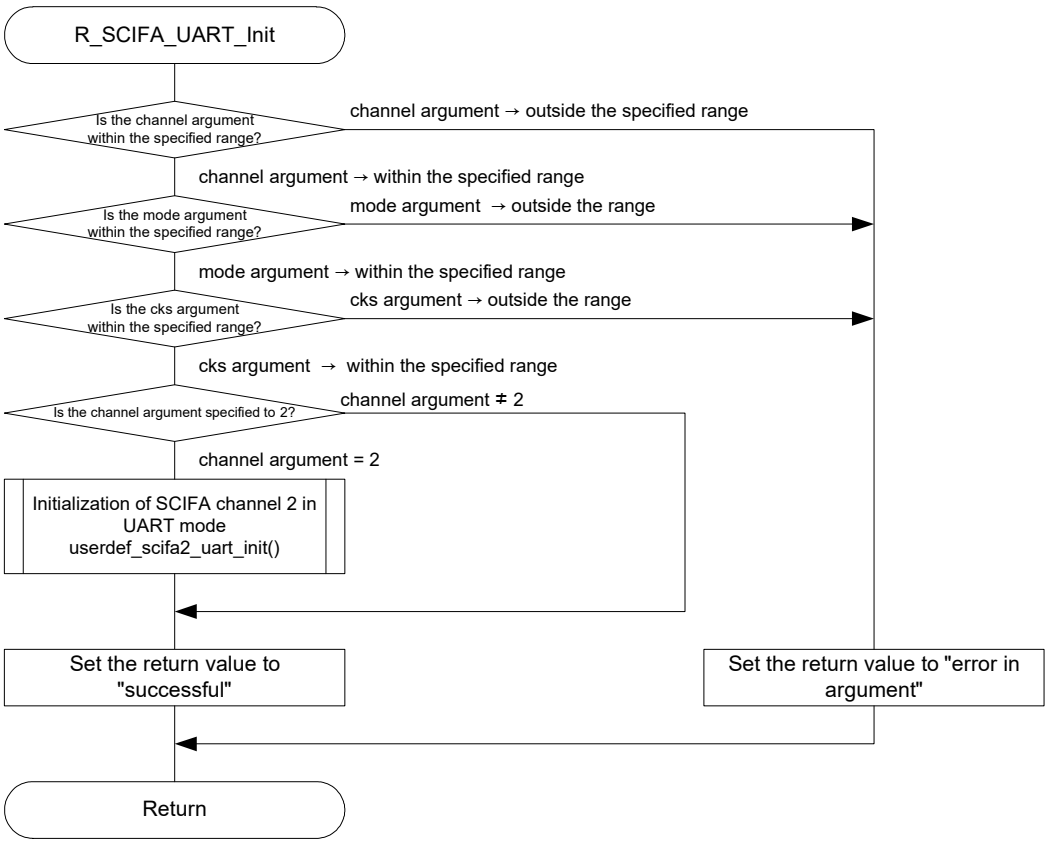


Figure 6.5 Initialization of SCIFA Channel 2

6.8.3 Initialization of SCIFA

Figure 6.6 shows a flowchart of initialization of the SCIFA.



Note: Only available for channel 2, but unavailable for channel 1, 3, and 4.

Figure 6.6 Initialization of SCIFA

6.8.4 Startup of SCIFA

Figure 6.7 shows a flowchart of startup of SCIFA.

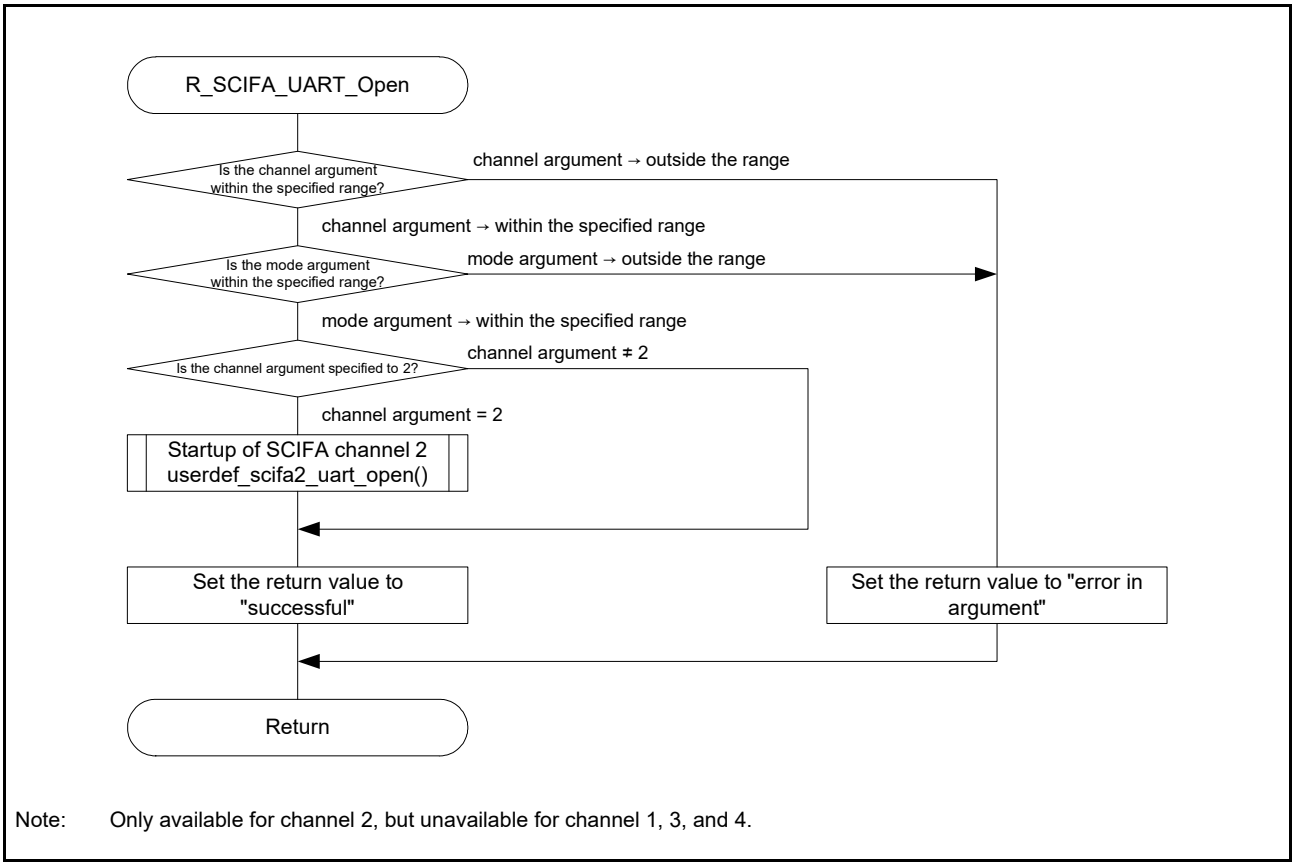
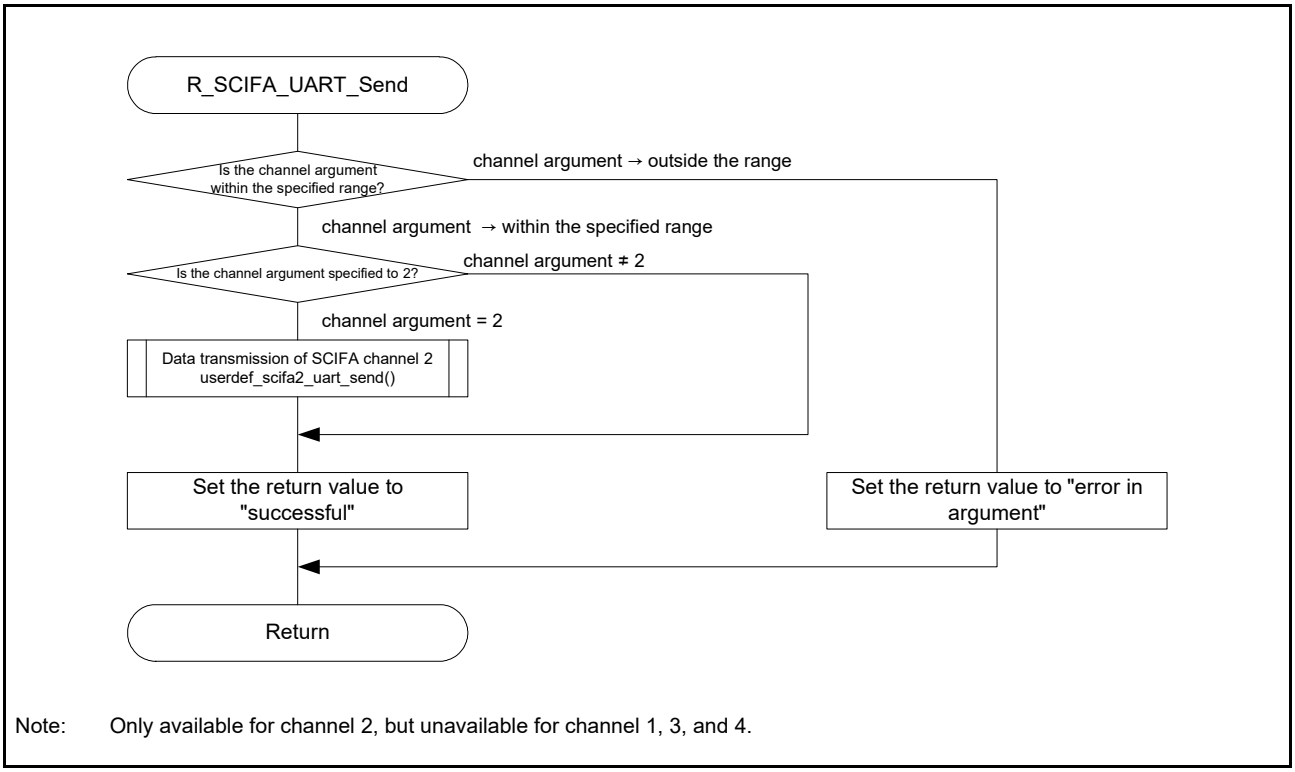


Figure 6.7 Startup of SCIFA

6.8.5 Data Transmission

Figure 6.8 shows a flowchart of data transmission processing.

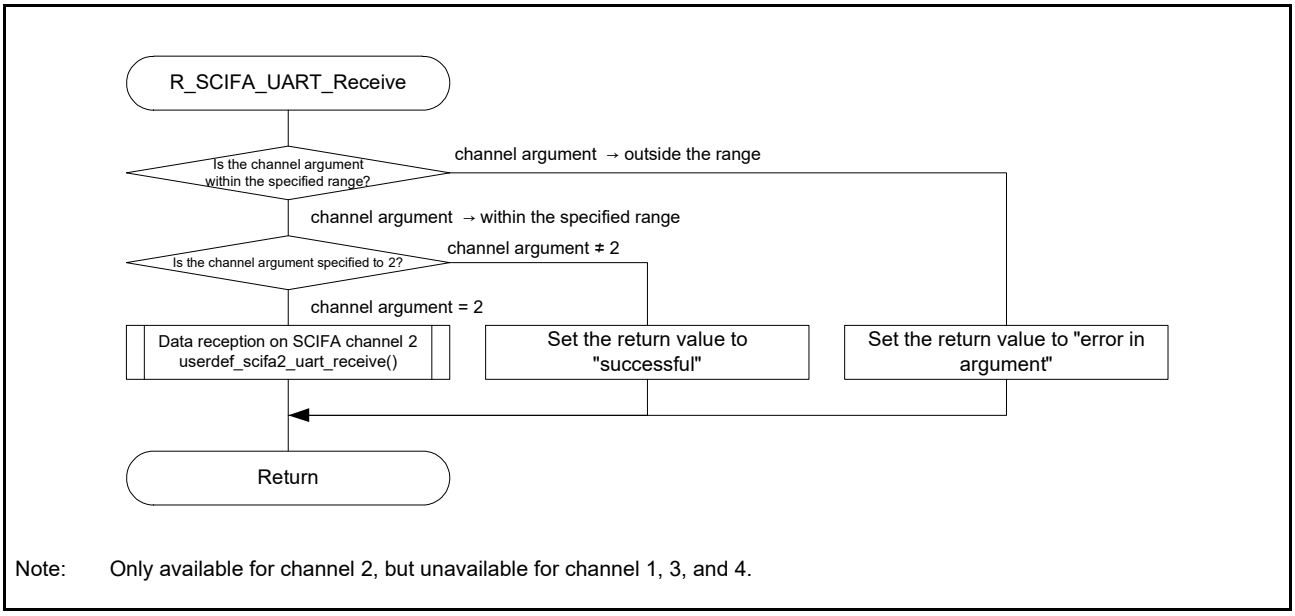


Note: Only available for channel 2, but unavailable for channel 1, 3, and 4.

Figure 6.8 Data Transmission

6.8.6 Data Reception

Figure 6.9 shows a flowchart of data reception processing.



Note: Only available for channel 2, but unavailable for channel 1, 3, and 4.

Figure 6.9 Data Reception

6.8.7 Initialization of SCIFA Channel 2 in UART Mode (User Defined)

Figure 6.10 and Figure 6.11 shows initialization of SCIFA channel 2 in UART mode (user defined).

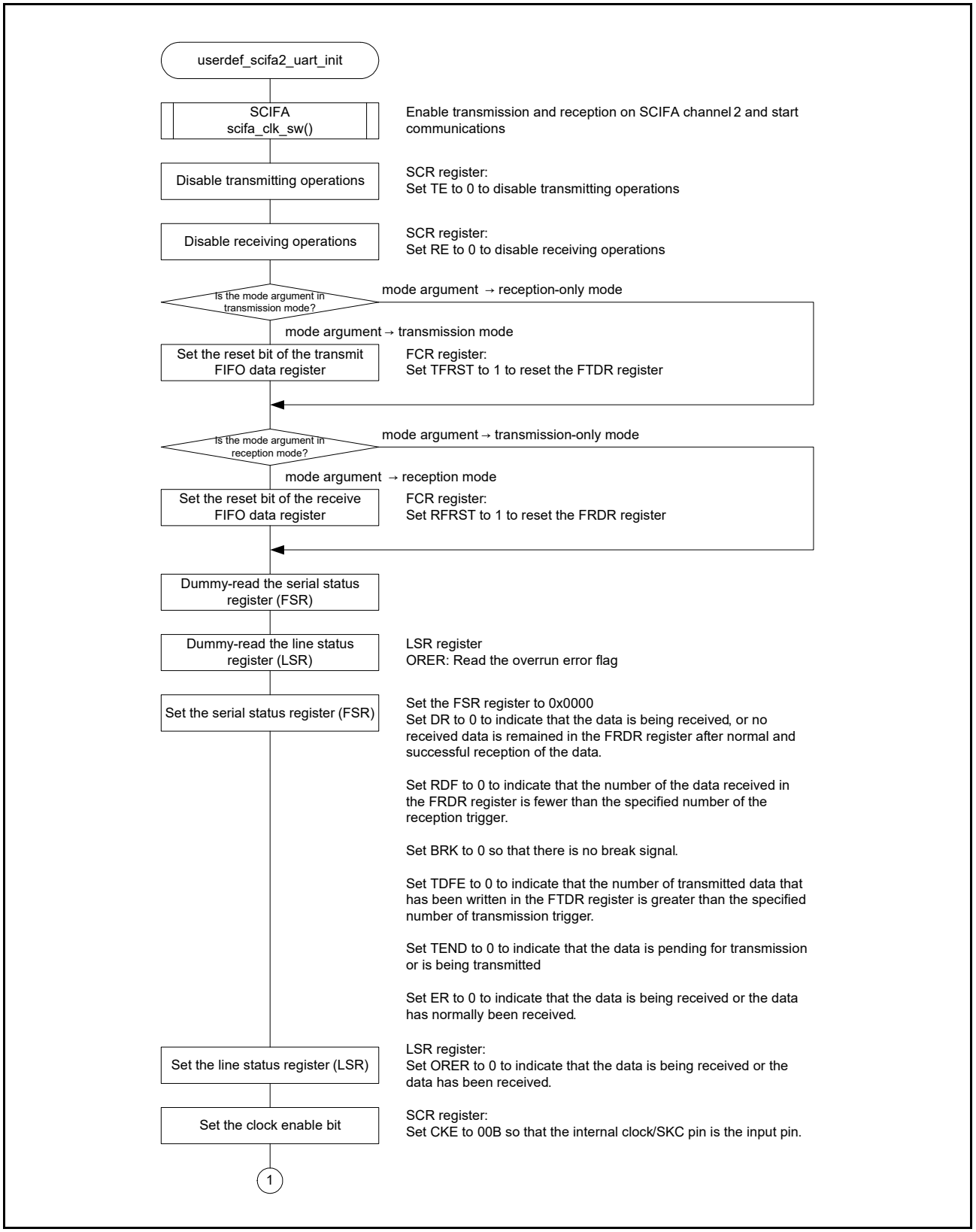


Figure 6.10 Initialization of SCIFA Channel 2 in UART Mode (User Defined) (1)

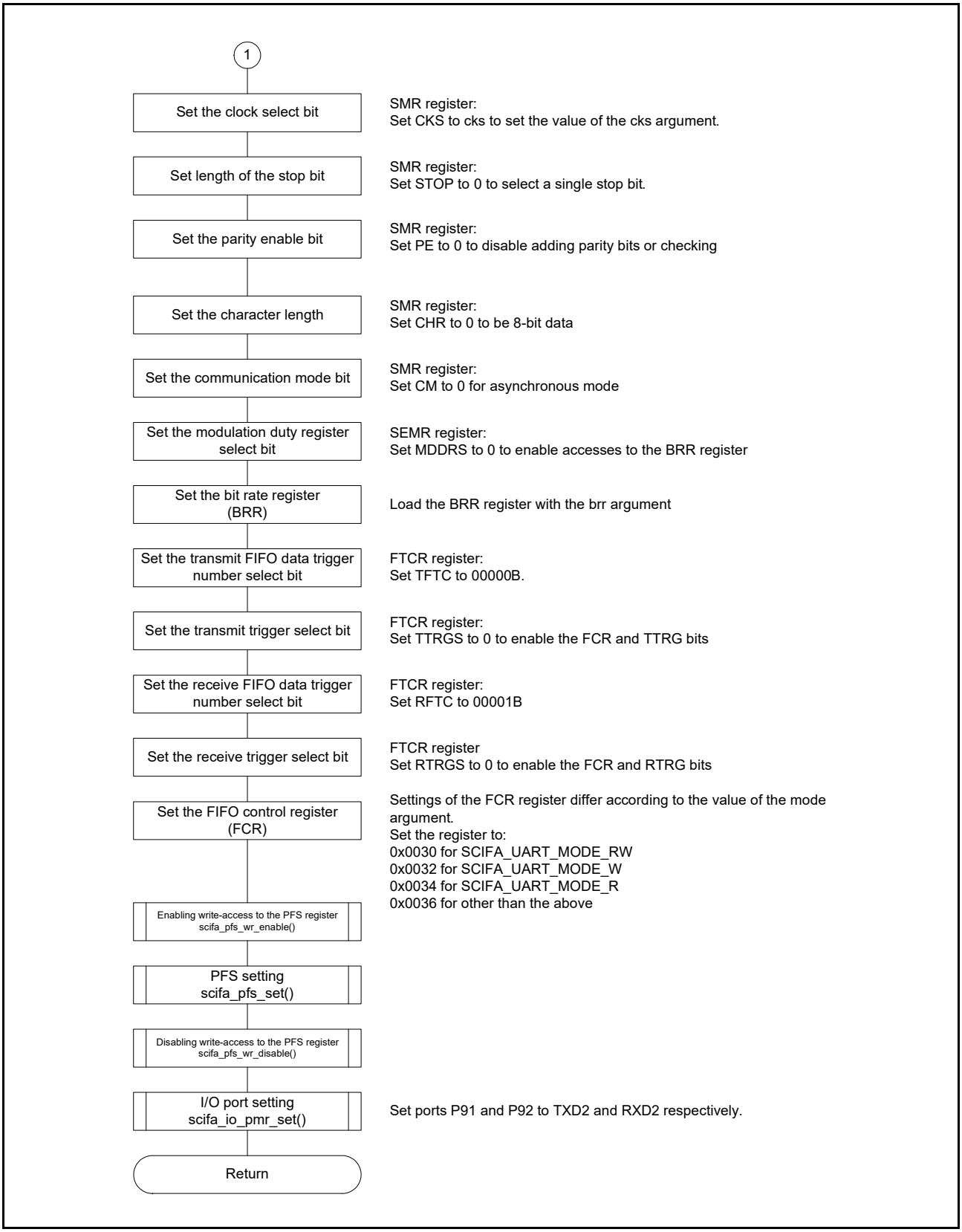


Figure 6.11 Initialization of SCIFA Channel 2 in UART Mode (User Defined) (2)

6.8.8 Startup of SCIFA Channel 2 in UART Mode (User Defined)

Figure 6.12 shows a flowchart of startup processing of SCIFA channel 2 in UART mode (user defined).

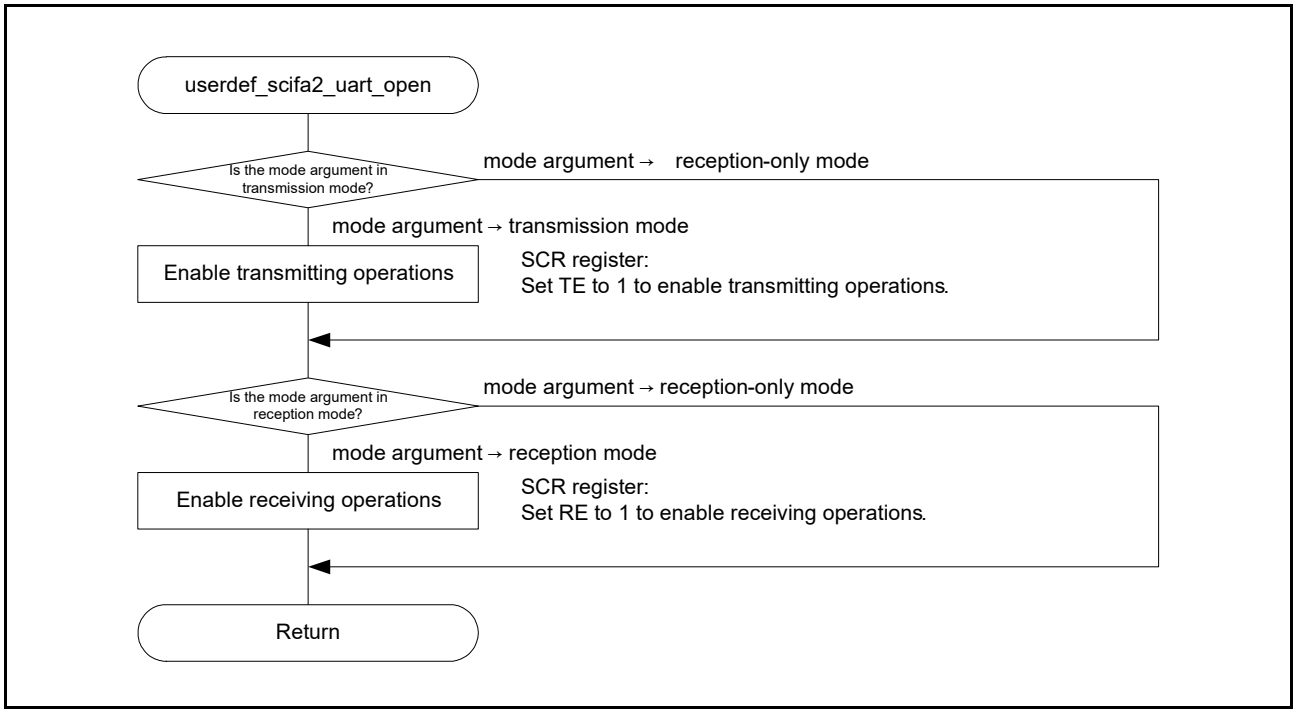


Figure 6.12 Startup of SCIFA Channel 2 in UART Mode (User Defined)

6.8.9 Data Transmission on SCIFA Channel 2 (User Defined)

Figure 6.13 shows a flowchart of data transmission processing of transmission of the SCIFA channel 2 (user defined).

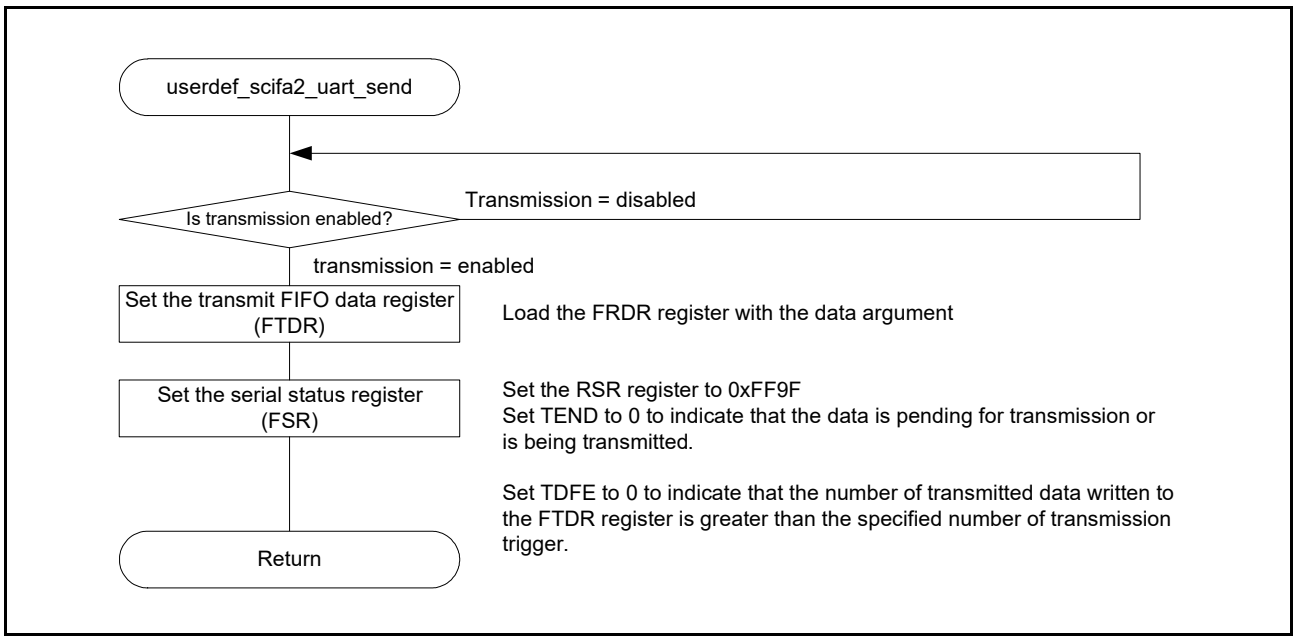


Figure 6.13 Transmission of SCIFA Channel 2 (User Defined)

6.8.10 Data Reception on SCIFA Channel 2 (User Defined)

Figure 6.14 shows a flowchart of data reception processing of data reception on SCIFA channel 2 (user defined).

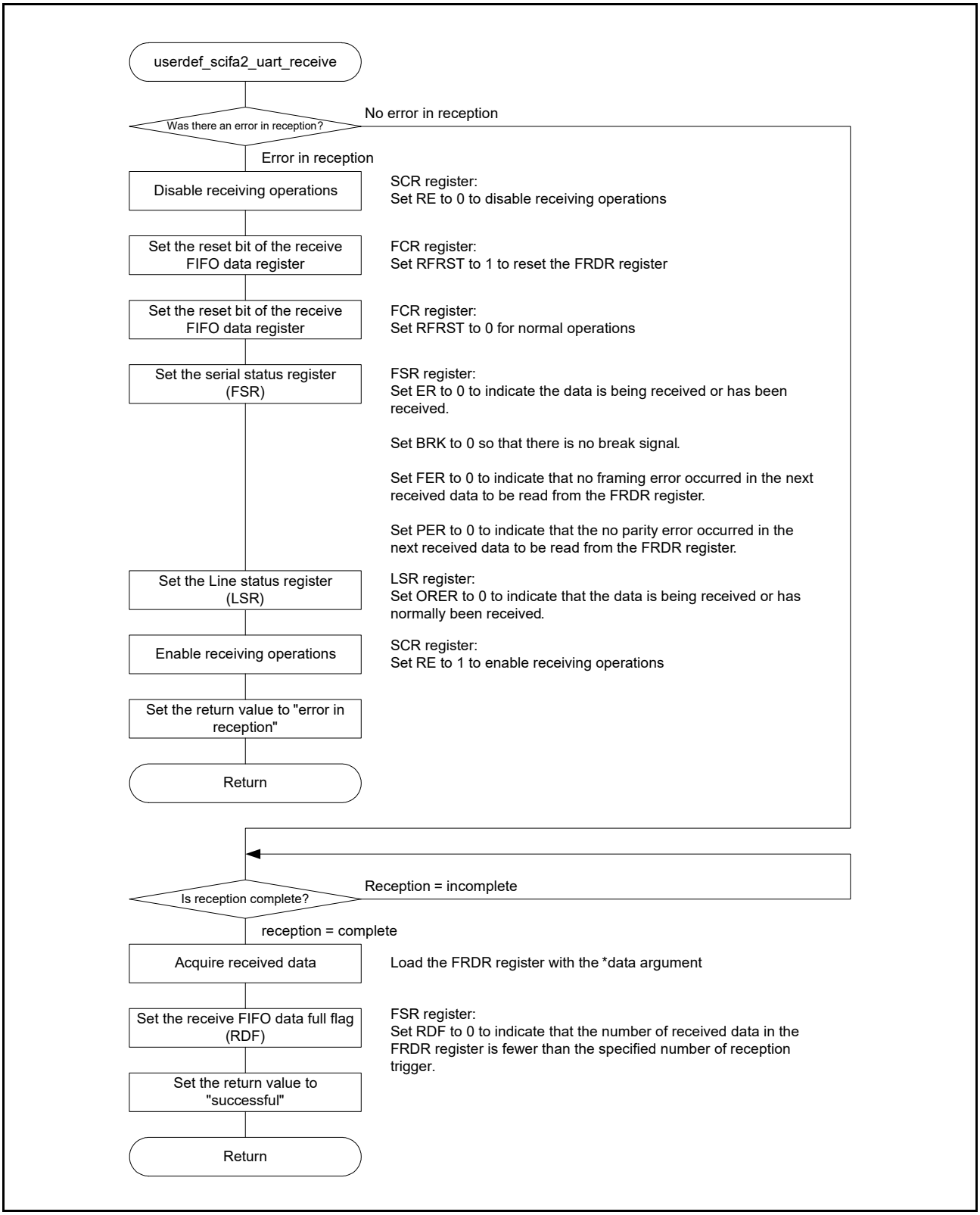


Figure 6.14 Data Reception on SICFA Channel 2 (User Defined)

7. Sample Program

The sample program is available on the Renesas Electronics website.

8. Reference Documents

User's manual: hardware:
RZ/T1 Group User's Manual: Hardware
(Download the latest version of the manual from the Renesas Electronics website.)

RZ/T1 Evaluation Board RTK7910022C00000BR User's Manual
(Download the latest version of the manual from the Renesas Electronics website.)

Technical Update / Technical News
(Download the latest version of the update or news from the Renesas Electronics website.)

User's manual: Development Environment
For IAR integrated development environment (IAR Embedded Workbench® for Arm), visit the IAR Systems website.
(Download the latest version from the IAR Systems website.)

Website and Support

Renesas Electronics website

http://www.renesas.com/

Inquiries

http://www.renesas.com/inquiry

Revision History	Application Note: FIFO Integrated Serial Communication Interface (SCIFA)

Rev.	Date	Description	
		Page	Summary
0.20	Mar. 18, 2015	—	First Edition issued
1.00	Apr. 10, 2015	—	Only the revision number was changed to be posted on a website.
1.10	Aug. 18, 2015	2. Operating Environment	
		5	Table 2.1 Operating Environment: Integrated Development Environment, partially amended and added
		6. Software	
		12	6.2.4 Required Memory Size: Description and reference added
		12	Table 6.2: Table title was partially amended
		12	Table 6.3 added
		13	Table 6.4 added
1.20	Dec. 04, 2015	2. Operating Environment	
		5	Table 2.1 Operating Environment: Integrated Development Environment, information partially amended
1.30	Apr. 05, 2017	2. Operating Environment	
		5	Table 2.1 Operating Environment: Integrated Development Environment, USB serial port driver for PC, modified
		6. Software	
		—	6.2.4 Required Memory Size, deleted
1.40	Jun. 07, 2018	2. Operating Environment	
		5	Table 2.1 Operating Environment: The description on the integrated development environment, modified
		5. Hardware	
		8	Figure 5.1 Hardware configuration example: The name of module, modified
		8. Related Documents	
		28	The name of IAR Embedded Workbench, modified

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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