RX71M Group, RX64M Group

Points of Difference Between RX71M Group and RX64M Group

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Introduction

This application note is intended as a reference for confirming the points of difference between the I/O registers of the RX71M group and RX64M group.

Target Device

- RX71M Group 177- and 176-pin versions, ROM capacity: 2 MB to 4 MB
- RX71M Group 145- and 144-pin versions, ROM capacity: 2 MB to 4 MB
- RX71M Group 100-pin version, ROM capacity: 2 MB to 4 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Comparison of Functions of RX71M Group and RX64M Group

A comparison of the functions of the RX71M group and RX64M group is provided below. For details of the functions, see 2., Comparative Overview of Functions, and 3., Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX71M and RX64M.

Table 1.1 Comparison of Functions of RX71M and RX64M

Function	Comparison Result
Voltage detection circuit (LVDA)	○
Clock generation circuit	△
Clock frequency accuracy measurement circuit (CAC)	○
Low-power consumption function	○
Battery backup function	○
Register write protection function	○
Interrupt controller (ICUA)	○
Buses	○
Memory-protection unit (MPU)	○
DMA controller (DMACAa)	○
DMA controller for the Ethernet controller (EDMACa)	○
Data transfer controller (DTCa)	○
Event link controller (ELC)	○
Multi-function pin controller (MPC)	○
Multi-function timer pulse unit 3 (MTU3a)	○
Port output enable 3 (POE3)	○
General PWM timer (GPTa)	○
16-bit timer pulse unit (TPUa)	○
Programmable pulse generator (PPG)	○
8-bit timer (TMR)	○
Compare match timer (CMT)	○
Compare match timer W (CMTW)	○
Realtime clock (RTCd)	○
Watchdog timer (WDTA)	○
Independent watchdog timer (IWDTa)	○
Ethernet controller (ETHERC)	○
PTP module for the Ethernet controller (EPTPC)	○
DMA module for the Ethernet controller (EDMACa)	○
USB 2.0 FS Host/Function module (USBb)	○
USB 2.0 Full-Speed Host/Function module (USBA): RX64M USB 2.0 Hi-Speed Host/Function module (USBAa): RX71M	△
Serial communications interface (SCIg, SCIh)	○
FIFO embedded serial communications interface (SCIFA)	○
I2C bus interface (RIICa)	○
CAN module (CAN)	○
Serial peripheral interface (RSPIa)	○
Quad serial peripheral interface (QSPI)	○
CRC calculator (CRC)	○
Serial sound interface (SSI)	○
Sampling rate converter (SRC)	○
SD host interface (SDHI)	○
MultiMediaCard interface (MMCIF)	○
Parallel data capture unit (PDC)	○

Function	Comparison Result
Boundary scan	○
AES: RX64M AESa: RX71M	○
DES	○
SHA: RX64M SHAa: RX71M	○
RNG	○
12-bit A/D converter (S12ADC)	○
12-bit D/A converter (R12DA)	○
Temperature sensor	○
Data operation circuit (DOC)	○
RAM	△
Standby RAM	○
Flash memory	△

Note: ○: Function implemented, △: Differences exist between implementations of function on RX71M and RX64M.

2. Comparative Overview of Functions

2.1 Clock Generation Circuit

Table 2.1 shows a comparative overview of clock generation circuit functions, and table 2.2 shows a comparison of clock generation circuit registers.

Table 2.1 Comparative Overview of Clock Generation Circuit Functions

Item	RX64M	RX71M
Application	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, EPTPC, USBA, RSPI, SCIF, MTU3, GPT, and AES. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12ADC. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB0 and the PHY in the USBA. • Generates the USBA clock (USBMCLK) to be supplied to the PHY in the USBA. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC subclock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, EPTPC, USBA, RSPI, SCIF, MTU3, GPT, and AES. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12ADC. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USB0 and the PHY in the USBA. • Generates the USBA clock (USBMCLK) to be supplied to the PHY in the USBA. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC subclock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX64M	RX71M
Operating frequency	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • USBMCLK: 20 MHz, 24 MHz • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 240 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • USBMCLK: 20 MHz, 24 MHz • CACCLK: Same as the clocks from the respective oscillators. • CANMCLK: 24MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and MTU3 and GPT output can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and MTU3 and GPT output can be forcedly driven to high-impedance.
Subclock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT
PLL frequency synthesizer	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock sources: Main clock, HOCO • Input pulse frequency division ratio: Selectable from ×1/1, ×1/2, and ×1/3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication factor: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control

Item	RX64M	RX71M
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2	• Selectable between BCLK clock output and high output • Selectable between BCLK and BCLK ×1/2
Control of output on SDCLK pin	Selectable between SDCLK clock output and high output SDCLK	Selectable between SDCLK clock output and high output SDCLK
Event linking (output)	Detection of stopping of main clock oscillator	Detection of stopping of main clock oscillator
Event linking (input)	Switching of clock source to low-speed on-chip oscillator	Switching of clock source to low-speed on-chip oscillator

Table 2.2 Comparison of Clock Generation Circuit Registers

Register	Bit	RX64M	RX71M
MEMWAIT	MEMWAIT	—	Memory wait cycle setting register

2.2 USB 2.0 Hi-Speed Host/Function Module (USBAa)

Table 2.3 shows a comparative overview of the USBA modules, and table 2.4 shows a comparison of USBA registers.

Table 2.3 Comparative Overview of USBA Functions

Item	RX64M (USBA)	RX71M (USBAa)
Features	• Incorporates a USB device controller (UDC) and transceiver for USB 2.0 Host controller and Function controller operations are provided, and the on-the-go (OTG) functionality is supported. • Host controller and Function controller operations are switchable by software.	• Incorporates a USB device controller (UDC) and transceiver for USB 2.0 Host controller and Function controller operations are provided, and the on-the-go (OTG) functionality is supported. • Host controller and Function controller operations are switchable by software.
	Host controller operation: • Support for full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • Automatic scheduling of start-of-frame (SOF) packets and other packet transmissions • Programmable intervals for isochronous and interrupt transfers • Communications with multiple peripheral devices connected via a single hub	Host controller operation: • Support for high-speed transfer (480 Mbps), full-speed transfer (12 Mbps), and low-speed transfer (1.5 Mbps) • Automatic scheduling of start-of-frame (SOF) packets and other packet transmissions • Programmable intervals for isochronous and interrupt transfers • Communications with multiple peripheral devices connected via a single hub
	Function controller operation: • Support for full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto-response function for SetAddress() request • SOF recovery function	Function controller operation: • Support for high-speed transfer (480 Mbps) and full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto-response function for SetAddress() request • SOF recovery function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer

Item	RX64M (USBA)	RX71M (USBAa)
Pipe configuration	• FIFO buffer of up to 8.5 KB for USB communications • Up to 10 pipes can be selected (including the default control pipe). • Programmable pipe configurations • Endpoint numbers can be assigned flexibly to pipes 1 to 9.	• FIFO buffer of up to 8.5 KB for USB communications • Up to 10 pipes can be selected (including the default control pipe). • Programmable pipe configurations • Endpoint numbers can be assigned flexibly to pipes 1 to 9.
	Transfer conditions that can be set for each pipe: • Pipe 0: Control transfer, 64-byte fixed single buffer • Pipes 1 and 2: Bulk transfer or isochronous transfer in continuous transfer mode, programmable buffer size (up to 2 KB, double buffer mode selectable) • Pipes 3 to 5: Bulk transfer in continuous transfer mode, programmable buffer size (up to 2 KB, double buffer mode selectable) • Pipes 6 to 9: Interrupt transfer, 64-byte fixed single buffers	Transfer conditions that can be set for each pipe: • Pipe 0: Control transfer, 64-byte fixed single buffer • Pipes 1 and 2: Bulk transfer or isochronous transfer in continuous transfer mode, programmable buffer size (up to 2 KB, double buffer mode selectable) • Pipes 3 to 5: Bulk transfer in continuous transfer mode, programmable buffer size (up to 2 KB, double buffer mode selectable) • Pipes 6 to 9: Interrupt transfer, 64-byte fixed single buffers
Other functions	• Transfer ending function using transaction count • Function that changes the BRDY interrupt event notification timing • Function that automatically clears the FIFO buffer after the data for the pipe specified at the D0FIFO port or D1FIFO port has been read • NAK setting function for response PID generated by end of transfer • Internal pull-up and pull-down resistors for D+ and D− • Support for USB 2.0 ECN for Link Power Management (LPM). A new sleep state (referred to as the L1 state) is available. • Support for Battery Charging Specification, Revision 1.2 • To reduce power consumption, a classic-only mode (CL-only mode) where operation emulates the USB 1.1 standard is selectable.	• Transfer ending function using transaction count • Function that changes the BRDY interrupt event notification timing • Function that automatically clears the FIFO buffer after the data for the pipe specified at the D0FIFO port or D1FIFO port has been read • NAK setting function for response PID generated by end of transfer • Internal pull-up and pull-down resistors for D+ and D− • Support for USB 2.0 ECN for Link Power Management (LPM). A new sleep state (referred to as the L1 state) is available. • Support for Battery Charging Specification, Revision 1.2 • To reduce power consumption, a classic-only mode (CL-only mode) where operation emulates the USB 1.1 standard is selectable.

Table 2.4 Comparison of USBA Registers

Register	Bit	RX64M	RX71M
SYSCFG	USBE	USB operation enable bit	USB operation enable bit
	DPRPU	D+ line resistor control bit	D+ line resistor control bit
	DRPD	D+/D− line resistor control bit	D+/D− line resistor control bit
	DCFM	Controller operation select bit	Controller operation select bit
	HSE	—	High-speed operation enable bit
	CNEN	Single end receiver enable bit	Single end receiver enable bit
TESTMODE	UTST	—	Test mode bits
UFRMNUM	UFRNM	—	μframe number bits
DCPCTR	PID	Response PID bits	Response PID bits
	CCPL	Control transfer end enable bit	Control transfer end enable bit
	PINGE	—	PING token issue enable bit
	PBUSY	Pipe busy flag	Pipe busy flag
	SQMON	Sequence toggle bit monitor flag	Sequence toggle bit monitor flag
	SQSET	Sequence toggle bit set bit	Sequence toggle bit set bit
	SQCLR	Sequence toggle bit clear bit	Sequence toggle bit clear bit
	SUREQCLR	SUREQ bit clear bit	SUREQ bit clear bit
	CSSTS	—	CSSTS status flag
	CSCLR	—	CSSTS status flag clear bit
	SUREQ	SETUP token transmission bit	SETUP token transmission bit
	BSTS	Buffer status flag	Buffer status flag
PIPEnCTR	PID	Response PID bits	Response PID bits
	PBUSY	Pipe busy flag	Pipe busy flag
	SQMON	Sequence toggle bit monitor flag	Sequence toggle bit monitor flag
	SQSET	Sequence toggle bit set bit	Sequence toggle bit set bit
	SQCLR	Sequence toggle bit clear bit	Sequence toggle bit clear bit
	ACLRM	Auto buffer clear mode bit	Auto buffer clear mode bit
	ATREPM	Auto response mode bit	Auto response mode bit
	CSSTS	—	CSSTS status flag
	CSCLR	—	CSPLIT status clear bit
	INBUFM	Transmit buffer monitor flag	Transmit buffer monitor flag
	BSTS	Buffer status flag	Buffer status flag
DEVADDm	USBSPD	Transfer speed of communication target device bits	Transfer speed of communication target device bits
	HUBPORT	—	HUB port connected for communication bits
	UPPHUB	—	HUB register connected for communication bits

2.3 RAM

Table 2.5 shows a comparative overview of RAM functions.

Table 2.5 Comparative Overview of RAM Functions

	RX64M		RX71M	
Item	**Without ECC Error Correction**	**With ECC Error Correction (ECCRAM)**	**Without ECC Error Correction**	**With ECC Error Correction (ECCRAM)**
RAM capacity	512 KB (RAM0: 512 KB)	32 KB	512 KB (RAM0: 512 KB)	32 KB
RAM address	RAM0: 0000 0000h to 0007 FFFFh	ECCRAM: 00FF 8000h to 00FF FFFFh	RAM0: 0000 0000h to 0007 FFFFh	ECCRAM: 00FF 8000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 3 (ECCRAM)	Memory bus 1	Memory bus 3 (ECCRAM)
Access	• Single-cycle access for both reading and writing • Ability to enable or disable RAM	• Ability to enable or disable ECCRAM • ECC function disabled: Access in two cycles for both reading and writing • ECC function enabled (when no error has occurred): Access in two cycles for both reading and writing • ECC function enabled (when an error has occurred): Access in three cycles for both reading and writing	• Single-cycle access for both reading and writing However, access to addresses in the range from 0004 0000h to 0007 FFFFh when MEMWAIT = 1 (this setting is required when the ICLK frequency is above 120 MHz) takes two cycles for reading or writing. • Ability to enable or disable RAM	• Ability to enable or disable ECCRAM [MEMWAIT = 0] • Access in two cycles for both reading and writing when ECC function disabled • ECC function enabled (when no error has occurred): Reading takes three cycles and writing takes two cycles. • Access in three cycles for both reading and writing when ECC function enabled (and an error has occurred) [MEMWAIT = 1] • ECC function disabled: Access in three cycles for both reading and writing • ECC function enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • ECC function enabled (when an error has occurred): Access takes five cycles whether for reading or writing.

	RX64M		RX71M	
Item	**Without ECC Error Correction**	**With ECC Error Correction (ECCRAM)**	**Without ECC Error Correction**	**With ECC Error Correction (ECCRAM)**
Data retention function	Data retention function not available in deep software standby mode	Data retention function not available in deep software standby mode	Data retention function not available in deep software standby mode	Data retention function not available in deep software standby mode
Low-power consumption function	Ability to select module-stop state	Ability to select module-stop state	Ability to select module-stop state	Ability to select module-stop state
Error checking	None	• Correction of 1-bit errors and detection of 2-bit errors • Generation of a non-maskable interrupt or interrupt when an error occurs	None	• Correction of 1-bit errors and detection of 2-bit errors • Generation of a non-maskable interrupt or interrupt when an error occurs

2.4 Flash Memory

Table 2.6 shows a comparative overview of the code flash memory and data flash memory.

Table 2.6 Comparative Overview of Code Flash Memory and Data Flash Memory

	RX64M		RX71M	
Item	**Code Flash Memory**	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Memory capacity	• User area: Max. 4 MB • User boot area: 32 KB	Data area: 64 KB	• User area: Max. 4 MB • User boot area: 32 KB	Data area: 64 KB
Advanced fetch unit (AFU)	—	—	Separation of instructions and operands	Out of the scope of caching
Read cycles	One cycle of ICLK for high-speed read operation	Eight cycles of FCLK for a read operation in words or bytes	Instructions • When branching occurs When the AFU is hit: No cycles When the AFU is missed: One cycle if ICLK ≤ 120 MHz Two cycles if ICLK > 120MHz • When no branching occurs One cycle if ICLK ≤ 120 MHz Two cycles if ICLK > 120MHz Operands When the AFU is hit: One cycle When the AFU is missed: Two cycles if ICLK ≤ 120 MHz Three cycles if ICLK > 120MHz	Six cycles of FCLK for a read operation in words or bytes
Value after erasure	FFh	Undefined	FFh	Undefined
Programming/ erasing method	• Programming and erasing of code flash and data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming of flash memory by a user program (self-programming)		• Programming and erasing of code flash and data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming of flash memory by a user program (self-programming)	
Security function	Protection against illicit tampering with or reading of data in flash memory		Protection against illicit tampering with or reading of data in flash memory	
Protection function	Protects against erroneous programming of the flash memory.		Protects against erroneous programming of the flash memory.	

Item	RX64M		RX71M	
	Code Flash Memory	**Data Flash Memory**	**Code Flash Memory**	**Data Flash Memory**
Trusted memory (TM) function	Protects against illicit reading of blocks 8 and 9 in the code flash memory.		Protects against illicit reading of blocks 8 and 9 in the code flash memory.	
Background operation (BGO) function	The code flash memory can be read while the code flash memory is being programmed. The code flash memory can be read while the data flash memory is being programmed.		The code flash memory can be read while the code flash memory is being programmed. The code flash memory can be read while the data flash memory is being programmed.	
Programming and erasure unit	• Unit of programming for user area or user boot area: 256 bytes • Unit of erasure for user area: Block	• Unit of programming for data area 4 bytes • Unit of erasure for data area: 64 bytes	• Unit of programming for user area or user boot area: 256 bytes • Unit of erasure for user area: Block	• Unit of programming for data area 4 bytes • Unit of erasure for data area: 64 bytes
Other functions	Interrupts can be accepted during self-programming.		Interrupts can be accepted during self-programming.	
	Option-setting memory can be specified in the initial settings of the microcontroller.		Option-setting memory can be specified in the initial settings of the microcontroller.	
On-board programming (four types)	Programming in boot mode (SCI interface) • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • The user boot area can also be programmed. Programming in boot mode (USB interface) • USBb is used. • Dedicated hardware is not required; direct connection to a PC is possible. Programming in user boot mode • The user can create original boot programs. Programming by a routine for code flash memory or data flash memory programming within the user program • Code flash memory or data flash memory can be programmed without resetting the system.		Programming in boot mode (SCI interface) • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. • The user boot area can also be programmed. Programming in boot mode (USB interface) • USBb is used. • Dedicated hardware is not required; direct connection to a PC is possible. Programming in user boot mode • The user can create original boot programs. Programming by a routine for code flash memory or data flash memory programming within the user program • Code flash memory or data flash memory can be programmed without resetting the system.	
Off-board programming (for products with 100 or more pins)	A flash programmer can be used to program the user area and user boot area.	A flash programmer cannot be used to program the data area.	A flash programmer can be used to program the user area and user boot area.	A flash programmer cannot be used to program the data area.

3. Reference Documents

User's Manual: Hardware

RX64M Group User's Manual: Hardware Rev.1.00 (R01UH0377EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

RX71M Group User's Manual: Hardware Rev.1.00 (R01UH0493EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website
http: //www.renesas.com/

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun. 11, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
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5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
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