RX630 Group

Interrupt Request Grouping (Level Detection Interrupt Requests)

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Introduction

This application note describes the settings used to group interrupt requests when the RX630 SCI (serial communications interface) module is used.

Target Device

RX630 Group

This application note can also be used with other RX family microcontrollers that have the same I/O registers (peripheral unit control registers) as the RX630 Group products. Note, however, that since there are changes between devices, such as additional functionality in certain functions, these operations must be verified with the manual for the device actually used. When using the methods described in this application note, full testing in the actual user system is required.

Contents

1. Specifications

Group interrupt operation, in which multiple interrupts are allocated to a single interrupt vector, is used when the SCI (serial communications interface) asynchronous serial transfer function is used. Figure 1.1 presents an overview of asynchronous serial reception using the group interrupt function and table 1.1 lists the peripheral function used and their uses.

1. SCI channels 0 and 2 are used.
2. The communication format is 8-bit data, 1 stop bit, no parity.
3. Reception operation consists of transferring the SCI receive data to an arbitrary receive buffer provided in advance on the receive data full interrupt.
4. For receive errors, the group interrupt function level detection interrupt group (group 12) is used to handle receive errors.

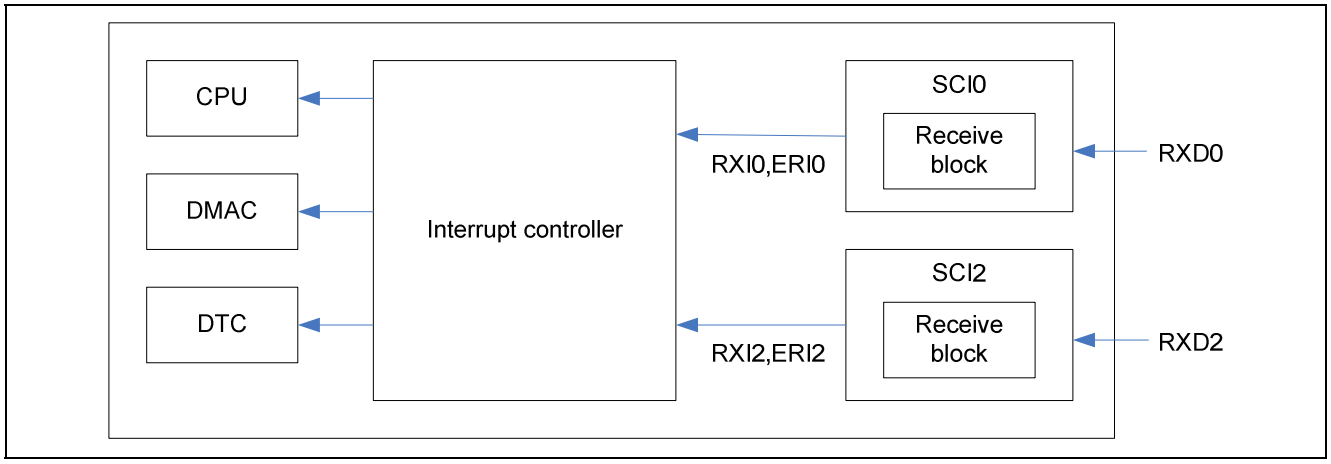

Figure 1.1 Overview of Asynchronous Serial Data Reception Using the Group Interrupt Function

Table 1.1 Peripheral Functions and their Uses

Peripheral Function	Use
Interrupt controller	• Peripheral function interrupts • Group interrupt function: Allocates multiple interrupts to a single interrupt vector. Here, a level detection interrupt group (group 12) is used. • Unit selection function: Not used • External pin interrupts: Not used • Software interrupts: Not used • DTC and DMAC control: Not used • Nonmaskable interrupts: Not used
SCI (serial communication)	• Channels used: channels 0 and 2 • Communication mode: Asynchronous communication mode • Interrupts: Receive data full interrupt (RXI) and receive error interrupt (ERI) • Transfer rate: 38,400 bps (PCLK = 50 MHz) • Data length: 8 bits • Stop bits:1 stop bit • Parity: No parity

2. Conditions of Checking the Operation of the Software

The sample code described in this application note has been confirmed to run normally under the operating conditions given below.

Table 2.1 Operating Conditions

Item	Description
MCU	RX630 (R5F5630EDDFP)
Memory used for evaluation	Xin clock: 12 MHz Subclock: 32.768 kHz
Operating voltage	3.3 V
Integrated development environment	Version 4.09.00.007
C compiler	RX Standard Toolchain (V.1.0.1.0) C/C++ compiler package for RX family V.1.01.00
	Compiler options: The default settings for the integrated development environment are used.
Operating mode	Single chip mode
Version of the sample code	Version 1.40
Board used	R0K505630C001BR

3. Software Description

In this application example, the SCI asynchronous serial transfer function is used with group interrupt operation with multiple interrupts allocated to a single vector.

3.1 Overview of Interrupt Controller Operation

The interrupt controller performs the following processing.

- Interrupt detection
- Interrupt enable/disable control
- Interrupt request source (CPU interrupt, DTC activation, DMAC activation) selection
- Interrupt priority discrimination

See the RX630 Group Hardware Manual Interrupt Controller (ICUb) for details on the interrupt controller.

Table 3.1 Interrupt Controller Overview

Item		Description
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: edge or level detection The detection method is fixed for each connected peripheral module. • Group interrupt function: Multiple interrupts are allocated to a single interrupt vector. Number of edge detection interrupt groups: 7 (groups 0 to 6) Number of level detection interrupt groups: 1 (group 12) • Unit selection function: Selects one of two interrupt requests. Number of units: 6
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ15 • Number of factors: 16 • Interrupt detection: one of low level, falling edge, rising edge, or both edges can be selected for each factor. • Digital filter function: provided
	Software interrupts	• Interrupts due to register write operations • Number of factors: 1
	Interrupt priorities	The priority level is set with registers.
	High-speed interrupt function	Can speed up CPU interrupt handling Only one factor can be specified.
	DTC and DMAC control	The DTC and DMAC units can be started by interrupts.
Nonmaskable interrupts	NMI pin interrupts	• Interrupt from the NMI pin • Interrupt detection: falling edge or rising edge • Digital filter function: provided
	Oscillator stop detection	Interrupt issued when an oscillator stop event is detected
	WDT underflow/ refresh error	Interrupt issued when the counter underflows in interval timer mode
	IWDT underflow/ refresh error	Interrupt issued when the decrement counter underflows
	Voltage monitor 1 interrupt	Voltage monitor interrupt for voltage detection circuit 1 (LVD1)
	Voltage monitor 2 interrupt	Voltage monitor interrupt for voltage detection circuit 2 (LVD2)

3.2 Overview of Serial Communications Interface (SCI) Operation

In SCI asynchronous mode, characters, which consist of 1 start bit that indicates the start of communication, 1 stop bit that indicates the end of communication, and a character added to the data, are transmitted or received in single character units in serial communications while synchronizing operation. Since both the send and receive blocks are double buffered, data can be read or written while transmission is in progress.

In asynchronous serial communication, the communication line is normally held in the mark state (high level). The SCI module monitors the communication line and if it detects a space (low level), it sees that as a start bit and starts a serial communication operation.

A single character in serial communications starts with a start bit (low level) and then consists of data (LSB first, i.e. it starts with the low-order bit), a parity bit (high or low), and finally a stop bit (high level) in that order.

See the section on the serial communications interface (SCIc, SCId) in the RX630 Group Hardware Manual for details on the SCI module.

Table 3.2 presents an overview of asynchronous communication.

Table 3.2 Overview of Asynchronous Serial Communication

Item	Description
Number of channels	13 channels (SCIc: 12 channels + SCId: 1 channel)
Transfer rate	Any baud rate can be set using the built-in baud rate generator.
Clock sources	Internal clocks: PCLK, PCLK/4, PCLK/16, and PCLK/64 (PCLK: peripheral module clock) External clock: Clock signal input to the SCKn pin
Data format	Transfer data lengths: 7 or 8 bits Transmit stop bits: 1 or 2 stop bits Parity function: Even, odd, or no parity Transfer orders: LSB first or MSB first When an internal clock is selected for the baud rate generator: 100 to 1,562,500 bps (when PCLK = 50 MHz) When a external clock is selected: Up to 781,250 bps (when PCLK = 50 MHz)
Error detection	Parity, overrun, and framing errors can be detected
Interrupt requests	Transmit data empty interrupt (TXI) Receive data full interrupt (RXI) Receive error interrupt (ERI) Transmit complete interrupt (TEI)
Clock source selection	Either an internal or an external clock can be selected.

3.3 Operational Overview

Table 3.3 lists the settings and conditions for the SCI communication function as used in this application example. Figure 3.1 shows the timing for this operation.

Table 3.3 SCI Settings and Conditions

Channels used	SCI0, SCI2
Communication mode	Asynchronous mode
Interrupts	• Receive data full interrupt (RXI) • Receive error interrupt (ERI)
Transfer rate	38,400 bps (PCLK = 50 MHz)
Data length	8 bits of data
Stop bits	One stop bit
Parity	None

Reception operation example

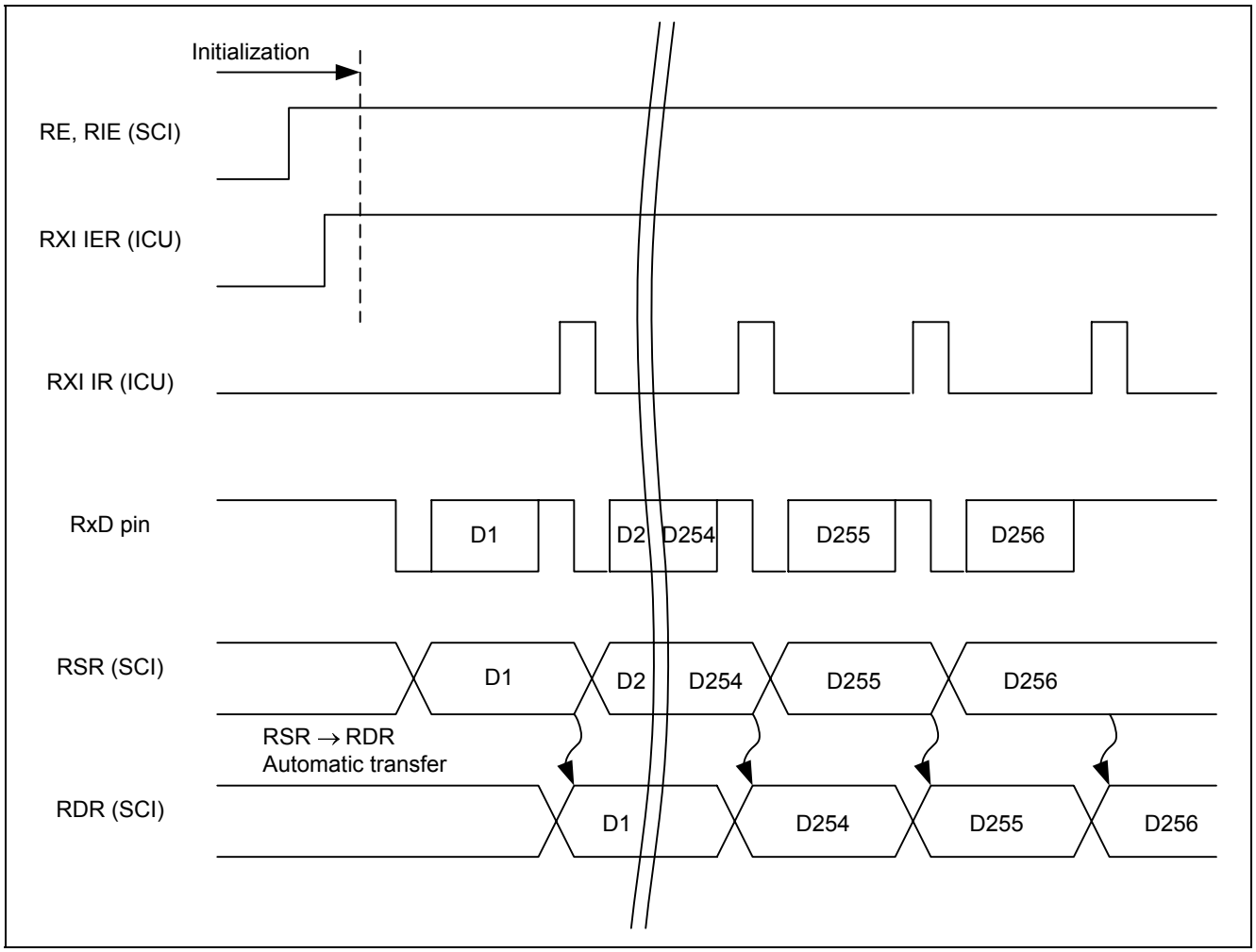

Figure 3.1 Operation Timing

3.4 File Structure

Table 3.4 lists the files used in the sample code.

Table 3.4 File Structure

File Name	Function	Notes
main_int_req_grouping.c	• The main processing • Interrupt grouping control related processing • SCI interrupt processing	
dbsct.c	B and R section settings	File automatically generated by the IDE
intprg.c	Interrupt handling (The SCI interrupt handler, which is used by this program, has been removed from this file.)	File automatically generated by the IDE
resetprg.c	Reset handling	File automatically generated by the IDE
sbrk.c	sbrk() function	File automatically generated by the IDE
vecttbl.c	Vector table related processing	File automatically generated by the IDE to which option and memory settings have been added
iodefine.h	I/O register related header file	
lowsrc.h	I/O streams related header file	File automatically generated by the IDE
sbrk.h	sbrk() function header file	File automatically generated by the IDE
stacksct.h	Stack area header file	File automatically generated by the IDE
typedefine.h	Integer type definitions header file	File automatically generated by the IDE
vect.h	Vector table related header file	File automatically generated by the IDE

3.5 Constants

Table 3.5 lists the constants used by the sample code.

Table 3.5 Constants Used in the Sample Code

Constant	Set Value	Description
None		

3.6 Variables

Table 3.6 lists the global variables.

Table 3.6 Global Variables

Type	Name	Description	Functions Where Used
unsigned char	RcvBuf0[256]	Array for storing SCI0 receive data	main, SCI0_Receive
unsigned char	RcvBuf2[256]	Array for storing SCI2 receive data	main, SCI2_Receive
unsigned char	RcvCount0	Pointer to array for storing SCI0 receive data	main, SCI0_Receive
unsigned char	RcvCount2	Pointer to array for storing SCI2 receive data	main, SCI2_Receive

3.7 Functions

Table 3.7 lists the functions defined in the sample code.

Table 3.7 Functions

Function Name	Overview
mcu_init	CPU initialization
clock_setting	CPU clock settings
peripheral_init	Peripheral function initialization
SCI_init	Serial communications interface (SCI) related initialization
SCI0_Receive	Serial communications interface (SCI0) reception processing
SCI2_Receive	Serial communications interface (SCI2) reception processing
Int_SCI0_RXI0	Serial communications interface (SCI0) receive interrupt handling
Int_SCI2_RXI2	Serial communications interface (SCI2) receive interrupt handling

3.8 Function Specifications

This section lists the specifications of the functions in the sample code.

Name	mcu_init
Overview	CPU initialization
Header	Iodefine.h
Declaration	void mcu_init(void)
Description	Sets the CPU clock
Arguments	None
Return values	None
Notes	

Name	clock_setting
Overview	Sets the CPU clock.
Header	Iodefine.h
Declaration	void clock_setting(void)
Description	• Stops the subclock oscillator. • Stops the high-speed clock oscillator. • Sets the oscillator stabilization time for the main clock oscillator to 131,072 cycles. • Sets the PLL oscillator stabilization time to 4,194,304 cycles. • Sets the PLL frequency multiplier to 16x. • Sets the main clock oscillator to the operating state. • Sets the PLL circuit to the operating state. • Sets the system clock to divided by 2, the FlashIF clock to divided by 4, the external bus clock to divided by 4, and the peripheral module clock to divided by 4. • Sets the clock source to be the PLL circuit.
Arguments	None
Return values	None
Notes	

Name	peripheral_init
Overview	Peripheral function initialization
Header	Iodefine.h
Declaration	void peripheral_init(void)
Description	Initializes SCI related items.
Arguments	None
Return values	None
Notes	

Name	SCI_init
Overview	Serial communications interface (SCI) related initialization
Header	Iodefine.h
Declaration	void SCI_init(void)
Description	• Clears the SCI0 module stop state. • Clears the SCI2 module stop state. • Pin settings: Sets the P20 (TxD0) and P21 (RxD0) pins to function as SCI0 pins. • Pin settings: Sets the P50 (TxD2) and P52 (RxD2) pins to function as SCI2 pins. • Disables SCI0 serial reception operation (RE) and also disables serial transmission operation (TE). • Sets the SCI0 clock to PCLK, disables multiprocessor communication functions, and sets SCI0 to 1 stop bit, no parity, 8-bit data, transmit/receive, asynchronous mode operation. • Sets the SCI0 smart card selection to serial communications interface mode. • Sets the SCI0 baud rate to 38,400 bps. • Disables SCI2 serial reception operation (RE) and also disables serial transmission operation (TE). • Sets the SCI2 clock to PCLK, disables multiprocessor communication functions, and sets SCI2 to 1 stop bit, no parity, 8-bit data, transmit/receive, asynchronous mode operation. • Sets the SCI2 smart card selection to serial communications interface mode. • Sets the SCI2 baud rate to 38,400 bps. • Sets the SCI serial reception error interrupt grouping interrupt level to level 1. • Sets the SCI0 reception interrupt grouping interrupt level to level 1. • Sets the SCI2 reception interrupt grouping interrupt level to level 1. • Sets SCI0 to internal clock operation, and the clock I/O pin to be an I/O port. Disables the TEI interrupt, enables serial reception operation, disables serial transmission operation, enables the RXI and ERI interrupts, and disables the TXI interrupt. • Sets SCI2 to internal clock operation, and the clock I/O pin to be an I/O port. Disables the TEI interrupt, enables serial reception operation, disables serial transmission operation, enables the RXI and ERI interrupts, and disables the TXI interrupt.
Arguments	None
Return values	None
Notes	

Name	SCI0_Receive
Overview	Serial communications interface (SCI0) reception processing
Header	Iodefine.h
Declaration	void SCI0_Receive(void)
Description	• Stores the SCI0 receive data in a receive buffer. • Updates the receive pointer.
Arguments	None
Return values	None
Notes	

Name	SCI2_Receive
Overview	Serial communications interface (SCI2) reception processing
Header	Iodefine.h
Declaration	void SCI2_Receive(void)
Description	• Stores the SCI2 receive data in a receive buffer. • Updates the receive pointer.
Arguments	None
Return values	None
Notes	

Name	Int_SCI0_RXI0
Overview	Serial communications interface (SCI0) receive interrupt handling
Header	None
Declaration	void Int_SCI0_RXI0(void)
Description	Performs the serial communications interface (SCI0) reception processing.
Arguments	None
Return values	None
Notes	

Name	Int_SCI0_RXI2
Overview	Serial communications interface (SCI2) receive interrupt handling
Header	None
Declaration	void Int_SCI0_RXI2(void)
Description	Performs the serial communications interface (SCI2) reception processing.
Arguments	None
Return values	None
Notes	

3.9 Flowcharts

3.9.1 Main Processing

Figure 3.2 shows the main processing flowchart.

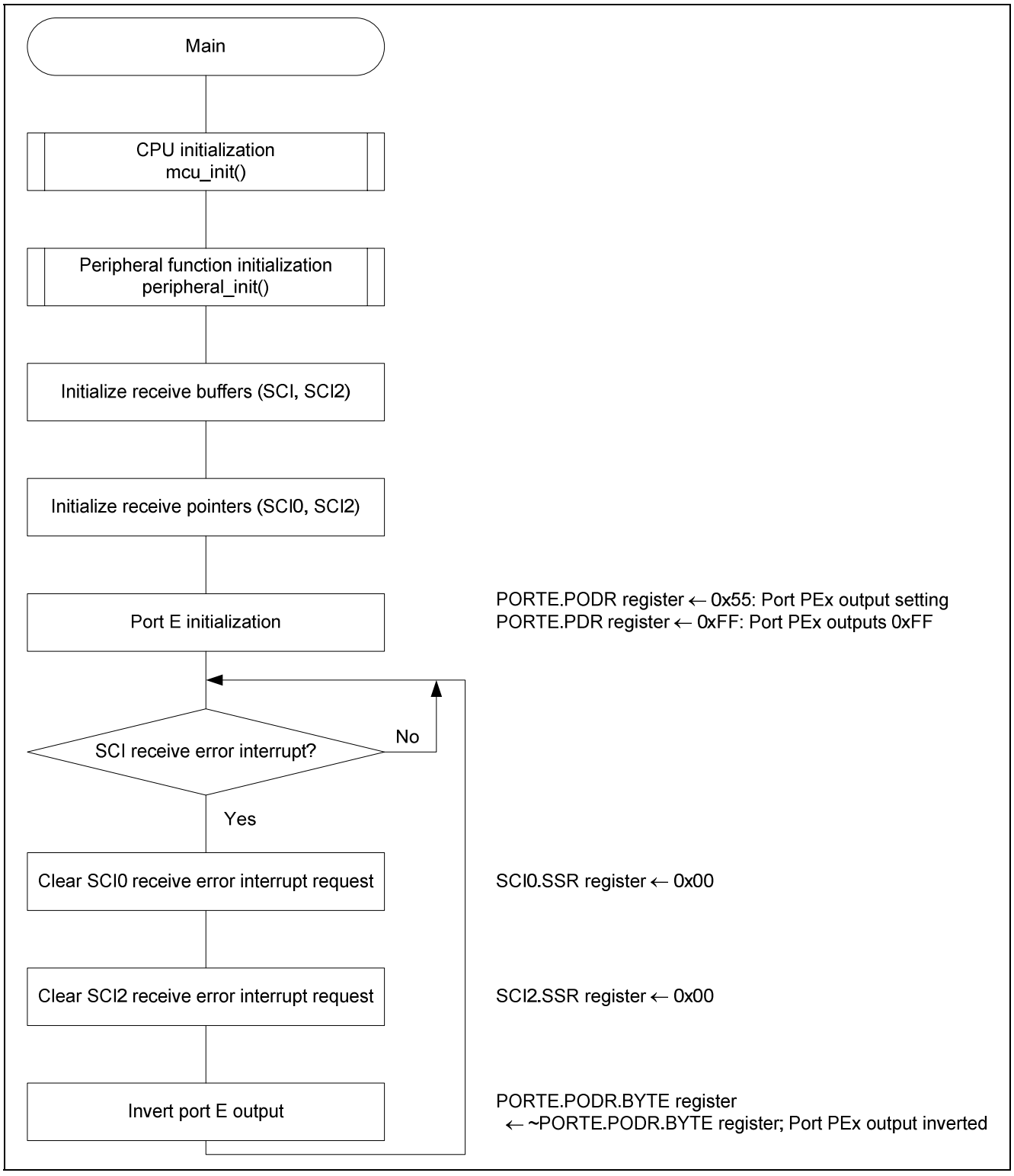

Figure 3.2 Main Processing

3.9.2 CPU Initialization

Figure 3.3 shows the flowchart for CPU initialization.

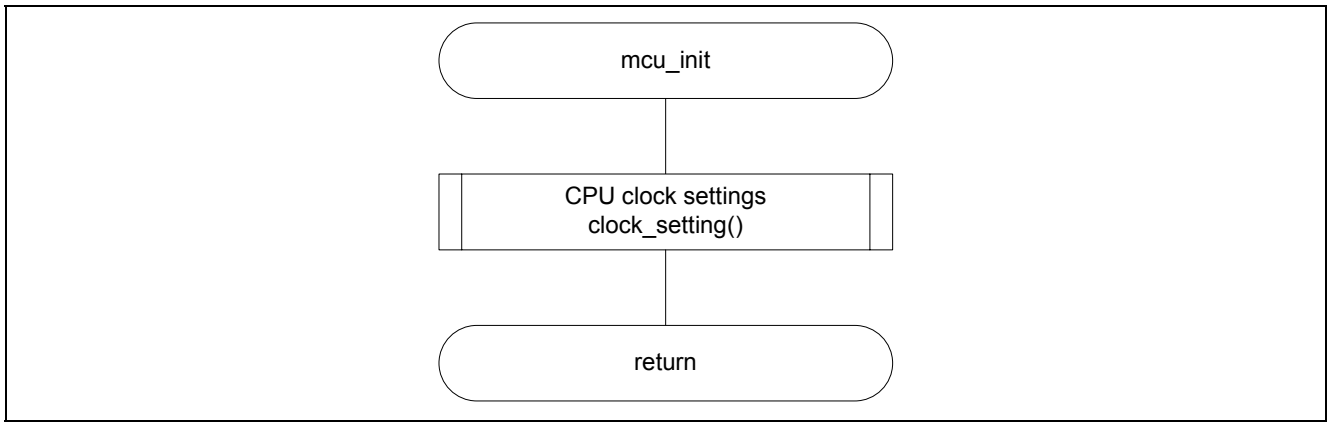

Figure 3.3 CPU Initialization

3.9.3 CPU Clock Settings

Figure 3.4 shows the flowchart for the CPU clock settings.

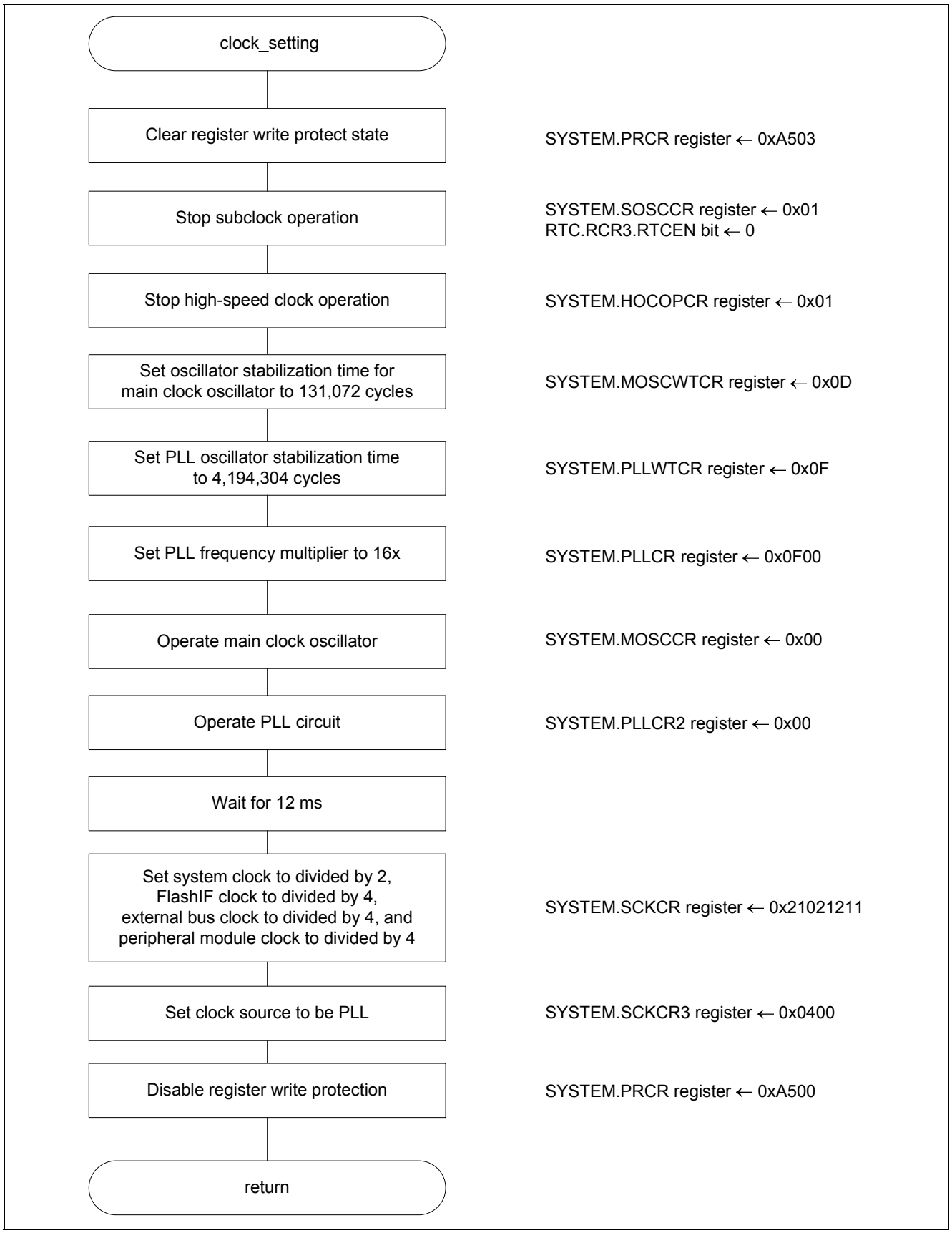

Figure 3.4 CPU Clock Settings

3.9.4 Peripheral Function Initialization

Figure 3.5 shows the flowchart for the peripheral function initialization.

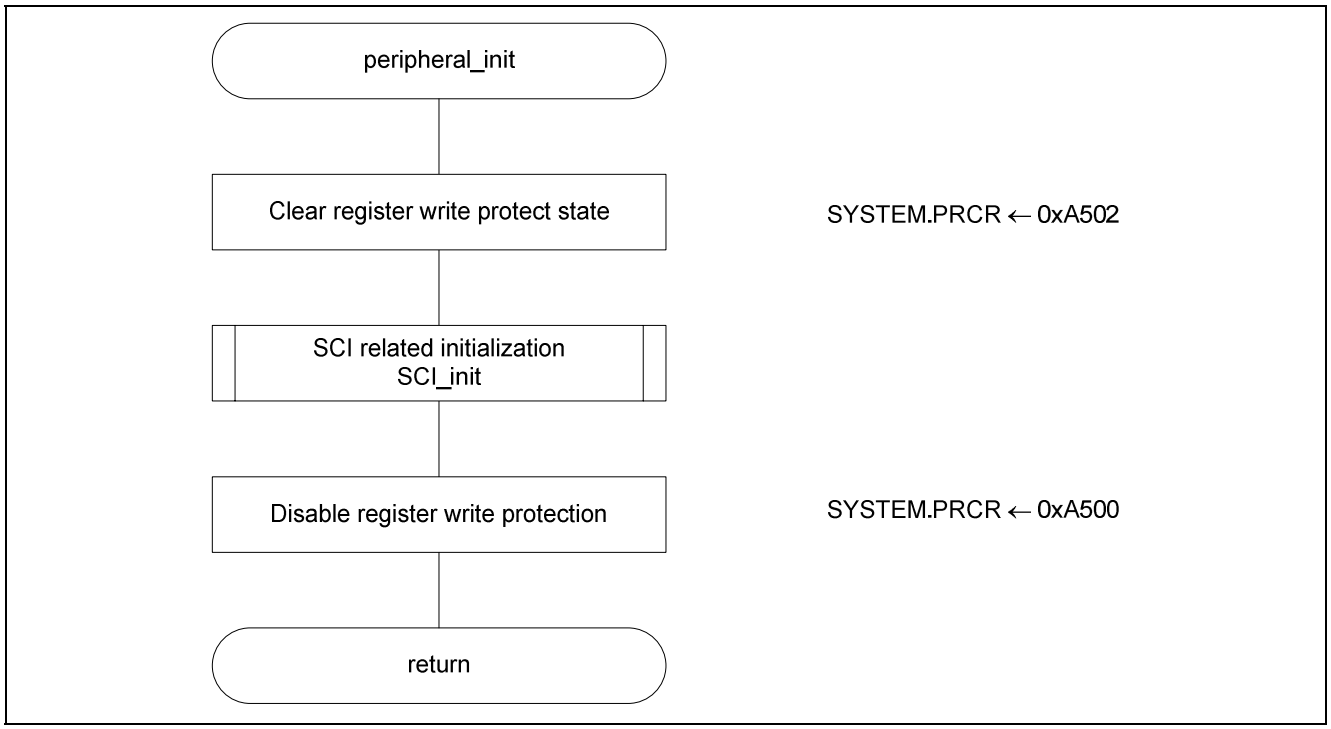

Figure 3.5 Peripheral Function Initialization

3.9.5 Serial Communications Interface (SCI) Related Initialization

Figures 3.6 and 3.7 show the flowcharts for serial communications interface (SCI) related initialization.

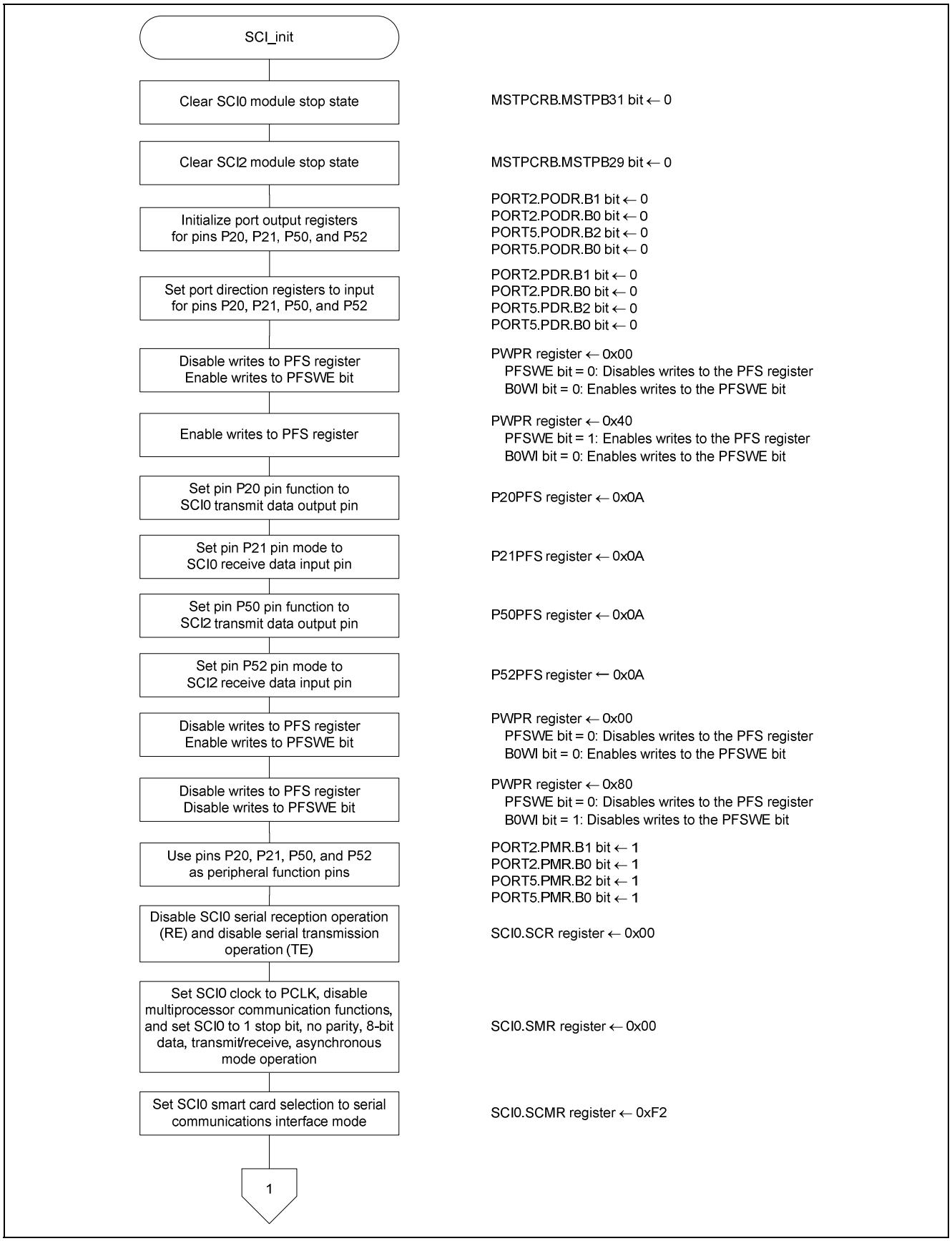

Figure 3.6 Peripheral Function Initialization (1)

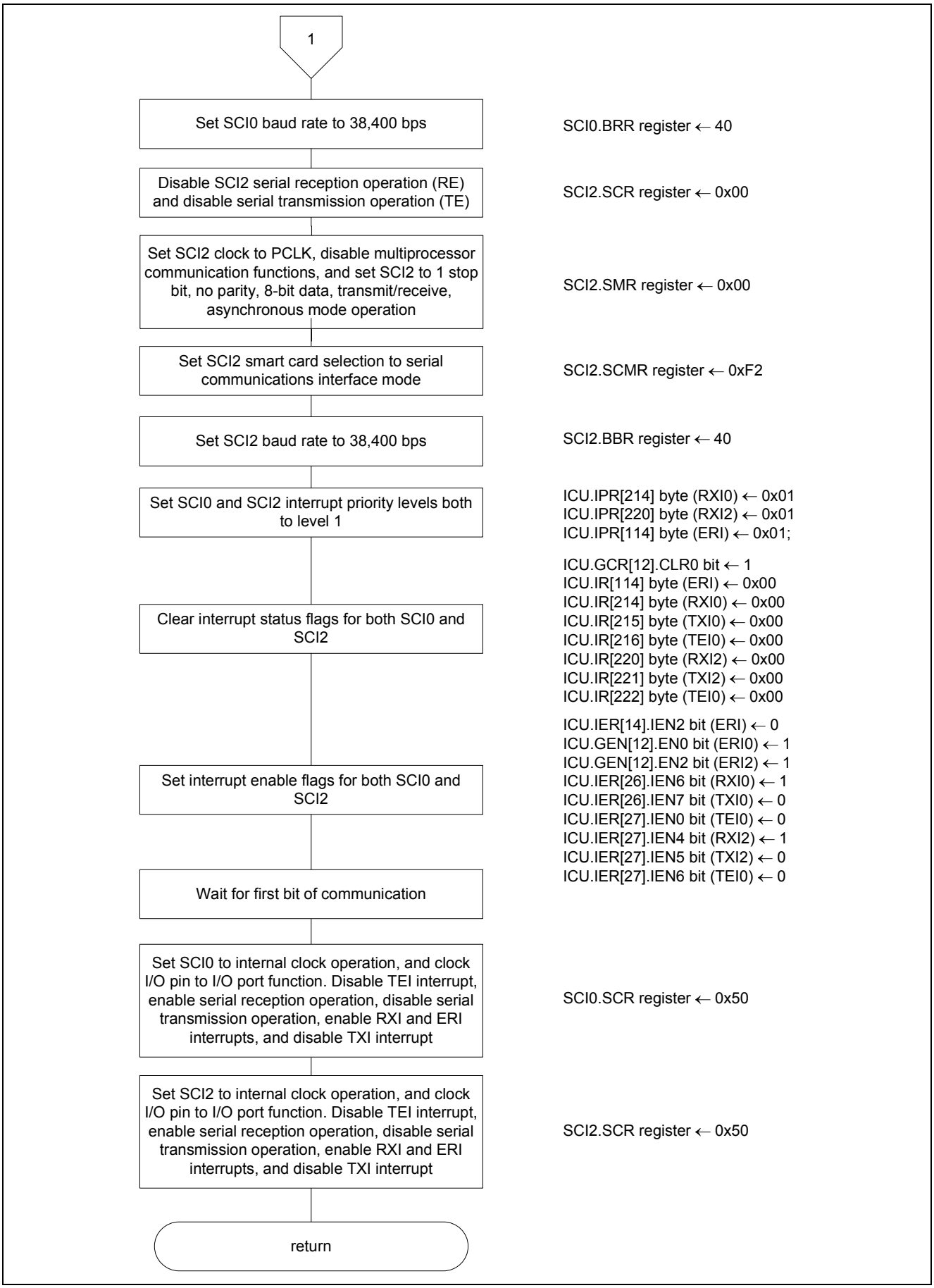

Figure 3.7 Peripheral Function Initialization (2)

3.9.6 Serial Communications Interface (SCI0) Reception Processing

Figure 3.8 shows the flowchart for serial communications interface (SCI0) reception processing.

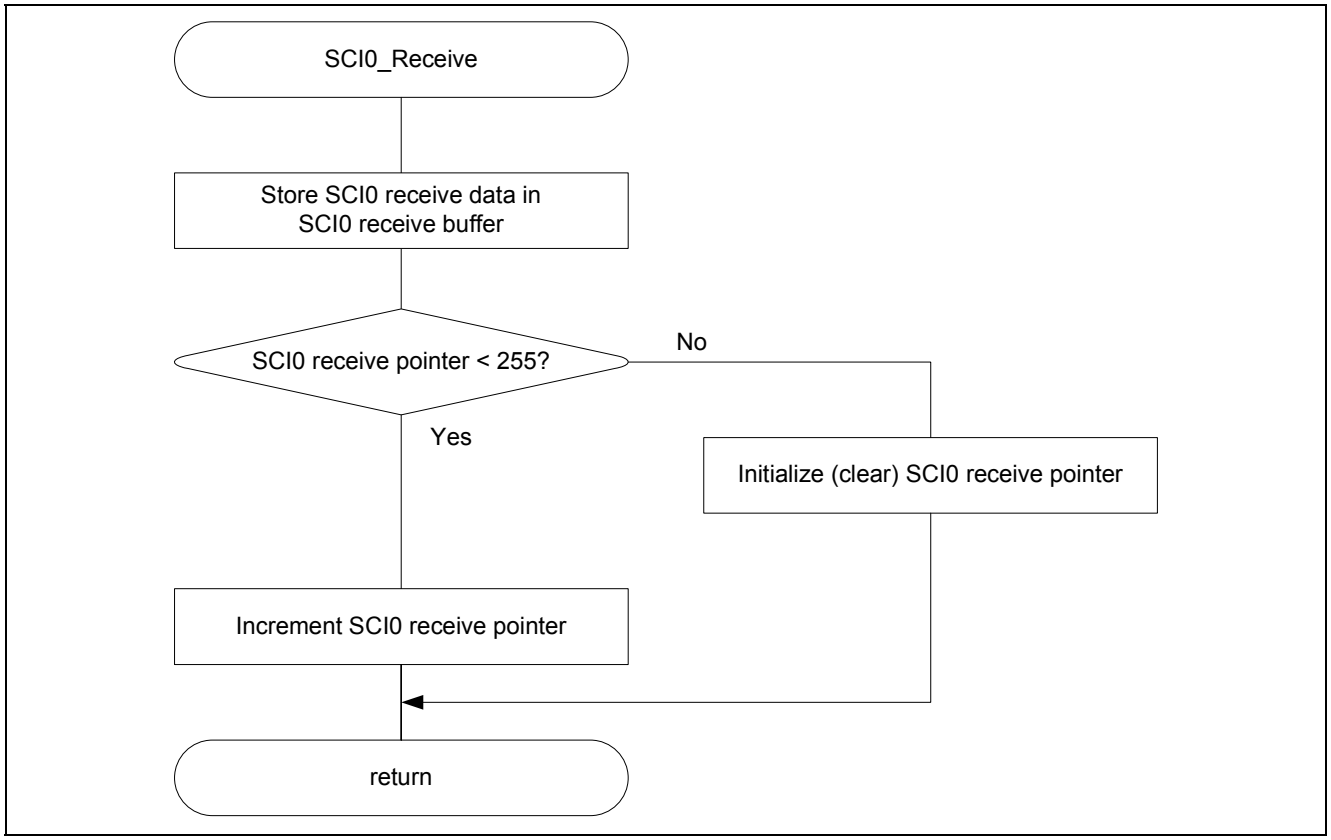

Figure 3.8 Serial Communications Interface (SCI0) Reception Processing

3.9.7 Serial Communications Interface (SCI2) Reception Processing

Figure 3.9 shows the flowchart for serial communications interface (SCI2) reception processing.

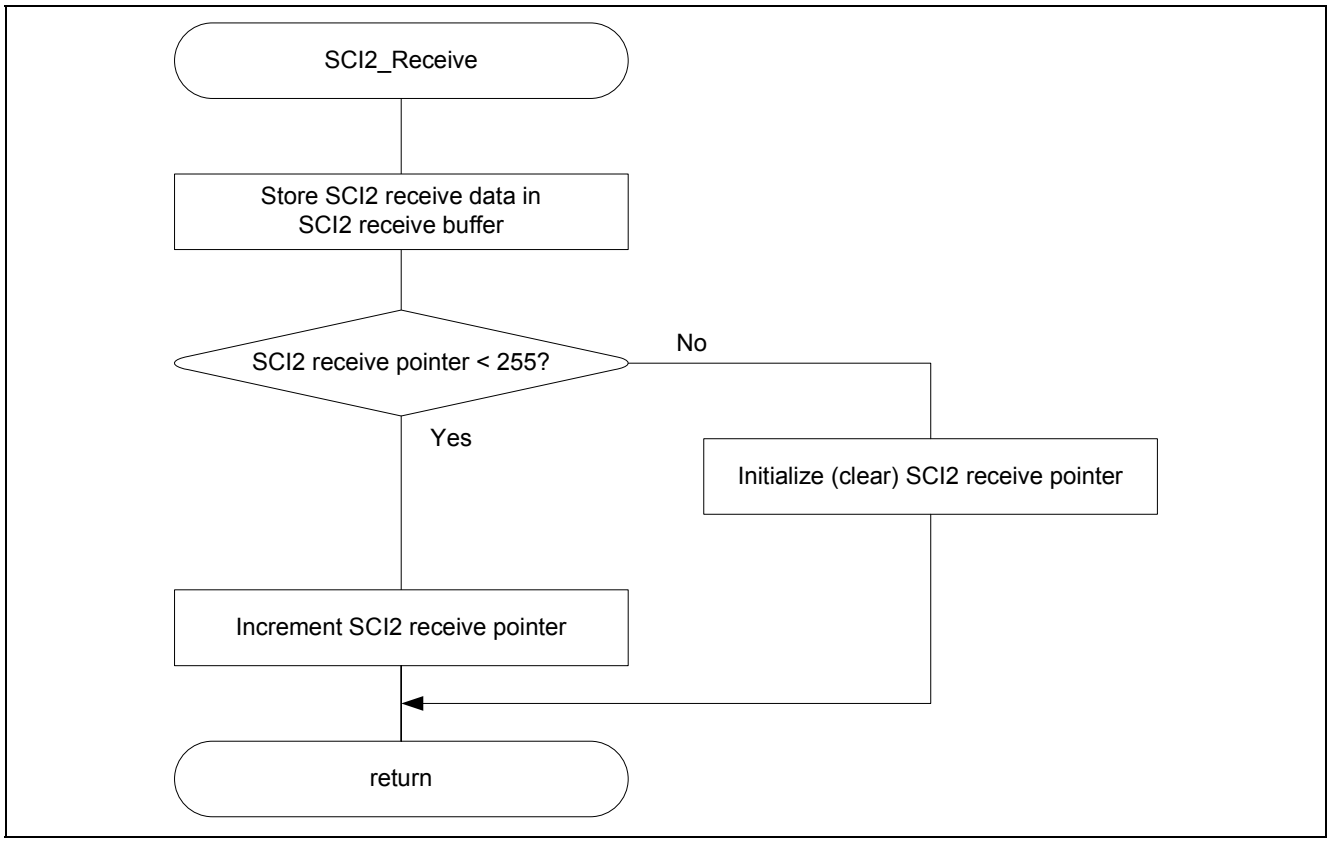

Figure 3.9 Serial Communications Interface (SCI2) Reception Processing

3.9.8 Serial Communications Interface (SCI0) Receive Interrupt Handling

Figure 3.10 shows the flowchart for serial communications interface (SCI0) receive interrupt handling.

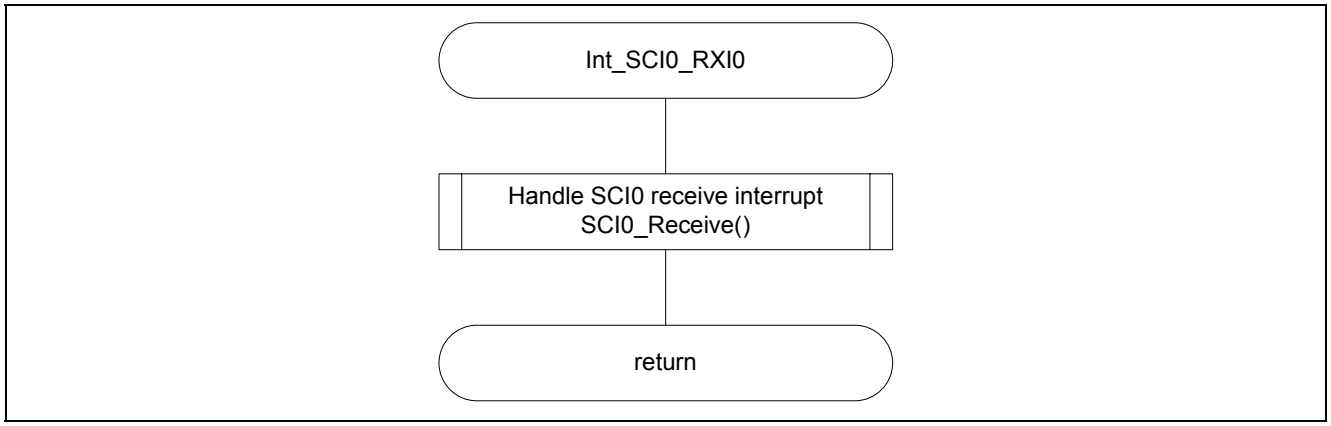

Figure 3.10 Serial Communications Interface (SCI0) Receive Interrupt Handling

3.9.9 Serial Communications Interface (SCI2) Receive Interrupt Handling

Figure 3.11 shows the flowchart for serial communications interface (SCI2) receive interrupt handling.

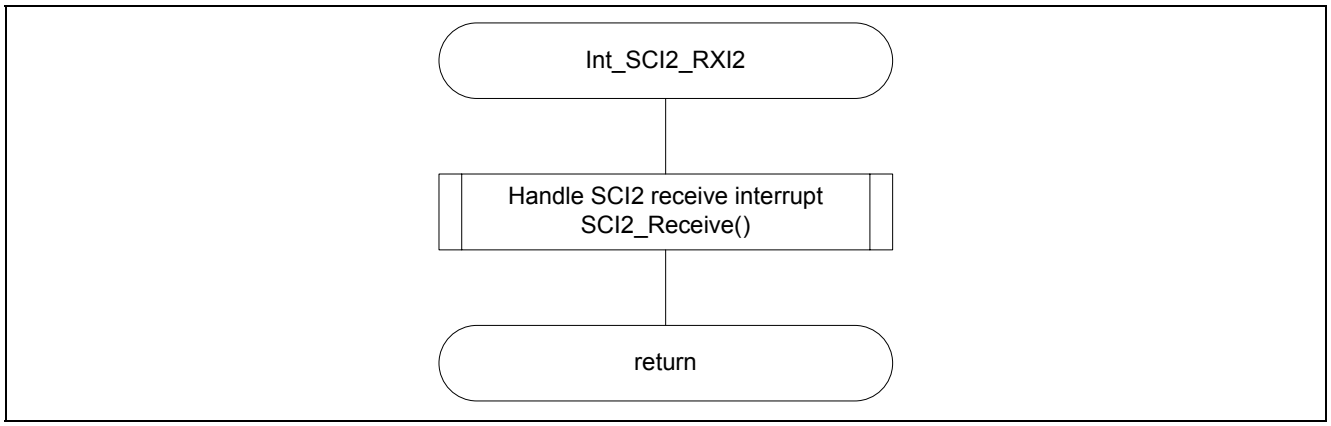

Figure 3.11 Serial Communications Interface (SCI2) Receive Interrupt Handling

4. Sample Programs

The sample program can be downloaded from the Renesas Electronics Web site.

5. Reference Documents

- RX630 Group User's Manual: Hardware, Rev.1.00
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Updates/Technical News
  (The latest information can be downloaded from the Renesas Electronics Web site.)
- C Compiler Manual
  RX Family C/C++ Compiler Package User's Manual V.1.0.1.0
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.13.11	—	First edition issued

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1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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