

RX630 Group

Initial Setting

R01AN1004EJ0100

Rev. 1.00

Apr. 5, 2013

Abstract

This document describes settings required after a reset such as clock settings or stop processing for active peripheral functions after a reset.

Products

- RX630 Group 177-pin and 176-pin packages with a ROM size between 768 KB and 2 MB
- RX630 Group 145-pin and 144-pin packages with a ROM size between 768 KB and 2 MB
- RX630 Group 100-pin package with a ROM size between 384 KB and 2 MB
- RX630 Group 80-pin package with a ROM size between 384 KB and 512 KB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications	4
1.1 Stopping Peripheral Functions Operating after a Reset	4
1.2 Configuring Nonexistent Ports	4
1.3 Setting Clocks	5
1.3.1 Overview	5
1.3.2 Clock Specifications Used in the Sample Code	5
2. Operation Confirmation Conditions	6
3. Software	7
3.1 Stop Processing for Active Peripheral Functions after a Reset	7
3.2 Nonexistent Port Initialization	8
3.2.1 Overview	8
3.2.2 Selecting the Number of Pins	8
3.3 Clock Settings	9
3.3.1 Clock Setting Procedure	9
3.3.2 Sub-Clock Setting Patterns	10
3.3.3 Oscillation Stabilization Wait Time for Each Clock	11
3.3.3.1 Main Clock Oscillation Stabilization Wait Time	11
3.3.3.2 PLL Clock Oscillation Stabilization Wait Time	12
3.3.3.3 Sub-Clock Oscillation Stabilization Wait Time	13
3.4 File Composition	14
3.5 Option-Setting Memory	14
3.6 Constants	14
3.7 Functions	18
3.8 Function Specifications	19
3.9 Flowcharts	24
3.9.1 Main Processing	24
3.9.2 Stop Processing for Active Peripheral Functions after a Reset	24
3.9.3 Nonexistent Port Initialization	25
3.9.4 Clock Initialization	26
3.9.5 Main Clock Oscillation Setting	27
3.9.6 PLL Clock Oscillation Setting	27
3.9.7 HOCO Clock Oscillation Setting	27
3.9.8 Sub-Clock Setting	28
3.9.9 Wait Processing	33
4. Appendices	34
4.1 Clock Oscillation Stabilization Wait Time	34
4.1.1 Operating PLL before Main Clock Oscillation Stabilizes	34
4.1.2 Using the Product with the Sub-Clock Oscillation Stabilization Wait Offset Time (tSUBOSCWT0)	35
4.1.2.1 When the Sub-Clock Oscillator Start-Up Time (tSUBOSC) is Less than tSUBOSCWT0	35
4.1.2.2 When the Sub-Clock Oscillator Start-Up Time (tSUBOSC) is Greater than the Sub-Clock Oscillation Stabilization Wait Offset Time (tSUBOSCWT0)	36

5. Sample Code 37

6. Reference Documents 37

1. Specifications

In the sample code, peripheral functions operating after a reset are stopped, and nonexistent port and clock settings are configured. The application note assumes processing at power-on (cold start).

1.1 Stopping Peripheral Functions Operating after a Reset

Some peripheral functions operate at power-on, and the module-stop function is disabled for some. These include the DMAC, DTC, RAM0, and RAM1. Although the sample code includes processing for stopping these peripheral functions, it is not executed in the sample code. Change the oscillation parameters as required to execute processing. Also the RTC needs to be stopped when it is not used. The setting to stop the RTC is performed in the clock setting part of the sample code.

1.2 Configuring Nonexistent Ports

Ports which are not connected to pins must be set as output for products with less than 176 pins. In the sample code, initial values are set for 100-pin products. Change the value according to the product used.

1.3 Setting Clocks

1.3.1 Overview

The clock setting procedure is as follows:

1. Main clock setting
2. Sub-clock setting
3. PLL clock setting
4. System clock switching

Processing of the sub-clock setting differs depending on sub-clock usage including processing when the sub-clock is not used. Five setting patterns are introduced in the application note (see section 3.3.2. for more information).

In the sample code, the PLL clock is used as the system clock without using the sub-clock.

1.3.2 Clock Specifications Used in the Sample Code

Table 1.1 lists the Clock Specifications Used in the Sample Code. Values such as the oscillation stabilization wait time are calculated using values listed on Table 1.1.

Table 1.2 lists the Peripheral Function and Its Application.

Table 1.1 Clock Specifications Used in the Sample Code

Clock	Oscillation Frequency	Oscillation Start-Up Time	Remarks
Crystal/ceramic resonator for the main clock	12 MHz	4.2 ms ⁽²⁾	
Crystal for the sub-clock	32.768 kHz ⁽¹⁾	1.3 sec. ⁽²⁾	For standard clock loads
PLL clock	192 MHz (main clock divided by 1 and multiplied by 16)	Maximum of 500 μ s ⁽³⁾	

Notes:

1. Sub-clock oscillation is disabled in the sample code.
2. The start-up time of a crystal/ceramic resonator differs depending on the wiring pattern, conditions of oscillation parameters, and other settings in the user system. Ask the crystal/ceramic resonator manufacturer to evaluate the user system and provide an appropriate start-up time.
3. Refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Table 1.2 Peripheral Function and Its Application

Peripheral Function	Application
Compare match timer, channel 0 (CMT0)	Measuring the clock oscillation stabilization wait time ⁽¹⁾

Note:

1. When using OS, select a channel for a timer that is not being used by OS.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F5630EDDFP (RX630 Group)
Operating frequencies	<ul style="list-style-type: none"> - Main clock: 12 MHz - Sub-clock: 32.768 kHz (stopped in setting patterns A and B) - PLL: 192 MHz (main clock divided by 1 and multiplied by 16) - HOCO: Stopped - System clock (ICLK): 96 MHz (PLL divided by 2) - Peripheral module clock B (PCLKB): 48 MHz (PLL divided by 4) - External bus clock (BCLK): 48 MHz (PLL divided by 4) - FlashIF clock (FCLK): 48 MHz (PLL divided by 4) - IEBUS clock (IECLK): 48 MHz (PLL divided by 4)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09.01
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V.1.02 Release 01 Compile options -cpu=rx600 -output=obj="\$\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -nologo (The default setting is used in the integrated development environment.)
iodefine.h version	Version 1.50
Endian	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for RX630 (product part no.: R0K505630C000BE)

3. Software

In the sample code, peripheral functions operating after a reset are stopped, nonexistent ports are configured, and then clock settings are configured.

3.1 Stop Processing for Active Peripheral Functions after a Reset

Peripheral functions that are operating after a reset are stopped in this processing.

The module-stop state is canceled after a reset only for modules listed in the Table 3.1. To enter the module-stop state, set the module stop bit to 1 (transition to the module-stop state is made). Power consumption can be reduced by entering the module-stop state.

In the sample code, set the MSTP_STATE_“target module” constant to 0 (MODULE_STOP_DISABLE), so the target module does not enter the module-stop state. When the system requires a module to enter the module-stop state, set the constant in r_init_stop_module.h to 1 (MODULE_STOP_ENABLE).

Table 3.1 lists the Peripheral Modules whose Module-Stop States are Canceled after a Reset.

Table 3.1 Peripheral Modules whose Module-Stop States are Canceled after a Reset

Peripheral Module	Module Stop Bit	Value after a Reset	Value when not Using the Module
DMAC/DTC	MSTPCRA.MSTPA28 bit	0 (module-stop state is canceled)	1 (transition to the module-stop state is made)
RAM0	MSTPCRC.MSTPC0 bit		
RAM1	MSTPCRC.MSTPC1 bit		

3.2 Nonexistent Port Initialization

3.2.1 Overview

When using a product with less than 176 pins, set the corresponding bits of nonexistent ports in the PDR register to 1 (output). After the nonexistent port initialization function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the I/O select bits in the PDR registers to 1 and set the output data store bits in the PODR registers to 0.

Table 3.2 lists Nonexistent Ports.

Table 3.2 Nonexistent Ports

Port Symbol	144-Pin and 145-Pin Packages	No. of Pins	100-Pin Package	No. of Pins	80-Pin Package	No. of Pins
PORT0	—	—	P00 to P03	4	P00 to P03	4
PORT1	P10 and P11	2	P10 and P11	2	P10 and P11	2
PORT2	—	—	—	—	P22 to P25	4
PORT3	—	—	—	—	P33	1
PORT4	—	—	—	—	—	—
PORT5	P57	1	P56 and P57	2	P50 to P53, P56, and P57	6
PORT6	—	—	P60 to P67	8	P60 to P67	8
PORT7	—	—	P70 to P77	8	P70 to P77	8
PORT8	P84 and P85	2	P80 to P87	8	P80 to P87	8
PORT9	P94 to P97	4	P90 to P97	8	P90 to P97	8
PORTA	—	—	—	—	PA7	1
PORTB	—	—	—	—	—	—
PORTC	—	—	—	—	PC0 and PC1	2
PORTD	—	—	—	—	PD3 to PD7	5
PORTE	—	—	—	—	PE6 and PE7	2
PORTF	PF0 to PF4	5	PF0 to PF5	6	PF0 to PF5	6
PORTG	PG0 to PG7	8	PG0 to PG7	8	PG0 to PG7	8
PORTH	PH4 and PH5	2	PH4 and PH5	2	PH4 and PH5	2
PORTJ	—	—	PJ5	1	PJ3 and PJ5	2
PORTK	PK0, PK1, PK6, and PK7	4	PK0 to PK7	8	PK0 to PK7	8
PORTL	PL2 to PL4	3	PL0 to PL4	5	PL0 to PL4	5

3.2.2 Selecting the Number of Pins

The number of pins in the sample code is set for the 100-pin package (PIN_SIZE=100). This application note covers 177-pin, 176-pin, 145-pin, 144-pin, 100-pin, and 80-pin packages. When using products with other than 100 pins, change PIN_SIZE in r_init_non_existent_port.h to the number of pins on the package.

3.3 Clock Settings

3.3.1 Clock Setting Procedure

Table 3.3 lists the Clock Setting with each processing and setting in the sample code.

In procedure 2. Sub-clock and RTC configuration, select a pattern from Table 3.4 according to the user system.

Steps 1 to 6 are all performed in the sample code. In processing, operate the main clock, PLL, and HOCO. Set the main clock as the RTC count source, switch the system clock to HOCO, and stop the sub-clock in the sub-clock setting (pattern A). Then switch the system clock to PLL and stop HOCO.

Table 3.3 Clock Setting Procedure

Step	Processing	Details	Setting in the Sample Code
1	Main clock oscillation setting	Set the MOSCWTCR register with a wait time until the main clock output is provided to the internal clock, and enable main clock oscillation. Then wait for the main clock oscillation stabilization wait time ⁽¹⁾ by software.	Main clock oscillator: Operating
2	Sub-clock and RTC configuration	Select the sub-clock setting pattern from five patterns listed in Table 3.4 according to the user system and configure the settings accordingly. - Patterns A and B Operate HOCO, set the RTC count source, switch the system clock to HOCO, and then configure the sub-clock and RTC. - Patterns C, D and E Set the RTC count source, and configure the sub-clock and RTC.	Sub-clock oscillator: Stopped (pattern A)
3	PLL oscillation setting ⁽²⁾	Set the PLL input frequency division ratio and frequency multiplication factor, set the PLLWTCR register with a wait time until the PLL clock output is provided to the internal clock, and enable PLL clock oscillation. Then wait for the PLL clock oscillation stabilization wait time ⁽¹⁾ by software.	PLL: Operating
4	Clock division ratio setting ⁽³⁾	Set the clock division ratio.	- ICLK: Divided by 2 - PCLKB, BCLK, FCLK.IECLK: Divided by 4 - BCLK: Stopped - UCLK: Not used
5	Switching the system clock	Switch the system clock according to the user system.	Clock switched to: PLL
6	HOCO setting	Set HOCO to be operating or stopped. When not using the HOCO clock, power consumption can be reduced by turning off the HOCO power supply.	- HOCO: Stopped - HOCO power supply: OFF

Notes:

1. Refer to 3.3.3 Oscillation Stabilization Wait Time for Each Clock for details on the oscillation stabilization wait time.
2. When not using PLL, the PLL clock setting is not necessary.
3. Do not set divide-by-1 and divide-by-2 when selecting the main clock as the system clock.

3.3.2 Sub-Clock Setting Patterns

The following five patterns are provided for step 2 in Table 3.3. The sample code uses pattern A. Change the SELECT_SUB constant in r_init_clock.h according to the user system.

- A. Neither the sub-clock nor the RTC is used.
- B. The sub-clock is not used and the RTC uses the main clock as the count source.
- C. The sub-clock is used as the system clock, and the RTC is not used.
- D. The sub-clock is used as the RTC count source.
- E. The sub-clock is used as both the system clock and RTC count source.

Table 3.4 lists the Sub-Clock Setting Patterns. Select a pattern from patterns A to E according to the user system.

Table 3.4 Sub-Clock Setting Patterns

Pattern	Sub-Clock		RTC		PCLKB ⁽¹⁾ when Setting the Sub-Clock
	Crystal Usage	System Clock	Usage	Count Source	
A	Not used	—	Not used	Main clock	HOCO divided by 1
B	Not used	—	Used	Main clock	HOCO divided by 1
C	Used	Used	Not used	Sub-clock	LOCO divided by 1
D	Used	Not used	Used	Sub-clock	LOCO divided by 1
E	Used	Used	Used	Sub-clock	LOCO divided by 1

Note:

- The set value for PCLKB must satisfy the following:
 $PCLKB \geq \text{RTC count source}$.

3.3.3 Oscillation Stabilization Wait Time for Each Clock

This section describes the wait control registers and oscillation stabilization wait times for the main clock, PLL and sub-clock. Values for the oscillation stabilization wait times are specified in the sample code.

3.3.3.1 Main Clock Oscillation Stabilization Wait Time

Figure 3.1 shows the Main Clock Oscillation Stabilization Wait Time and Table 3.5 lists the Setting Value for the MOSCWTCR Register and Oscillation Stabilization Wait Time.

Set the main clock oscillator wait control register (MOSCWTCR) to a value greater than or equal to the main clock oscillator start-up time ($t_{MAINOSC}$) recommended by the crystal/ceramic resonator manufacturer. Set the main clock oscillation stabilization wait time ($t_{MAINOSCWT}$) to a value greater than ' $t_{MAINOSC}$ recommended by the crystal/ceramic resonator manufacturer + (wait time set in the MOSCWTCR register + 16384 cycles)'.

$t_{MAINOSC}$ used in the sample code is 4.2 ms, thus the setting value in the MOSCWTCR register is 0Ch (approximately 5.46 ms), and the setting value for $t_{MAINOSCWT}$ is approximately 11.026 ms.

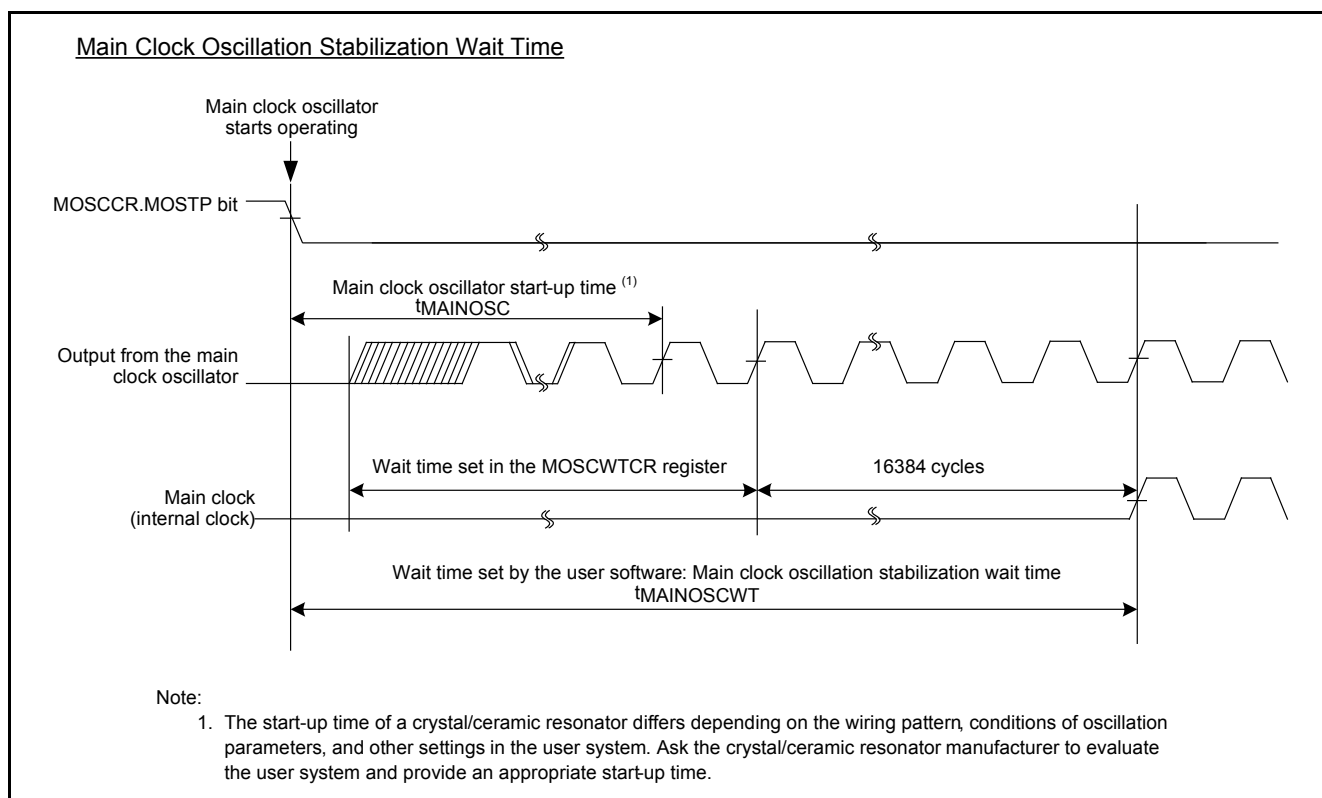


Figure 3.1 Main Clock Oscillation Stabilization Wait Time

Table 3.5 Setting Value for the MOSCWTCR Register and Oscillation Stabilization Wait Time

Setting Item	Condition of Setting Value and Calculation Method	Setting Value in the Sample Code
MOSCWTCR.MSTS[4:0] bits	Value greater than or equal to $t_{MAINOSC}$ recommended by the crystal/ceramic resonator manufacturer	0Ch (approx. 5.46 ms)
Oscillation stabilization wait time ($t_{MAINOSCWT}$)	When n is the wait time selected by the MOSCWTCR.MSTS[4:0] bits: $t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$	Approx. 11.026 ms

3.3.3.2 PLL Clock Oscillation Stabilization Wait Time

(When enabling PLL oscillation after the main clock oscillation stabilization wait time elapses)

Figure 3.2 shows the PLL Clock Oscillation Stabilization Wait Time and Table 3.6 lists the Setting Value of the PLLWTCR Register and Oscillation Stabilization Wait Time.

Set a value greater than or equal to PLL lock time (t_{PLL1} (max. 500 μ s)) to the PLL wait control register (PLLWTCR). Set the PLL clock oscillation stabilization wait time (t_{PLLWT1}) to a value greater than ' t_{PLL1} (500 μ s) + (wait time set in the PLLWTCR register + 131072 cycles)'.

t_{PLL1} is a maximum of 500 μ s, thus the setting value in the PLLWTCR register is 0Ah (approximately 681.6 μ s), and the setting value for the t_{PLLWT1} is approximately 1.865 ms.

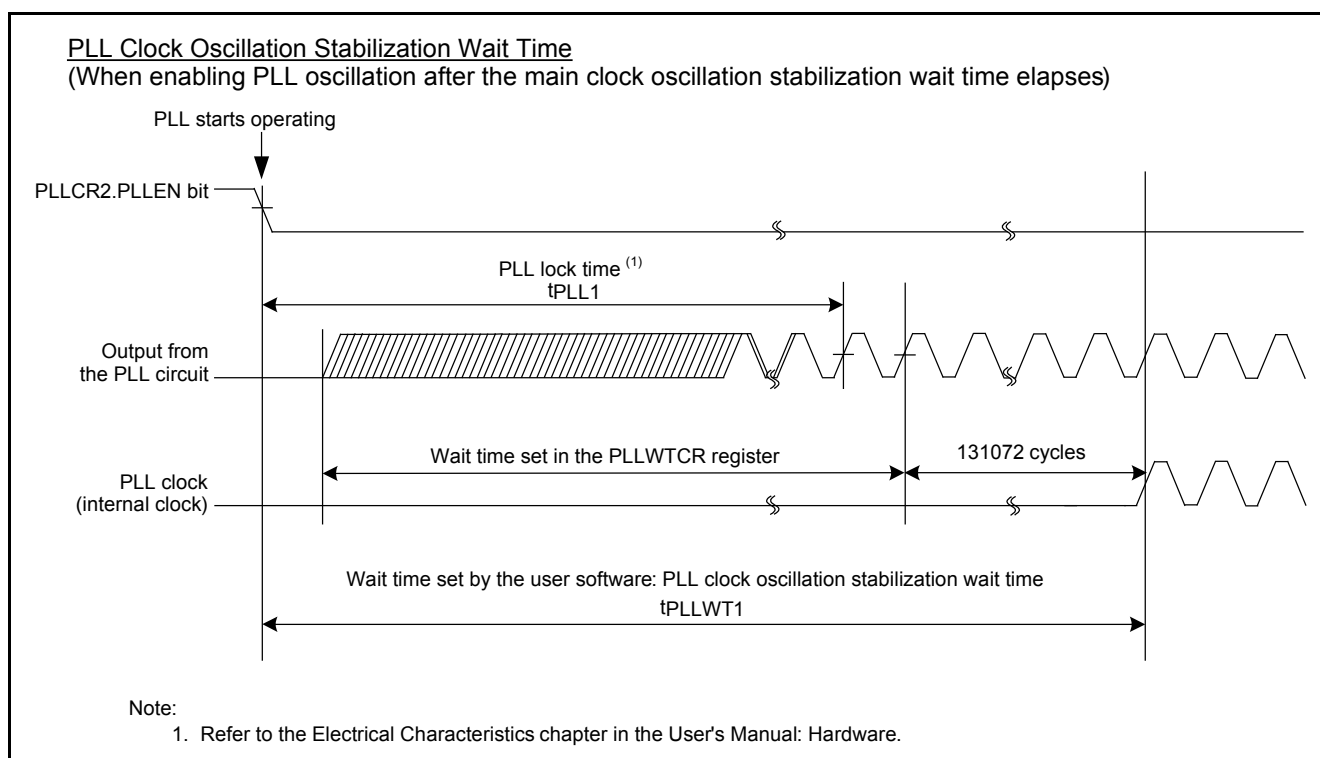


Figure 3.2 PLL Clock Oscillation Stabilization Wait Time

Table 3.6 Setting Value of the PLLWTCR Register and Oscillation Stabilization Wait Time

Setting Item	Condition of Setting Value and Calculation Method	Setting Value in the Sample Code
PLLWTCR.PSTS[4:0] bits	Value greater than or equal to t_{PLL1} (max. 500 μ s)	0Ah (approx. 681.6 μ s)
Oscillation stabilization wait time (t_{PLLWT1})	When n is the wait time selected by the PLLWTCR.PSTS[4:0] bits: $t_{PLL1} + \frac{n + 131072}{f_{PLL}}$	Approx. 1.865 ms

3.3.3.3 Sub-Clock Oscillation Stabilization Wait Time

Some RX630 Group products do not have the sub-clock oscillation wait offset time (tSUBOSCWT0). Refer to the List of Products tables in the Overview chapter in the User's Manual: Hardware. The sample code sets the oscillation stabilization wait time (tSUBOSCWT) for products without tSUBOSCWT0. Refer to 4.1.2 for details of tSUBOSCWT for products with tSUBOSCWT0.

Figure 3.3 shows the Sub-Clock Oscillation Stabilization Wait Time (For Products without tSUBOSCWT0) and Table 3.7 lists the Setting Value of the SOSCWTCCR Register and Oscillation Stabilization Wait Time (For Products without tSUBOSCWT0).

Set the sub-clock oscillator wait control register (SOSCWTCCR) to a value greater than or equal to the sub-clock oscillator start-up time (tSUBOSC) recommended by the crystal/ceramic resonator manufacturer. Set tSUBOSCWT to a value greater than tSUBOSC recommended by the crystal/ceramic resonator manufacturer plus the wait time set in the SOSCWTCCR register.

tSUBOSC used in the sample code is 1.3 seconds, thus the setting value in the SOSCWTCCR register is 0Ch (approximately 2 seconds), and the setting value for tSUBOSCWT is approximately 3.3 seconds.

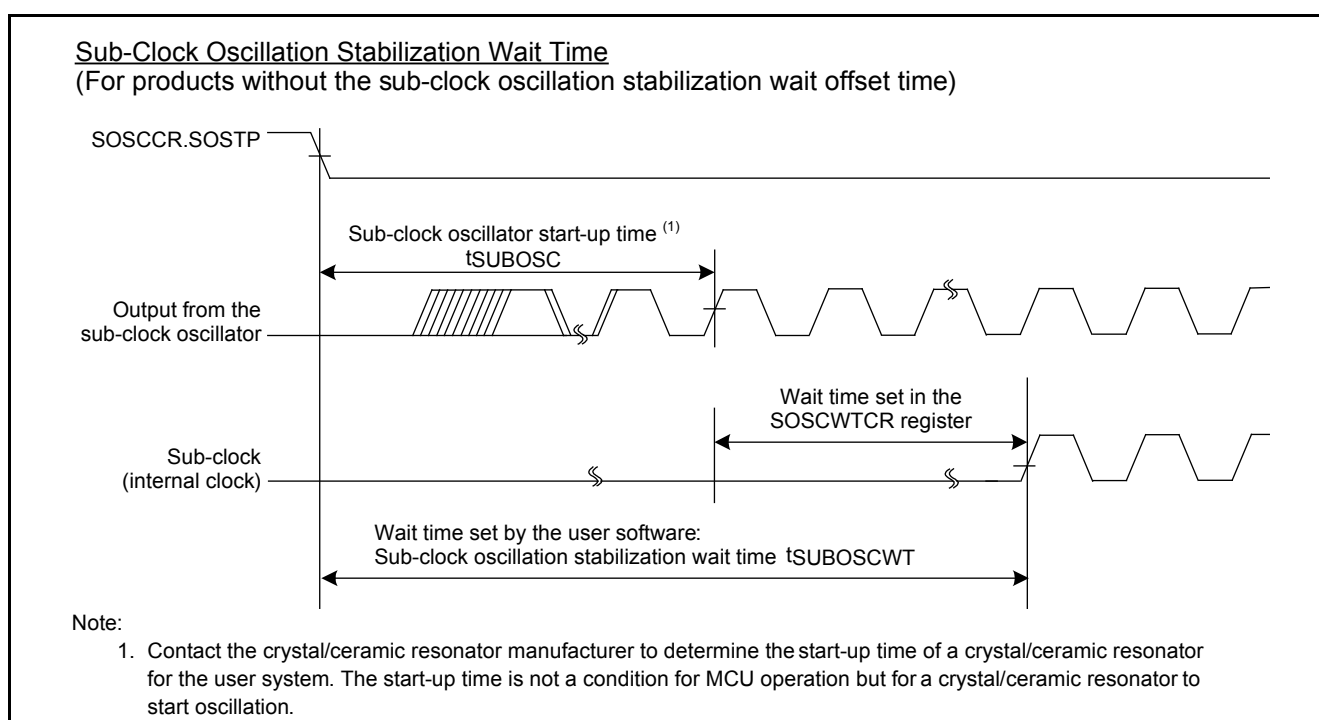


Figure 3.3 Sub-Clock Oscillation Stabilization Wait Time (For Products without tSUBOSCWT0)

Table 3.7 Setting Value of the SOSCWTCCR Register and Oscillation Stabilization Wait Time (For Products without tSUBOSCWT0)

Setting Item	Condition of Setting Value and Calculation Method	Setting Value in the Sample Code
SOSCWTCCR.SSTS[4:0] bits	Value greater than or equal to tSUBOSC recommended by the crystal/ceramic resonator manufacturer	0Ch (approx. 2 sec.)
Oscillation stabilization wait time (tSUBOSCWT)	When n is the wait time selected by the SOSCWTCCR.SSTS[4:0] bits: $tSUBOSC \text{ recommended by the crystal/ceramic resonator manufacturer (1.3 sec.)} + \frac{n}{f_{SUB}}$	Approx. 3.3 sec.

3.4 File Composition

Table 3.8 lists the Files Used in the Sample Code. Files generated by the integrated development environment are not included in this table.

Table 3.8 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing	
r_init_stop_module.c	Stop processing for active peripheral functions after a reset	
r_init_stop_module.h	Header file for r_init_stop_module.c	
r_init_non_existent_port.c	Nonexistent port initialization	
r_init_non_existent_port.h	Header file for r_init_non_existent_port.c	
r_init_clock.c	Clock initialization	
r_init_clock.h	Header file for r_init_clock.c	

3.5 Option-Setting Memory

Table 3.9 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 3.9 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FFFF FF8Fh to FFFF FF8Ch	FFFF FFFFh	The IWDT is stopped after a reset. The WDT is stopped after a reset.
OFS1	FFFF FF8Bh to FFFF FF88h	FFFF FFFFh	The voltage monitor 0 reset is disabled after a reset. HOCO oscillation is disabled after a reset.
MDES	FFFF FF83h to FFFF FF80h	FFFF FFFFh	Little endian

3.6 Constants

Table 3.10 lists the Constants Used in the Sample Code, Table 3.11 lists the Constants when a 177-Pin or 176-Pin Package is Used (PIN_SIZE=177 or PIN_SIZE=176), Table 3.12 lists the Constants when a 145-Pin or 144-Pin Package is Used (PIN_SIZE=145 or PIN_SIZE=144), Table 3.13 lists the Constants when a 100-Pin Package is Used (PIN_SIZE=100), and Table 3.14 lists Constants when a 80-Pin Package is Used (PIN_SIZE=80).

Table 3.10 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
MAIN_CLOCK_Hz ⁽¹⁾	12,000,000 L	Oscillation frequency of a crystal/ceramic resonator for the main clock (Hz)
SUB_CLOCK_Hz ⁽¹⁾	32,768 L	Oscillation frequency of a crystal for the sub-clock (Hz)
WAIT_TIME_FOR_MAIN_OSCILLATION ⁽¹⁾	11,026,000 L	Main clock oscillation stabilization wait time (ns)
WAIT_TIME_FOR_SUB_OSCILLATION ⁽¹⁾	3,300,000,000 L	Sub-clock oscillation stabilization wait time (ns)
WAIT_TIME_FOR_PLL_OSCILLATION ⁽¹⁾	1,865,000 L	PLL clock oscillation stabilization wait time (ns)
WAIT_TIME_FOR_HOCO_OSCILLATION	2,000,000 L	HOCO clock oscillation stabilization wait time (ns)
PATTERN_A	1	Sub-clock setting pattern A
PATTERN_B	2	Sub-clock setting pattern B
PATTERN_C	3	Sub-clock setting pattern C
PATTERN_D	4	Sub-clock setting pattern D
PATTERN_E	5	Sub-clock setting pattern E
SELECT_SUB ⁽¹⁾	PATTERN_A	Selection of the sub-clock setting pattern
MSTP_STATE_DMADCDC ⁽²⁾	MODULE_STOP_DISABLE	Cancel the module-stop state for DMAC and DTC
MSTP_STATE_RAM0 ⁽²⁾	MODULE_STOP_DISABLE	Cancel the module-stop state for RAM0
MSTP_STATE_RAM1 ⁽²⁾	MODULE_STOP_DISABLE	Cancel the module-stop state for RAM1
PIN_SIZE ⁽³⁾	100	Number of pins of the product used
MAIN_CLOCK_CYCLE	$(1/\text{MAIN_CLOCK_Hz}) \times 10^9$	Main clock cycle (ns)
SUB_CLOCK_CYCLE	$(1/\text{SUB_CLOCK_Hz}) \times 10^9$	Sub-clock cycle (ns)
FOR_CMT0_TIME (when the RTC count source is the sub-clock)	1/LOCO*32	Count period (ns) of the CMT0 timer for the oscillation stabilization wait time (LOCO = 143.75 kHz (max.), PCLKB divided by 32)
FOR_CMT0_TIME (when the RTC count source is the main clock)	1/HOCO*32	Count period (ns) of the CMT0 timer for the oscillation stabilization wait time (HOCO = 55 MHz (max.), PCLKB divided by 32)
FOR_CMT0_LOCO (when the RTC count source is the main clock)	1/LOCO*32	Count period (ns) of the CMT0 timer for the main clock and PLL oscillation stabilization wait times when the RTC count source is the main clock. (LOCO = 143.75 kHz (max.), PCLKB divided by 32)
MODULE_STOP_ENABLE	1	Module stop-state
MODULE_STOP_DISABLE	0	Module stop-state is canceled

Notes:

1. Change the setting value in r_init_clock.h according to the user system.
2. Change the setting value in r_init_stop_module.h according to the user system.
3. Change the setting value in r_init_non_existent_port.h according to the user system.

Table 3.11 Constants when a 177-Pin or 176-Pin Package is Used (PIN_SIZE=177 or PIN_SIZE=176)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x00	Setting value for the port P0 direction register
DEF_P1PDR	0x00	Setting value for the port P1 direction register
DEF_P2PDR	0x00	Setting value for the port P2 direction register
DEF_P3PDR	0x00	Setting value for the port P3 direction register
DEF_P4PDR	0x00	Setting value for the port P4 direction register
DEF_P5PDR	0x00	Setting value for the port P5 direction register
DEF_P6PDR	0x00	Setting value for the port P6 direction register
DEF_P7PDR	0x00	Setting value for the port P7 direction register
DEF_P8PDR	0x00	Setting value for the port P8 direction register
DEF_P9PDR	0x00	Setting value for the port P9 direction register
DEF_PAPDR	0x00	Setting value for the port PA direction register
DEF_PBPDR	0x00	Setting value for the port PB direction register
DEF_PCPDR	0x00	Setting value for the port PC direction register
DEF_PDPDR	0x00	Setting value for the port PD direction register
DEF_PEPDR	0x00	Setting value for the port PE direction register
DEF_PFPDR	0x00	Setting value for the port PF direction register
DEF_PGPDR	0x00	Setting value for the port PG direction register
DEF_PHPDR	0x00	Setting value for the port PH direction register
DEF_PJPDR	0x00	Setting value for the port PJ direction register
DEF_PKPDR	0x00	Setting value for the port PK direction register
DEF_PLPDR	0x00	Setting value for the port PL direction register

Table 3.12 Constants when a 145-Pin or 144-Pin Package is Used (PIN_SIZE=145 or PIN_SIZE=144)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x00	Setting value for the port P0 direction register
DEF_P1PDR	0x03	Setting value for the port P1 direction register
DEF_P2PDR	0x00	Setting value for the port P2 direction register
DEF_P3PDR	0x00	Setting value for the port P3 direction register
DEF_P4PDR	0x00	Setting value for the port P4 direction register
DEF_P5PDR	0x80	Setting value for the port P5 direction register
DEF_P6PDR	0x00	Setting value for the port P6 direction register
DEF_P7PDR	0x00	Setting value for the port P7 direction register
DEF_P8PDR	0x30	Setting value for the port P8 direction register
DEF_P9PDR	0xF0	Setting value for the port P9 direction register
DEF_PAPDR	0x00	Setting value for the port PA direction register
DEF_PBPDR	0x00	Setting value for the port PB direction register
DEF_PCPDR	0x00	Setting value for the port PC direction register
DEF_PDPDR	0x00	Setting value for the port PD direction register
DEF_PEPDR	0x00	Setting value for the port PE direction register
DEF_PFPDR	0x1F	Setting value for the port PF direction register
DEF_PGPDR	0xFF	Setting value for the port PG direction register
DEF_PHPDR	0x30	Setting value for the port PH direction register
DEF_PJPDR	0x00	Setting value for the port PJ direction register
DEF_PKPDR	0xC3	Setting value for the port PK direction register
DEF_PLPDR	0x1C	Setting value for the port PL direction register

Table 3.13 Constants when a 100-Pin Package is Used (PIN_SIZE=100)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x0F	Setting value for the port P0 direction register
DEF_P1PDR	0x03	Setting value for the port P1 direction register
DEF_P2PDR	0x00	Setting value for the port P2 direction register
DEF_P3PDR	0x00	Setting value for the port P3 direction register
DEF_P4PDR	0x00	Setting value for the port P4 direction register
DEF_P5PDR	0xC0	Setting value for the port P5 direction register
DEF_P6PDR	0xFF	Setting value for the port P6 direction register
DEF_P7PDR	0xFF	Setting value for the port P7 direction register
DEF_P8PDR	0xFF	Setting value for the port P8 direction register
DEF_P9PDR	0xFF	Setting value for the port P9 direction register
DEF_PAPDR	0x00	Setting value for the port PA direction register
DEF_PBPDR	0x00	Setting value for the port PB direction register
DEF_PCPDR	0x00	Setting value for the port PC direction register
DEF_PDPDR	0x00	Setting value for the port PD direction register
DEF_PEPDR	0x00	Setting value for the port PE direction register
DEF_PFPDR	0x3F	Setting value for the port PF direction register
DEF_PGPDR	0xFF	Setting value for the port PG direction register
DEF_PHPDR	0x30	Setting value for the port PH direction register
DEF_PJPDR	0x20	Setting value for the port PJ direction register
DEF_PKPDR	0xFF	Setting value for the port PK direction register
DEF_PLPDR	0x1F	Setting value for the port PL direction register

Table 3.14 Constants when a 80-Pin Package is Used (PIN_SIZE=80)

Constant Name	Setting Value	Contents
DEF_P0PDR	0x0F	Setting value for the port P0 direction register
DEF_P1PDR	0x03	Setting value for the port P1 direction register
DEF_P2PDR	0x3C	Setting value for the port P2 direction register
DEF_P3PDR	0x08	Setting value for the port P3 direction register
DEF_P4PDR	0x00	Setting value for the port P4 direction register
DEF_P5PDR	0xCF	Setting value for the port P5 direction register
DEF_P6PDR	0xFF	Setting value for the port P6 direction register
DEF_P7PDR	0xFF	Setting value for the port P7 direction register
DEF_P8PDR	0xFF	Setting value for the port P8 direction register
DEF_P9PDR	0xFF	Setting value for the port P9 direction register
DEF_PAPDR	0x80	Setting value for the port PA direction register
DEF_PBPDR	0x00	Setting value for the port PB direction register
DEF_PCPDR	0x03	Setting value for the port PC direction register
DEF_PDPDR	0xF8	Setting value for the port PD direction register
DEF_PEPDR	0xC0	Setting value for the port PE direction register
DEF_PFPDR	0x3F	Setting value for the port PF direction register
DEF_PGPDR	0xFF	Setting value for the port PG direction register
DEF_PHPDR	0x30	Setting value for the port PH direction register
DEF_PJPDR	0x28	Setting value for the port PJ direction register
DEF_PKPDR	0xFF	Setting value for the port PK direction register
DEF_PLPDR	0x1F	Setting value for the port PL direction register

3.7 Functions

Table 3.15 lists the Functions Used in the Sample Code.

Table 3.15 Functions Used in the Sample Code

Function Name	Outline
main	Main processing
R_INIT_StopModule	Stop processing for active peripheral functions after a reset
R_INIT_NonExistentPort	Nonexistent port initialization
R_INIT_Clock	Clock initialization
CGC_oscillation_main	Main clock oscillation setting
CGC_oscillation_PLL	PLL clock oscillation setting
CGC_oscillation_HOCO	HOCO clock oscillation setting
CGC_no_use_subclk	Sub-clock setting pattern A (when the sub-clock is not used as the system clock or RTC count source)
CGC_disable_subclk_RTC_use_mainclk	Sub-clock setting pattern B (when the sub-clock is not used and the RTC operates using the main clock)
CGC_subclk_as_sysclk	Sub-clock setting pattern C (when the sub-clock is used as the system clock and not used as the RTC count source)
CGC_subclk_as_RTC	Sub-clock setting pattern D (when the sub-clock is used as the RTC count source and not used as the system clock)
CGC_subclk_as_sysclk_RTC	Sub-clock setting pattern E (when the sub-clock is used as both the system clock and RTC count source)
disable_subclk	Disabling the sub-clock
oscillation_subclk	Sub-clock oscillation setting
no_use_subclk_as_sysclk	Processing when the sub-clock is not used as the system clock
resetting_wtcr_mainclk	Resetting the wait control register (RTC count source is the main clock)
resetting_wtcr_subclk	Resetting the wait control register (RTC count source is the sub-clock)
enable_RTC	Initialization when using the RTC
disable_RTC_mainclk	Initialization when not using the RTC (RTC count source is the main clock)
disable_RTC_subclk	Initialization when not using the RTC (RTC count source is the sub-clock)
cmt0_wait	Wait processing

3.8 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Call the following functions: Stop processing for active peripheral functions after a reset, nonexistent port initialization, and clock initialization.
Arguments	None
Return Value	None
R_INIT_StopModule	
Outline	Stop processing for active peripheral functions after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Configure the setting to enter the module-stop state.
Arguments	None
Return Value	None
Remarks	Transition to the module-stop state is not performed in the sample code.
R_INIT_NonExistentPort	
Outline	Nonexistent port initialization
Header	r_init_non_existent_port.h
Declaration	void R_INIT_NonExistentPort(void)
Description	Initialize port direction registers for ports that do not exist in products with less than 176 pins.
Arguments	None
Return Value	None
Remarks	The number of pins in the sample code is set for the 100-pin package (PIN_SIZE=100). After this function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the I/O select bits in the PDR registers to 1 and set the output data store bits in the PODR registers to 0.
R_INIT_Clock	
Outline	Clock initialization
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Initialize the clock.
Arguments	None
Return Value	None
Remarks	The sample code selects processing which uses PLL as the system clock without using the sub-clock.

CGC_oscillation_main	
Outline	Main clock oscillation setting
Header	r_init_clock.h
Declaration	void CGC_oscillation_main(void)
Description	Set the MOSCWTCR register, and enable main clock oscillation. Then wait for the main clock oscillation stabilization wait time by software.
Arguments	None
Return Value	None
CGC_oscillation_PLL	
Outline	PLL clock oscillation setting
Header	r_init_clock.h
Declaration	void CGC_oscillation_PLL(void)
Description	Set the PLL input frequency division ratio and frequency multiplication factor, set the PLLWTCR register, and enable PLL clock oscillation. Then wait for the PLL clock oscillation stabilization wait time by software.
Arguments	None
Return Value	None
Remarks	This processing is not necessary if PLL is not used as the system clock.
CGC_oscillation_HOCO	
Outline	HOCO clock oscillation setting
Header	r_init_clock.h
Declaration	void CGC_oscillation_HOCO(void)
Description	Oscillate HOCO and then wait for HOCO oscillation stabilization wait time by software.
Arguments	None
Return Value	None
CGC_no_use_subclk	
Outline	Sub-clock setting pattern A
Header	r_init_clock.h
Declaration	void CGC_no_use_subclk(void)
Description	Configure the setting when the sub-clock is not used as the system clock or RTC count source.
Arguments	None
Return Value	None
CGC_disable_subclk_RTC_use_mainclk	
Outline	Sub-clock setting pattern B
Header	r_init_clock.h
Declaration	void CGC_disable_subclk_RTC_use_mainclk(void)
Description	Configure the setting when the sub-clock is not used and the RTC operates using the main clock.
Arguments	None
Return Value	None

CGC_subclk_as_sysclk	
Outline	Sub-clock setting pattern C
Header	r_init_clock.h
Declaration	void CGC_subclk_as_sysclk(void)
Description	Configure the setting when the sub-clock is used as the system clock and not used as the RTC count source.
Arguments	None
Return Value	None
CGC_subclk_as_RTC	
Outline	Sub-clock setting pattern D
Header	r_init_clock.h
Declaration	void CGC_subclk_as_RTC(void)
Description	Configure the setting when the sub-clock is used as the RTC count source and not used as the system clock.
Arguments	None
Return Value	None
CGC_subclk_as_sysclk_RTC	
Outline	Sub-clock setting pattern E
Header	r_init_clock.h
Declaration	void CGC_subclk_as_sysclk_RTC(void)
Description	Configure the setting when the sub-clock is used as both the system clock and RTC count source.
Arguments	None
Return Value	None
disable_subclk	
Outline	Disabling the sub-clock
Header	None
Declaration	static void disable_subclk(void)
Description	Configure the setting when the sub-clock is not used as the system clock or RTC count source.
Arguments	None
Return Value	None
oscillation_subclk	
Outline	Sub-clock oscillation setting
Header	None
Declaration	static void oscillation_subclk(void)
Description	Configure the sub-clock oscillation.
Arguments	None
Return Value	None

<hr/> no_use_subclk_as_sysclk <hr/>	
Outline	Processing when the sub-clock is not used as the system clock
Header	None
Declaration	static void no_use_subclk_as_sysclk(void)
Description	Stop the sub-clock for processing when the sub-clock is used only as the RTC count source.
Arguments	None
Return Value	None
<hr/>	
resetting_wtcr_mainclk <hr/>	
Outline	Resetting the wait control register (RTC count source is the main clock)
Header	None
Declaration	static void resetting_wtcr_mainclk(void)
Description	Reset the wait control register when exiting from software standby mode. Set the minimum value to the wait control register.
Arguments	None
Return Value	None
<hr/>	
resetting_wtcr_subclk <hr/>	
Outline	Resetting the wait control register (RTC count source is the sub-clock)
Header	None
Declaration	static void resetting_wtcr_subclk(void)
Description	Reset the wait control register when exiting from software standby mode. Set the minimum value to the wait control register.
Arguments	None
Return Value	None
<hr/>	
enable_RTC <hr/>	
Outline	Initialization when using the RTC
Header	None
Declaration	static void enable_RTC(void)
Description	Initialize the settings when using the RTC (setting for clock provision and RTC software reset).
Arguments	None
Return Value	None
<hr/>	
disable_RTC_mainclk <hr/>	
Outline	Initialization when not using the RTC (RTC count source is the main clock)
Header	None
Declaration	static void disable_RTC_mainclk(void)
Description	Initialize the settings when not using the RTC.
Arguments	None
Return Value	None

disable_RTC_subclk	
Outline	Initialization when not using the RTC (RTC count source is the sub-clock)
Header	None
Declaration	static void disable_RTC_subclk(void)
Description	Initialize the settings when not using the RTC.
Arguments	None
Return Value	None
cmt0_wait	
Outline	Wait processing
Header	None
Declaration	static void cmt0_wait(uint32_t cnt)
Description	This function is used when waiting for the oscillation stabilization wait time.
Arguments	uint32_t cnt: Oscillation stabilization wait time $\text{cnt} = \text{oscillation stabilization wait time (ns)}^{(1)} \div \text{FOR_CMT0_TIME}^{(2)}$
Return Value	None
Remarks	<ol style="list-style-type: none"> 1. The oscillation stabilization wait time varies depending on the crystal/ceramic resonator. Set the value referring to 3.3.3 Oscillation Stabilization Wait Time for Each Clock. 2. The value of FOR_CMT0_TIME varies depending on the RTC count source. FOR_CMT0_TIME is calculated using 55 MHz (max.) as a HOCO value when the RTC count source is the main clock, and 143.75 kHz (max.) as a LOCO value when the RTC count source is the sub-clock. The actual wait time may differ according to the HOCO or LOCO frequency.

3.9 Flowcharts

3.9.1 Main Processing

Figure 3.4 shows the Main Processing.

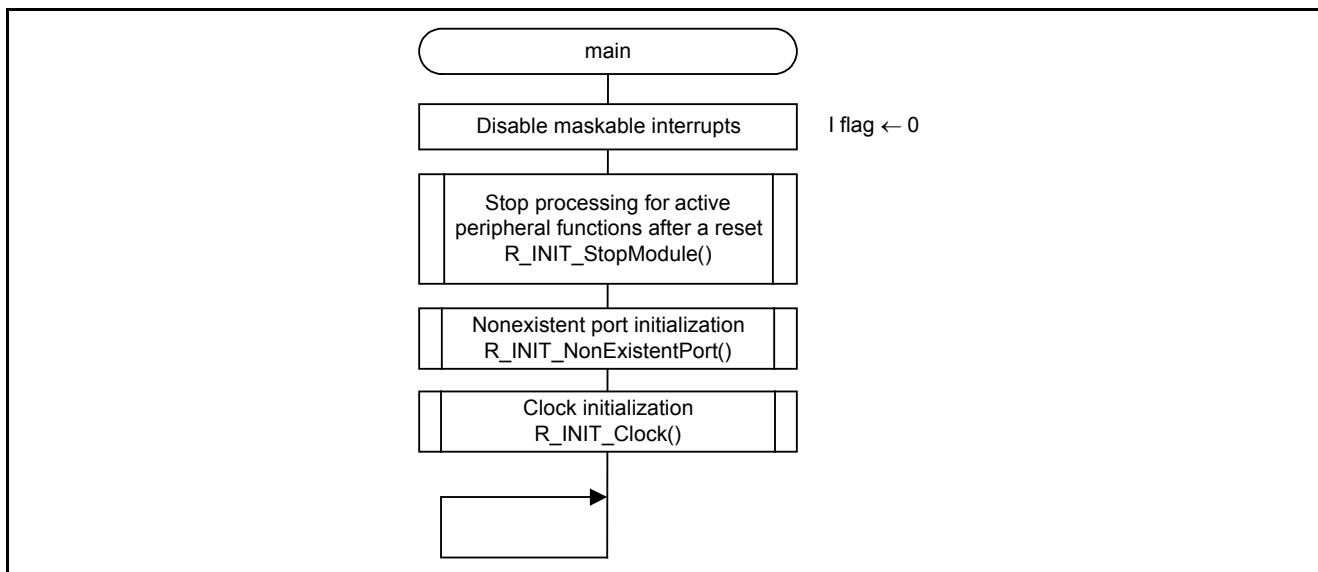


Figure 3.4 Main Processing

3.9.2 Stop Processing for Active Peripheral Functions after a Reset

Figure 3.5 shows the Stop Processing for Active Peripheral Functions after a Reset.

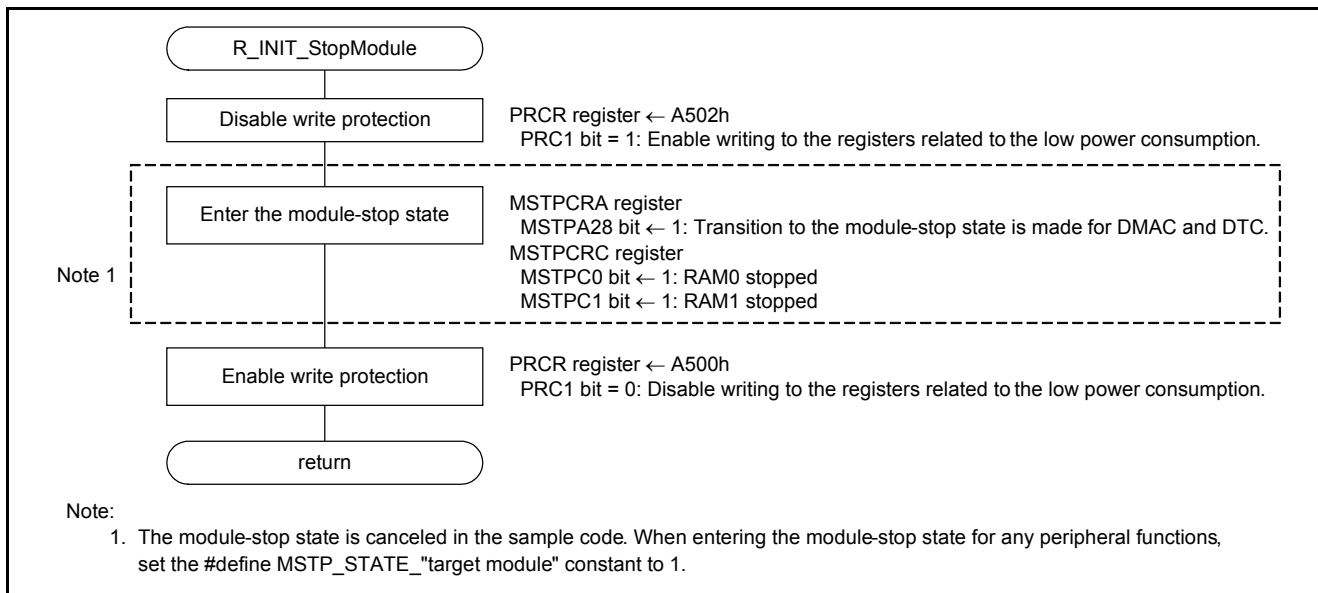


Figure 3.5 Stop Processing for Active Peripheral Functions after a Reset

3.9.3 Nonexistent Port Initialization

Figure 3.6 shows the Nonexistent Port Initialization.

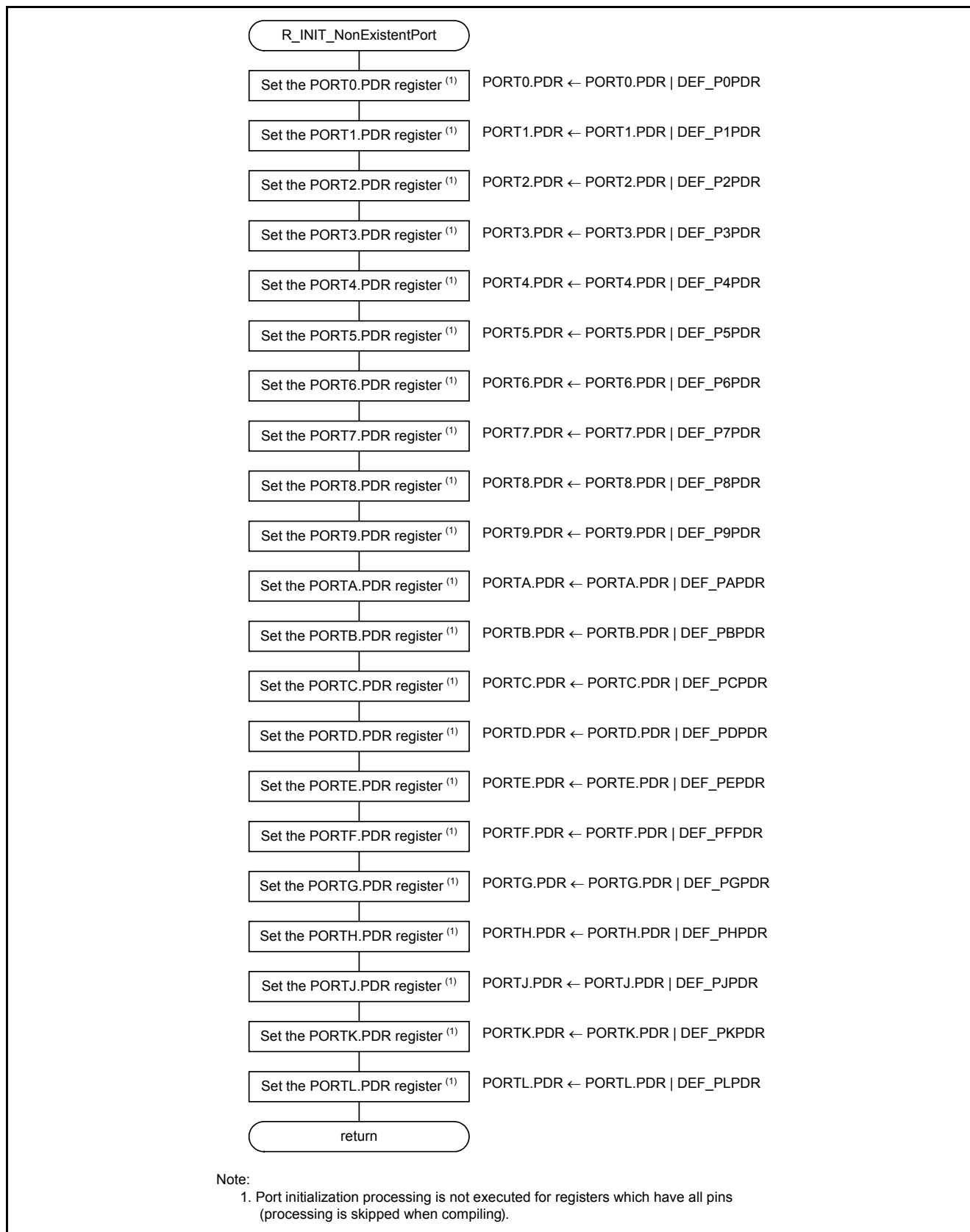


Figure 3.6 Nonexistent Port Initialization

3.9.4 Clock Initialization

Figure 3.7 shows the Clock Initialization.

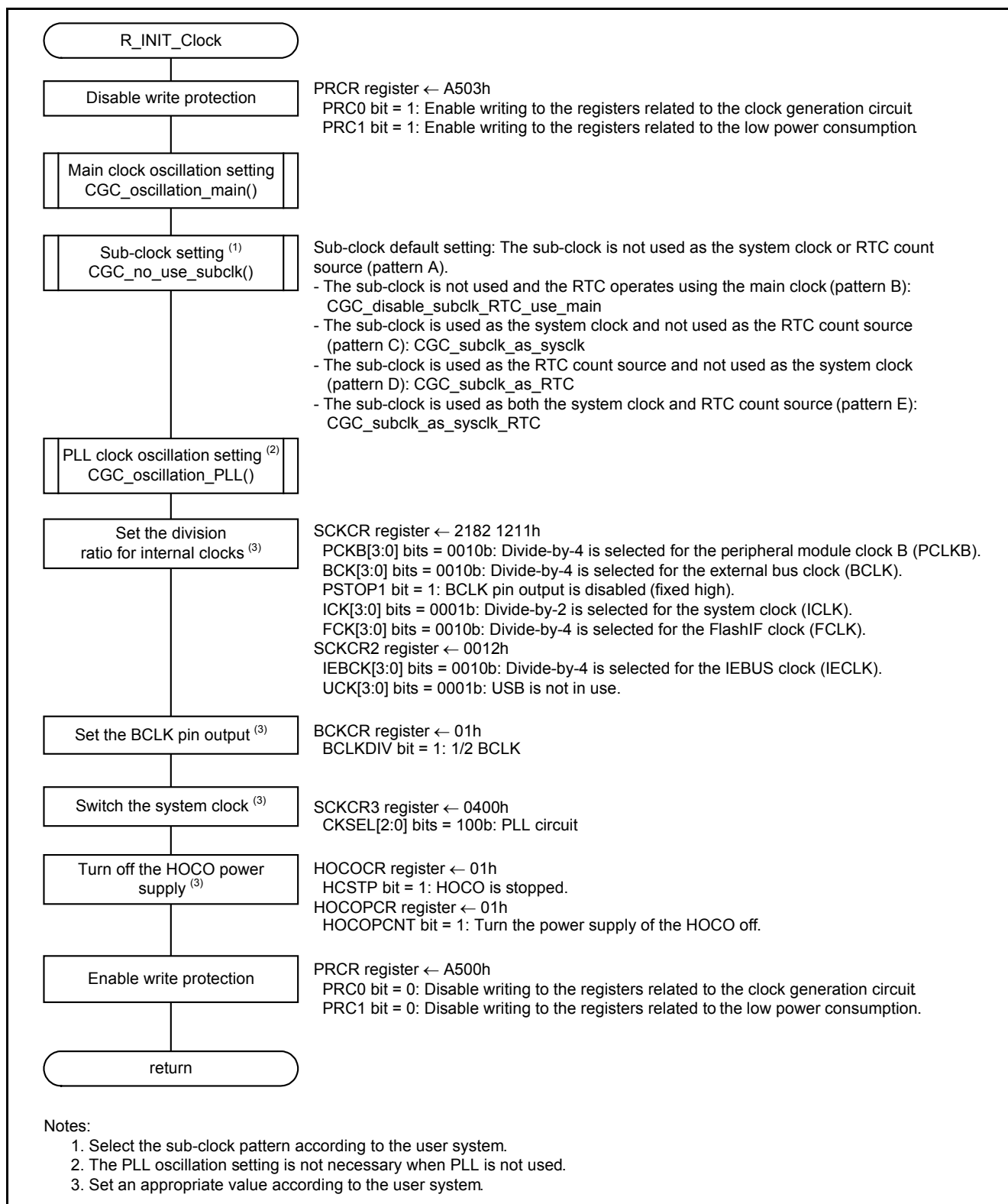


Figure 3.7 Clock Initialization

3.9.5 Main Clock Oscillation Setting

Figure 3.8 shows the Main Clock Oscillation Setting.

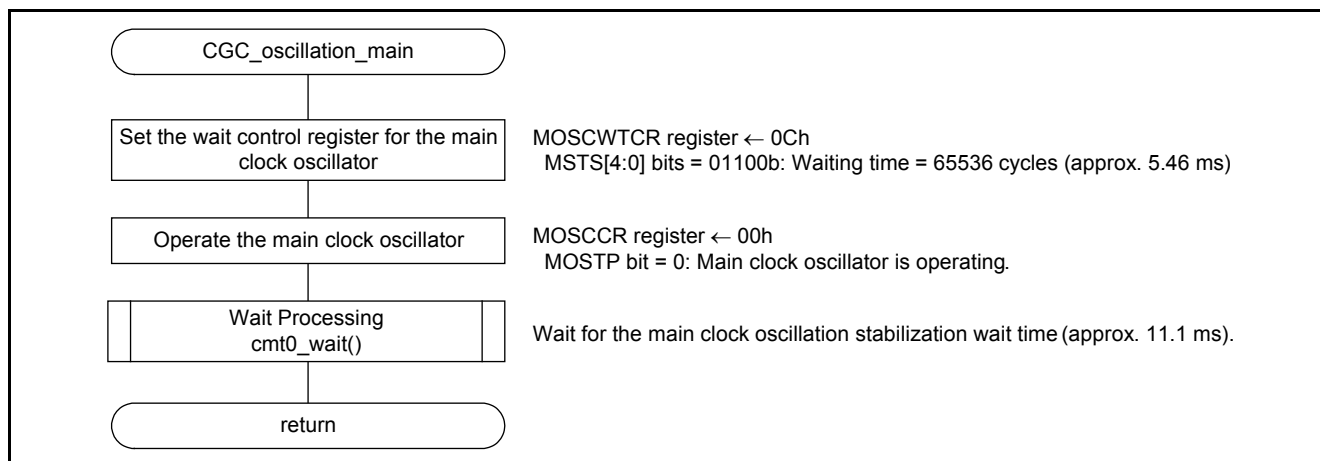


Figure 3.8 Main Clock Oscillation Setting

3.9.6 PLL Clock Oscillation Setting

Figure 3.9 shows the PLL Clock Oscillation Setting.

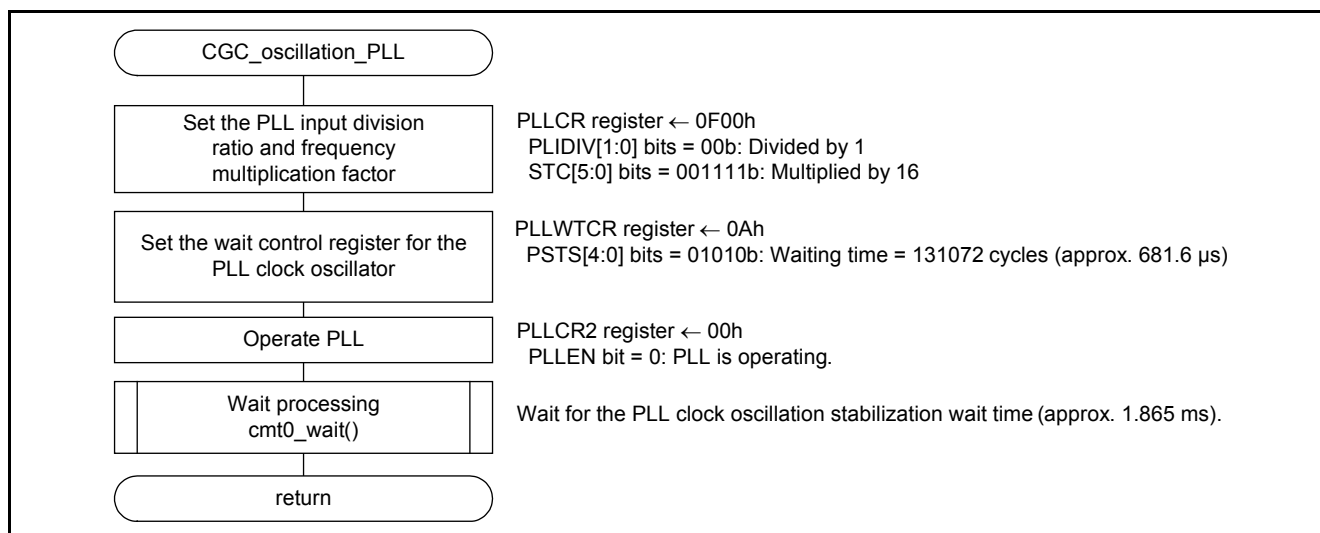


Figure 3.9 PLL Clock Oscillation Setting

3.9.7 HOCO Clock Oscillation Setting

Figure 3.10 shows the HOCO Clock Oscillation Setting.

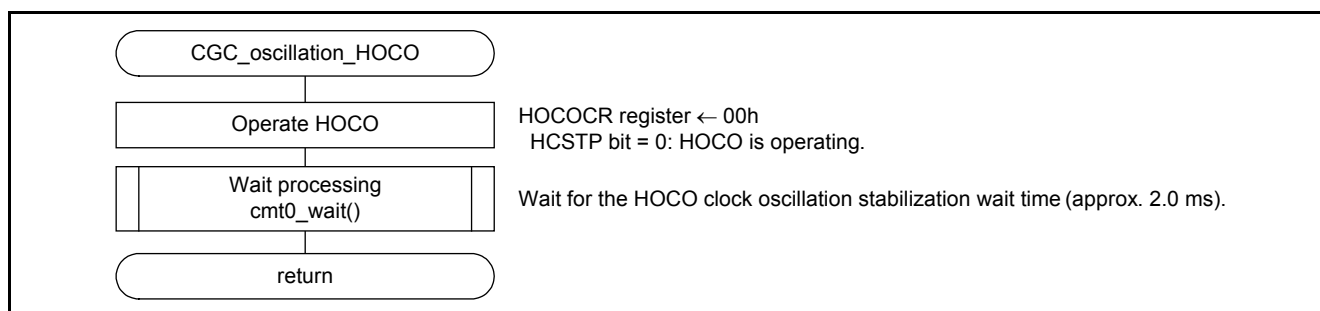


Figure 3.10 HOCO Clock Oscillation Setting

3.9.8 Sub-Clock Setting

Figure 3.11 to Figure 3.15 show the sub-clock setting patterns A to E.

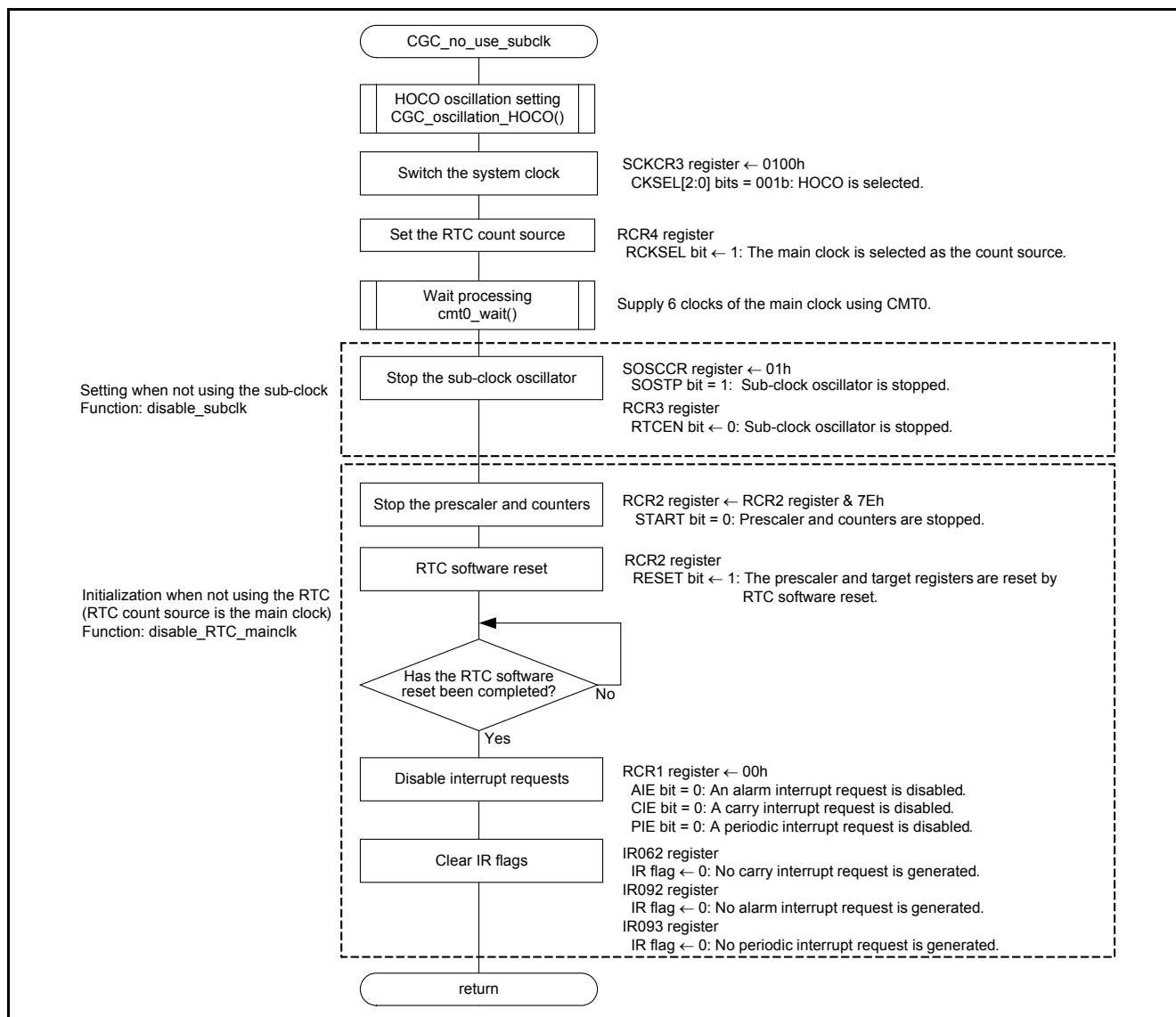


Figure 3.11 Sub-Clock Setting Pattern A (when the Sub-Clock is not Used as the System Clock or RTC Count Source)

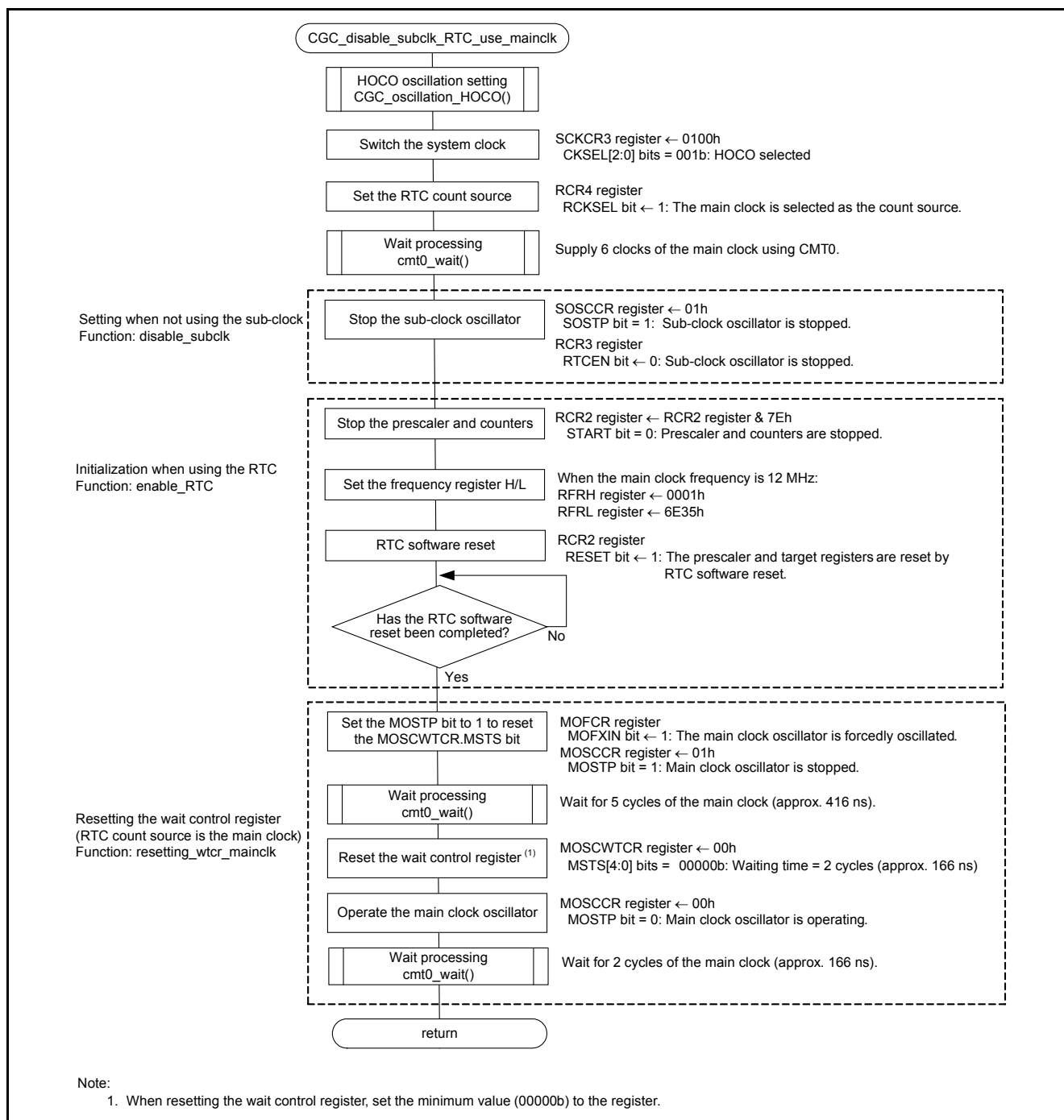


Figure 3.12 Sub-Clock Setting Pattern B (when the Sub-Clock is Stopped and the RTC Operates Using the Main Clock)

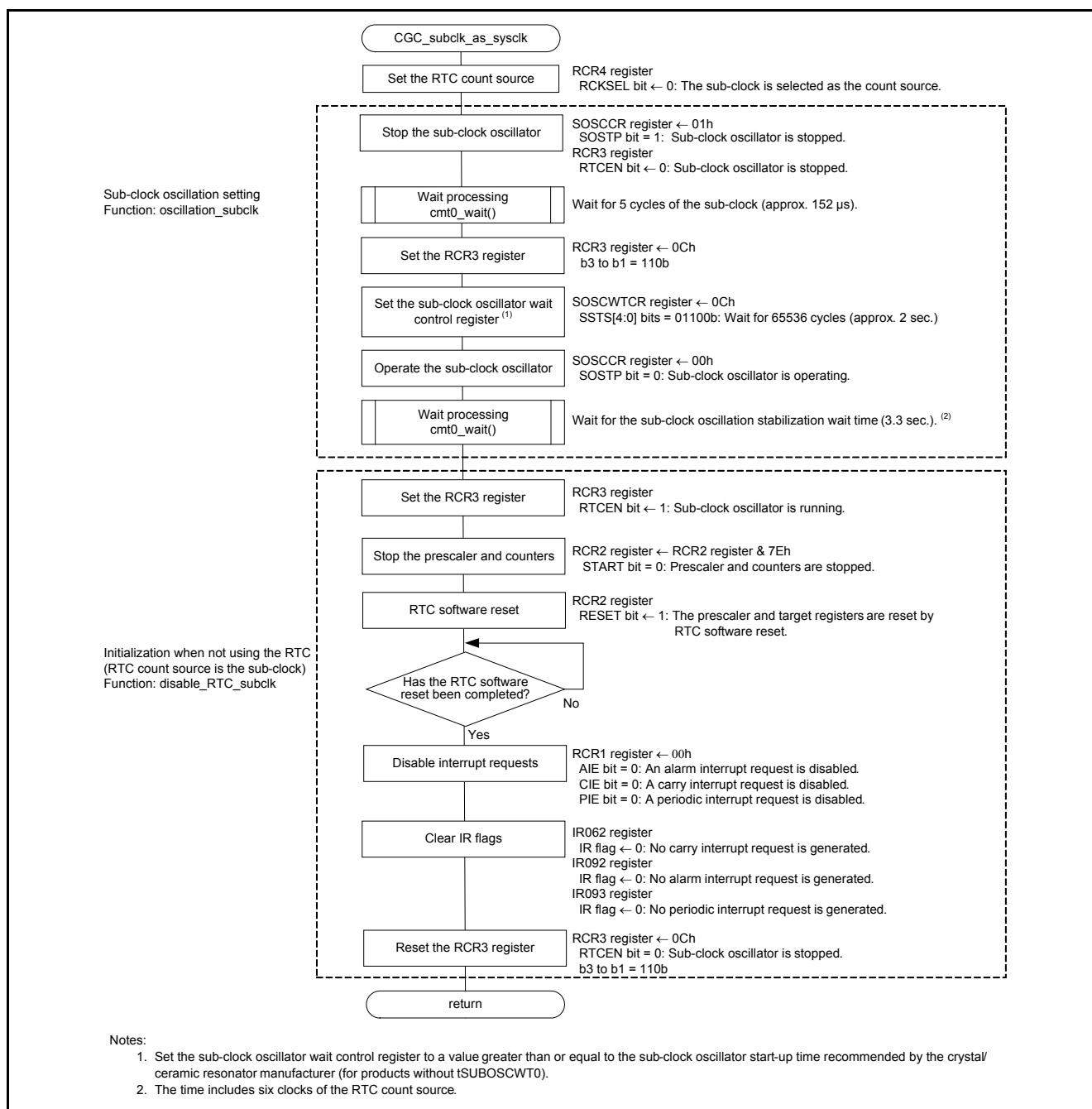


Figure 3.13 Sub-Clock Setting Pattern C (when the Sub-Clock is Used as the System Clock and not Used as the RTC Count Source)

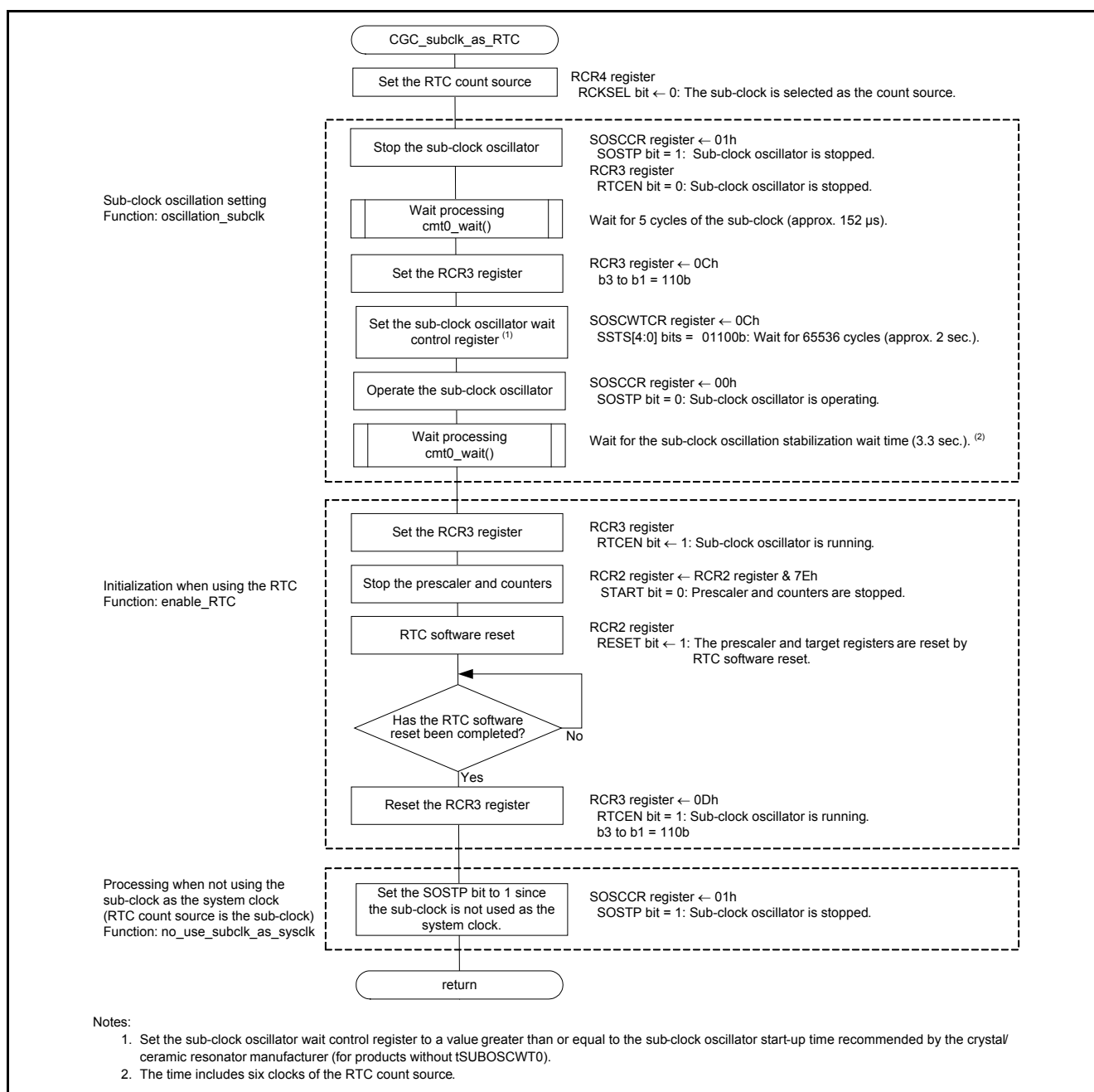


Figure 3.14 Sub-Clock Setting Pattern D (when the Sub-Clock is Used as the RTC Count Source and not Used as the System Clock)

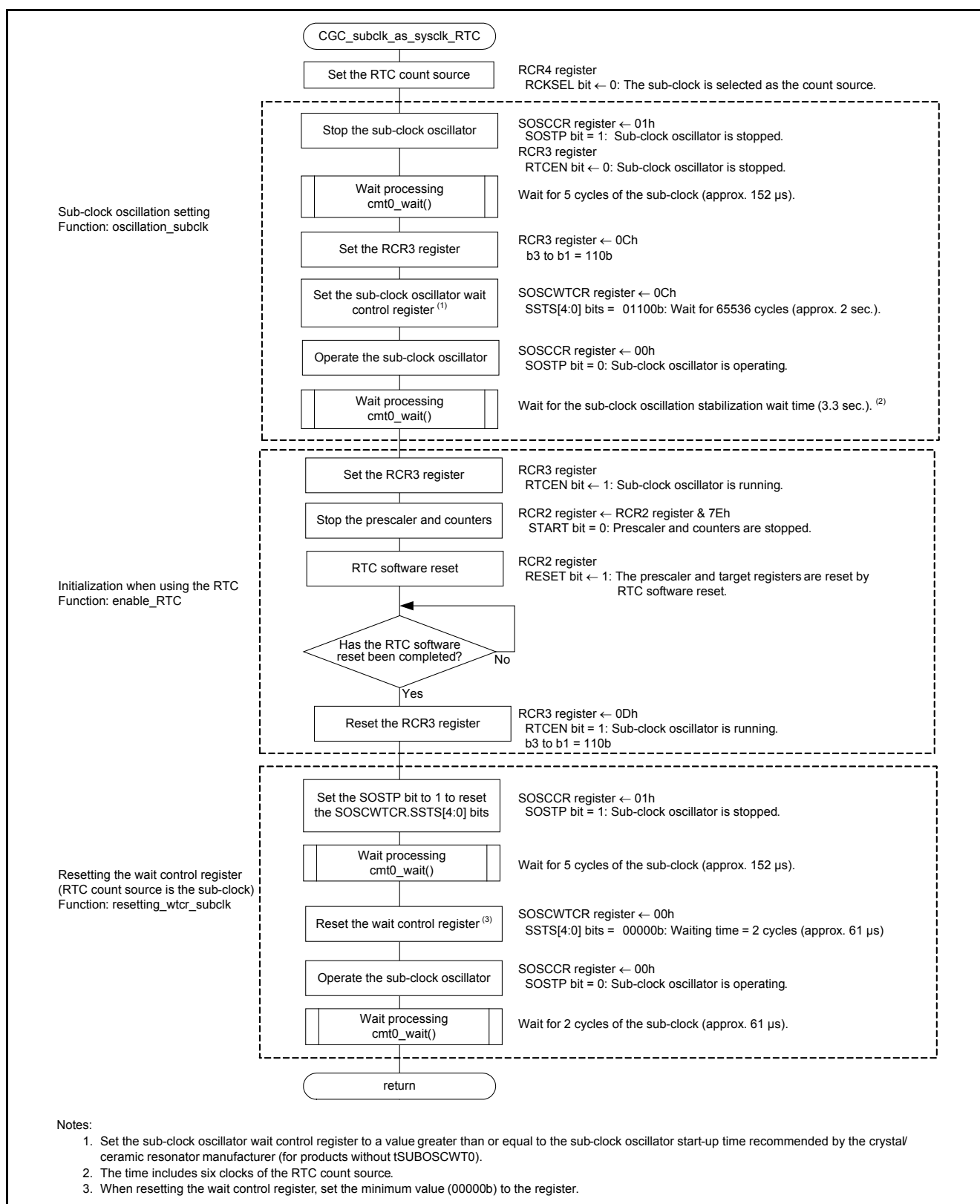


Figure 3.15 Sub-Clock Setting Pattern E (when the Sub-Clock is Used as Both the System Clock and RTC count source)

3.9.9 Wait Processing

Figure 3.16 shows the Wait Processing.

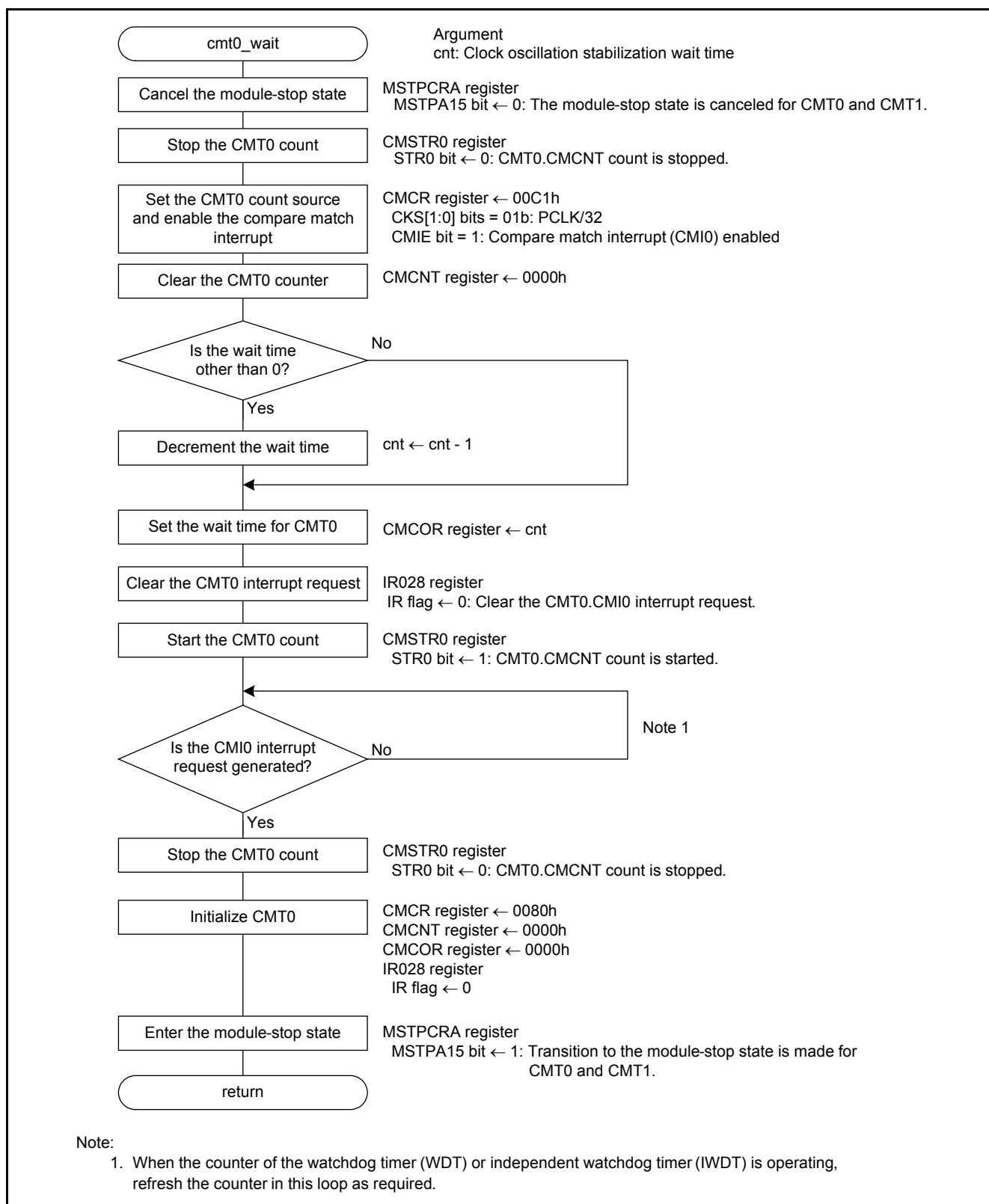


Figure 3.16 Wait Processing

4. Appendices

4.1 Clock Oscillation Stabilization Wait Time

4.1.1 Operating PLL before Main Clock Oscillation Stabilizes

When oscillating the main clock and PLL clock, their oscillation stabilization wait times can be combined into a single wait time.

Figure 4.1 shows the PLL Oscillation Stabilization Wait Time (when Operating PLL before the Main Clock Stabilizes) and Table 4.1 lists the Setting Value for the PLL Clock Wait Control Register and Oscillation Stabilization Wait Time (when Operating PLL before Main Clock Oscillation Stabilizes).

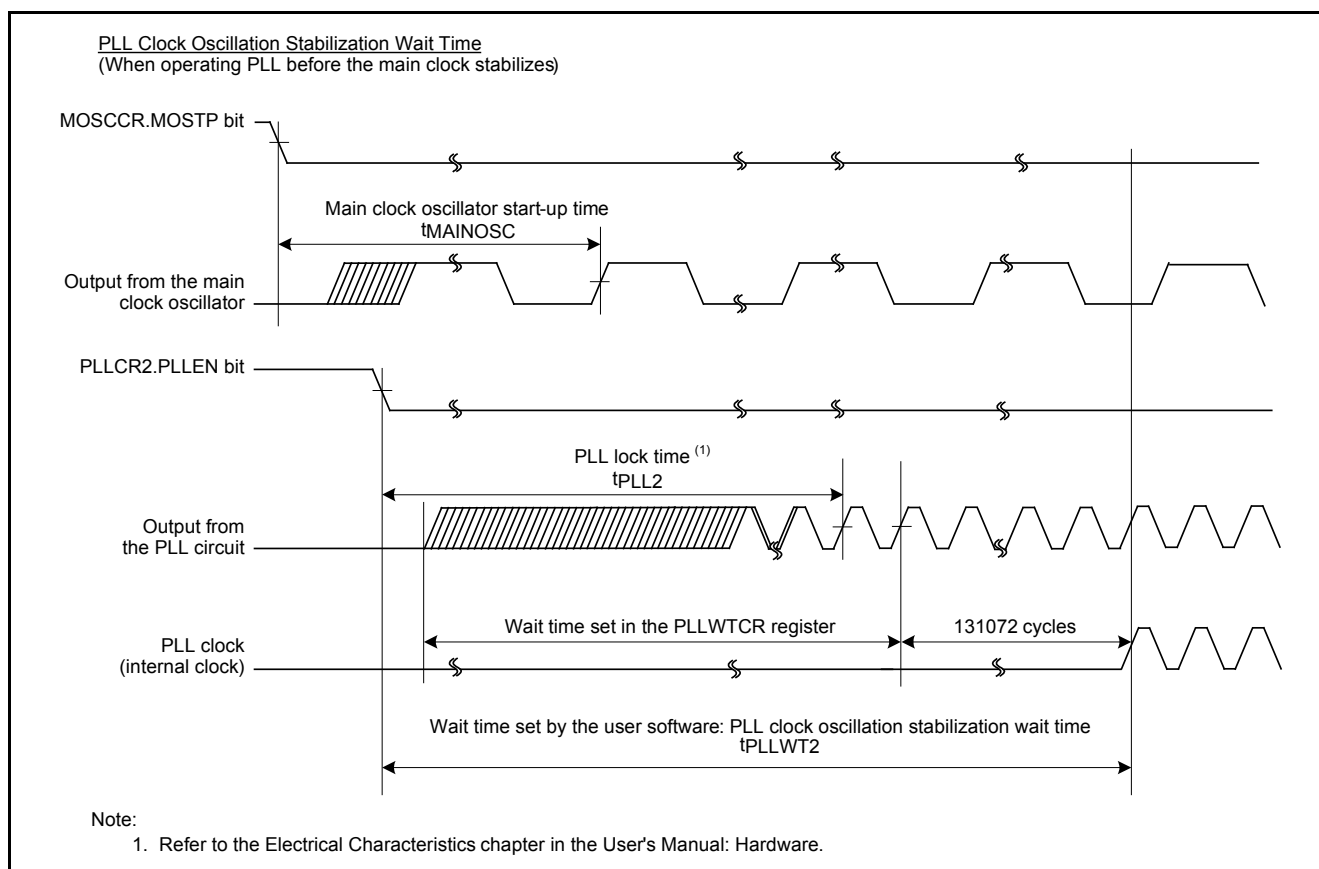


Figure 4.1 PLL Oscillation Stabilization Wait Time (when Operating PLL before the Main Clock Stabilizes)

Table 4.1 Setting Value for the PLL Clock Wait Control Register and Oscillation Stabilization Wait Time (when Operating PLL before Main Clock Oscillation Stabilizes)

Setting Item	Condition of Setting Value and Calculation Method
PLL wait control register (PLLWTCR.PSTS[4:0] bits)	Value greater than or equal to the main clock oscillator start-up time recommended by the crystal/ceramic resonator manufacturer plus t_{PLL1} (max. 500 μ s)
Oscillation stabilization wait time (t_{PLLWT2})	When n is the wait time selected by the PLLWTCR.PSTS[4:0] bits: $t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$

4.1.2 Using the Product with the Sub-Clock Oscillation Stabilization Wait Offset Time (tSUBOSCWT0)

4.1.2.1 When the Sub-Clock Oscillator Start-Up Time (tSUBOSC) is Less than tSUBOSCWT0

Figure 4.2 shows the Sub-Clock Oscillation Stabilization Wait Time (when tSUBOSC is less than tSUBOSCWT0) and Table 4.2 lists the Setting Value for the Sub-Clock Oscillator Wait Control Register and Oscillation Stabilization Wait Time (when tSUBOSC is less than tSUBOSCWT0).

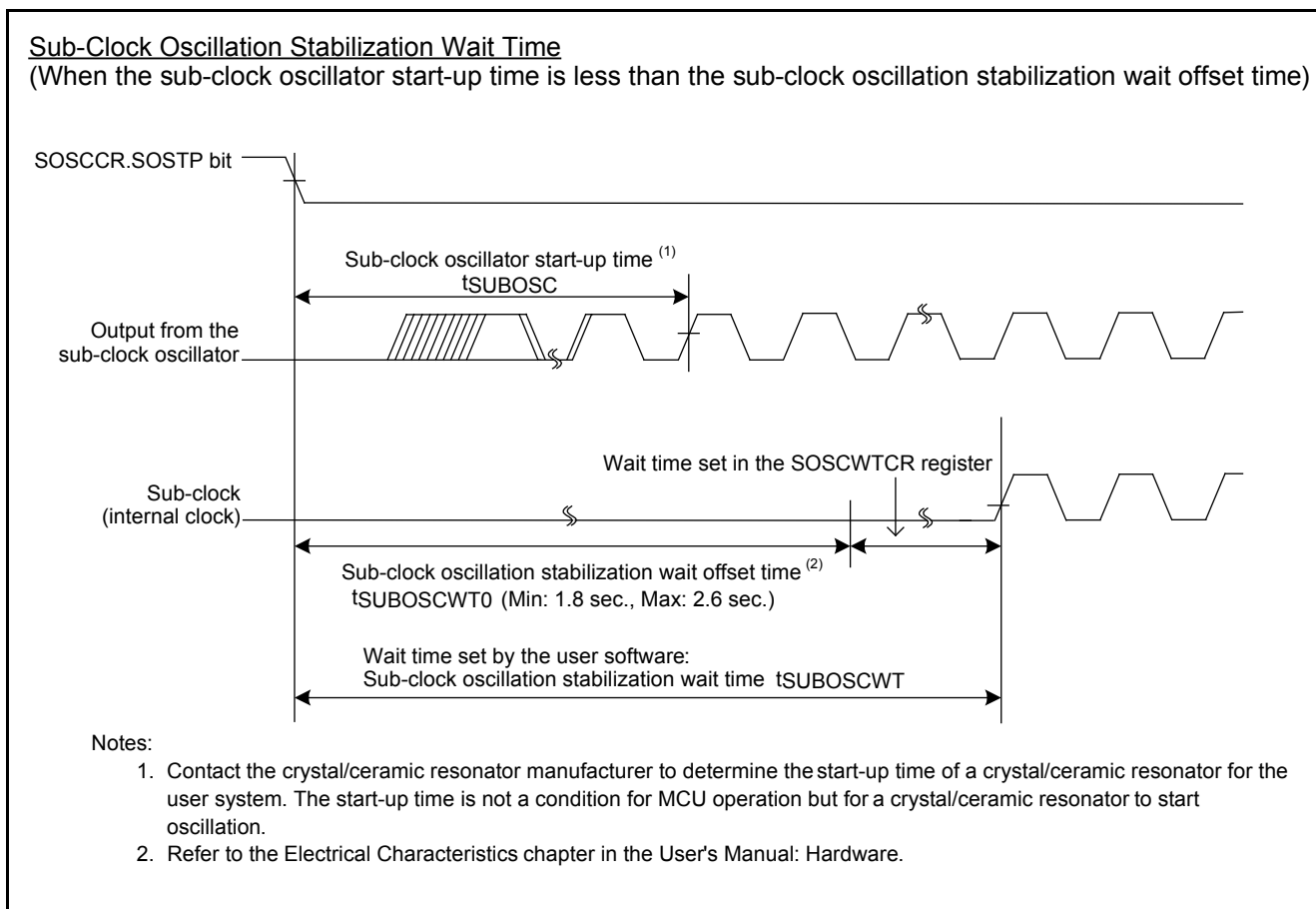


Figure 4.2 Sub-Clock Oscillation Stabilization Wait Time (when tSUBOSC is less than tSUBOSCWT0)

Table 4.2 Setting Value for the Sub-Clock Oscillator Wait Control Register and Oscillation Stabilization Wait Time (when tSUBOSC is less than tSUBOSCWT0)

Setting Item	Condition of Setting Value and Calculation Method
Sub-clock oscillator wait control register (SOSCWTCR.SSTS[4:0] bits)	Value greater than or equal to tSUBOSC recommended by the crystal/ceramic resonator manufacturer minus the minimum value of tSUBOSCWT0 (1.8 sec.)
Oscillation stabilization wait time (tSUBOSCWT)	When n is the wait time selected in the SOSCWTCR.SSTS[4:0] bits: $\text{Maximum value of } tSUBOSCWT0 (2.6 \text{ sec.}) + \frac{n}{f_{SUB}}$

4.1.2.2 When the Sub-Clock Oscillator Start-Up Time (t_{SUBOSC}) is Greater than the Sub-Clock Oscillation Stabilization Wait Offset Time ($t_{\text{SUBOSCWT0}}$)

Figure 4.3 shows the Sub-Clock Oscillation Stabilization Wait Time (when t_{SUBOSC} is Greater than $t_{\text{SUBOSCWT0}}$) and Table 4.3 lists the Setting Value for the Sub-Clock Oscillator Wait Control Register and Oscillation Stabilization Wait Time (when t_{SUBOSC} is Greater than $t_{\text{SUBOSCWT0}}$).

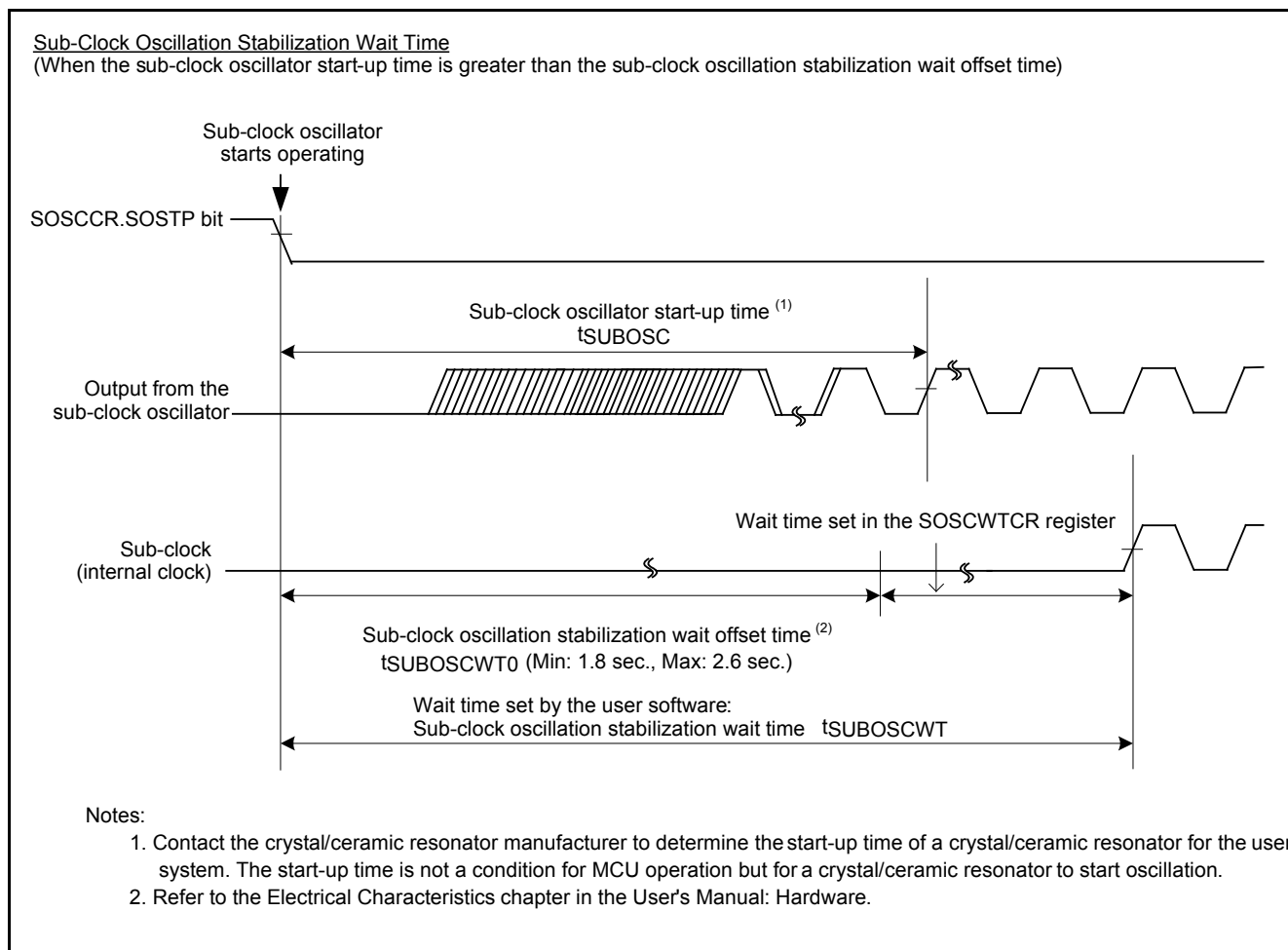


Figure 4.3 Sub-Clock Oscillation Stabilization Wait Time (when t_{SUBOSC} is Greater than $t_{\text{SUBOSCWT0}}$)

Table 4.3 Setting Value for the Sub-Clock Oscillator Wait Control Register and Oscillation Stabilization Wait Time (when t_{SUBOSC} is Greater than $t_{\text{SUBOSCWT0}}$)

	Condition of Setting Value and Calculation Method
Sub-clock oscillator wait control register (SOSCWT0CR.SSTS[4:0] bits)	Value greater than or equal to t_{SUBOSC} recommended by the crystal/ceramic resonator manufacturer minus the minimum value of $t_{\text{SUBOSCWT0}}$ (1.8 sec.)
Oscillation stabilization wait time (t_{SUBOSCWT})	When n is the wait time selected in the SOSCWT0CR.SSTS[4:0] bits: エラー! リンクが正しくありません。

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040EJ)

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)

The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

<http://www.renesas.com>

Inquiries

<http://www.renesas.com/contact/>

REVISION HISTORY	RX630 Group Application Note Initial Setting
-------------------------	---

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 5, 2013	—	First edition issued

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Ampcorp, Ampcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141