RX62T

GPT Three-Phase Saw-Wave Complementary PWM

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Introduction

The RX62T Group has a general PWM timer (GPT) consisting of a four-channel 16-bit timer, the GPT operates at a maximum of 100 MHz. This application note is going to show the setting of three-phase saw-wave complementary PWM with automatic dead time setting in GPT function.

Target Device

RX62T

Contents

1. Specification

- 16 bit x 4channels
- Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter.
- Clock sources independently selectable for each channel.
- Two input/output pins per channel.
- Two output compare/input capture registers per channel.
- For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use.
- In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms.
- Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow).
- Synchronically operation of the several counters
- Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting).
- Generation of dead times in PWM operation.
- Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times.
- Starting, clearing, and stopping counters in response to external or internal triggers.
- ınternal trigger sources: output of the internal comparator, software, and compare match.
- The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the IWDT-dedicated low-speed on-chip oscillator clock signal (to detect abnormal oscillation).

Fig. 1-1 is the block diagram of General PWM Timer (GPT).

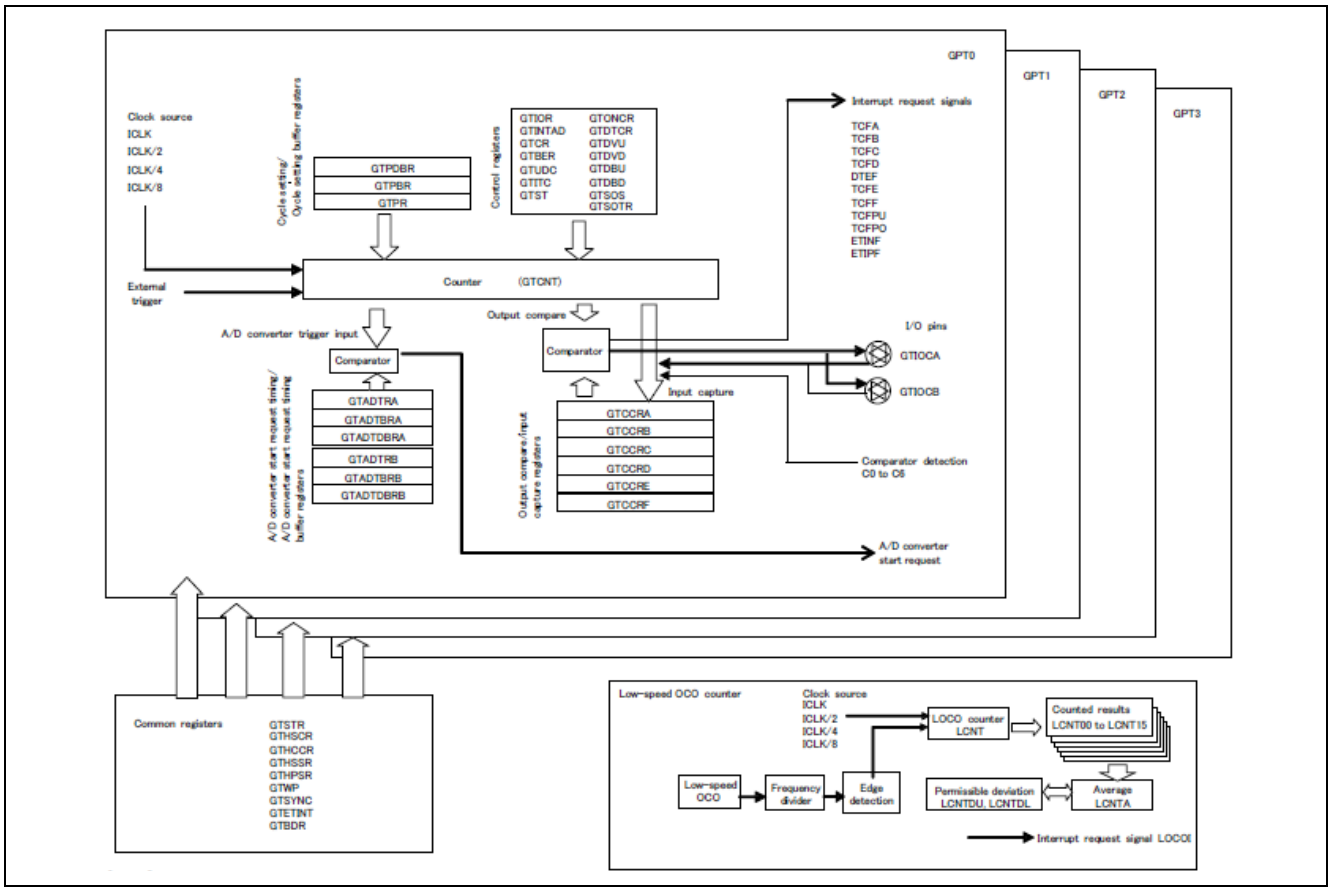


Figure 1-1 Block diagram for GPT

Table 1-1 Specifications of General PWM Timer (GPT) Register

GTSTR	General PWM timer software start register
GTHSCR	General PWM timer hardware source start control register
GTHCCR	General PWM timer hardware source clear control register
GTHSSR	General PWM timer hardware start source select register
GTHPSR	General PWM timer hardware stop/clear source select register
GTWP	General PWM timer write-protection register
GTSYNC	General PWM timer sync register
GTETINT	General PWM timer external trigger input interrupt register
GTBDR	General PWM timer buffer operation disable register
GTIOR	General PWM timer I/O control register
GTINTAD	General PWM timer interrupt output setting register
GTCR	General PWM timer control register
GTBER	General PWM timer buffer enable register
GTUDC	General PWM timer count direction register
GTITC	General PWM timer interrupt and A/D converter start request skipping setting
GTST	General PWM timer status register
GTCNT	General PWM timer counter value
GTCCRA	General PWM timer compare capture register A
GTCCRB	General PWM timer compare capture register B
GTCCRC	General PWM timer compare capture register C
GTCCRD	General PWM timer compare capture register D
GTCCRE	General PWM timer compare capture register E
GTCCRF	General PWM timer compare capture register F
GTPR	General PWM timer cycle setting register
GTPBR	General PWM timer cycle setting buffer register
GTPDBR	General PWM timer cycle setting double-buffer register
GTADTRA	A/D converter start request timing register A
GTADTBRA	A/D converter start request timing buffer register A
GTADTDBRA	A/D converter start request timing double-buffer register A
GTADTRB	A/D converter start request timing register B
GTADTBRB	A/D converter start request timing buffer register B
GTADTDBRB	A/D converter start request timing double-buffer register B
GTONCR	General PWM timer output negate control register
GTDTCR	General PWM timer dead time control register
GTDVU	General PWM timer dead time value register
GTDVD	General PWM timer dead time value register

2. Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

2.1 Example Three Channel Synchronized Operation

Figure 2.1 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

By setting GTDTCR, a negative-phase waveform with dead time based on the dead time value registers GTDVU and GTDVD can be output from each pin.

Fig. 2-1 shows an example of Saw-Wave One-Shot Pulse Mode operation.

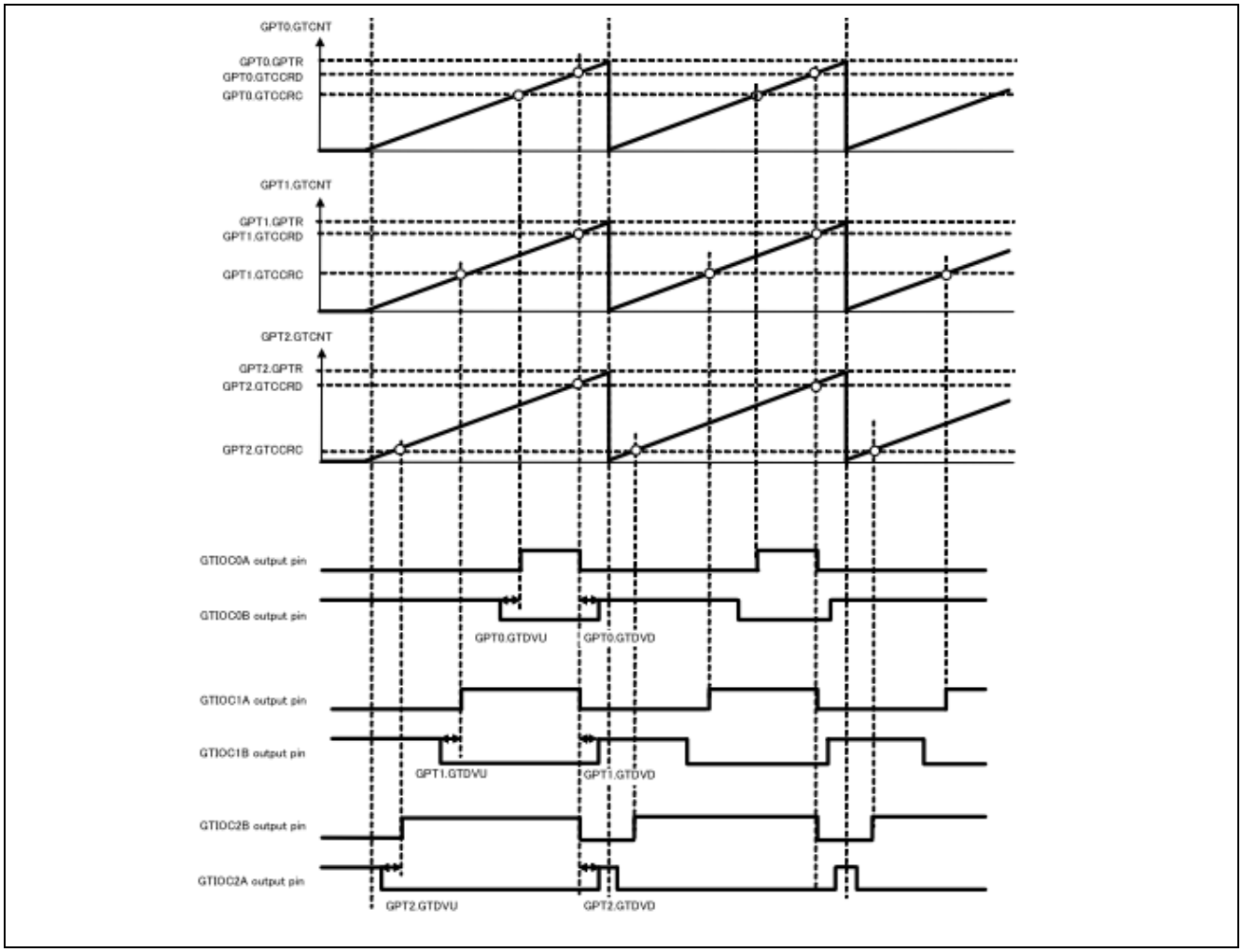


Figure 2-1 Example of Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

2.2 Example of Procedure for Setting Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

Fig. 2-2 shows an example of the procedure for setting Saw-Wave One-Shot Pulse Mode.

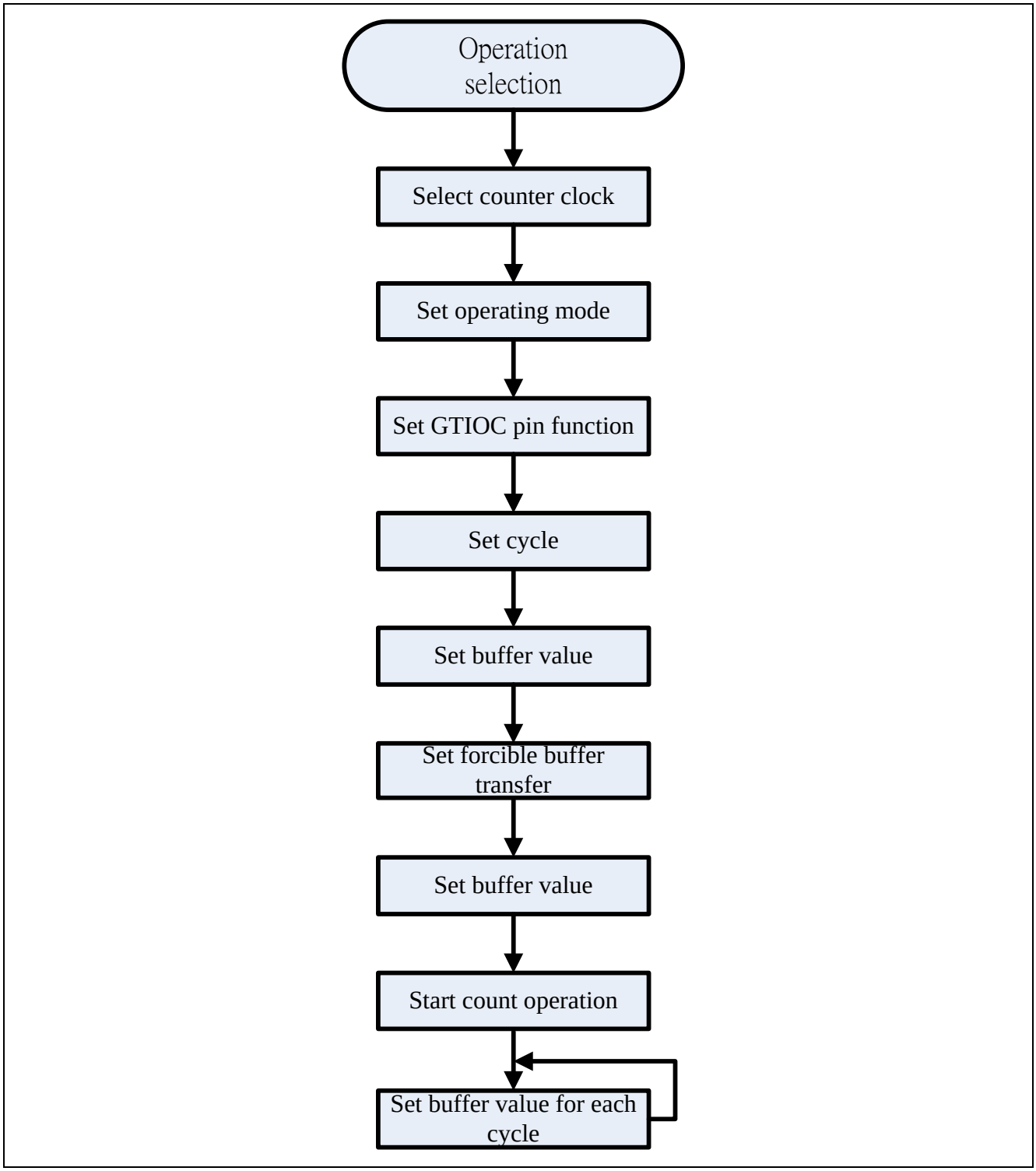


Figure 2-2 Example of Procedure for Setting Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

3. General PWM Timer Software Register Setting

General PWM Timer Control Register (GTCR):

GTCR controls GTCNT.
GTCR should be set while GTCNT operation is stopped.

When synchronized clearing is selected, synchronized clearing is handled equally to clearing by the counter's overflow or underflow in saw-wave mode. The output of output compare is changed and buffer transfer performed. However, the overflow flag and underflow flag are not changed.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CCLR[1:0]		—	—	TPCS[1:0]		—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MD[2:0]	Mode Select	b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at crest) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) fixed buffer operation) 1 1 1: Setting prohibited	R/W
b7 to b3	—	(Reserved)	These bits are read as 0. The write value should be 0.	R/W
b8, b9	TPCS[1:0]	Timer Prescaler Select	b8 b9 0 0: ICLK (system clock) 0 1: ICLK/2 (system clock) 1 0: ICLK/4 (system clock) 1 1: ICLK/8 (system clock)	R/W
b11, b10	—	(Reserved)	These bits are read as 0. The write value should be 0.	R/W
b13, b12	CCLR[1:0]	Counter Clear	b13 b12 0 0: Controlled only by GPTn.GTPR. 0 1: GPTn.GTCNT cleared by GPTn.GGTCCRA input capture 1 0: GPTn.GTCNT cleared by GPTn.GTCCRB input capture 1 1: Cleared by counter clearing in another channel performing synchronized clearing/synchronized operation	
b15, b14	—	(Reserved)	These bits are read as 0. The write value should be 0.	R/W

Figure 3-1 GTCR Setting

General PWM Timer I/O Control Register (GTIOR):

GPTn.GTIOR sets the functions of the GTIOCnA and GTIOCnB pins (n = 0 to 3). Each channel has one GTIOCnA pin and one GTIOCnB pin.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBHLD	OBDFLT	GTIOB[5: 0]						OAHLD	OADFLT	GTIOA[5: 0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	GTIOA[5:0]	GTIOCnA Pin Function Select	See table 17.5.	R/W
b6	OADFLT	Output Value at GTIOCnA Pin Count Stop	Output value is specified.	R/W
b7	OAHLD	Output Retain at GTIOCnA Pin Count Start/Stop	0: Register setting is used 1: Output is retained	R/W
b13 to b8	GTIOB[5:0]	GTIOCnB Pin Function Select	See table 17.5.	R/W
b14	OBDFLT	Output Value at GTIOCnB Pin Count Stop	Output value is specified.	R/W
b15	OBHLD	Output Retain at GTIOCnB Pin Count Start/Stop	0: Register setting is used 1: Output is retained	R/W

Figure 3-2 GTIOR Setting

General PWM Timer Cycle Setting Buffer Register (GTPBR):

The first have to set the counter cycle from GTPR register and the GTPBR is the buffer for GTPR

General PWM Timer Compares Capture Register C (GTCCRC):

Set the compare match value.

General PWM Timer Dead Time Control Register (GTDTCR):

GTDTCR enables automatic setting of a negative-phase waveform with dead time.

From Fig. 3-3 the TDE have set to 1, compare match value of a negative-phase waveform with Dead time is automatically set to GPTn.GTCCRB and TDFER is also set to1, TDBUE and TDBDE is also set to 1 that buffer operation enable.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: Normal operation 1: Compare match value of a negative-phase waveform with dead time is automatically set to GPTn.GTCCRB	R/W
b3 to b1	—	(Reserved)	These bits are read as 0. The write value should be 0.	R/W
b4	TDBUE	GTDVU Buffer Operation Enable	0: GPTn.GTDVU buffer operation is disabled 1: GPTn.GTDVU buffer operation is enabled	R/W
b5	TDBDE	GTDVD Buffer Operation Enable	0: GPTn.GTDVD buffer operation is disabled 1: GPTn.GTDVD buffer operation is enabled	R/W
b7, b6	—	(Reserved)	These bits are read as 0. The write value should be 0.	R/W
b8	TDFER	GTDVD Setting	0: Normal operation (GPTn.GTDVU and GPTn.GTDVD operate separately) 1: The value written to GPTn.GTDVU is set to GPTn.GTDVD	R/W
b15 to b9	—	(Reserved)	These bits are read as 0. The write value should be 0.	R/W

Figure 3-3 GTDTCR Setting

General PWM Timer Dead Time Values Register (GTDVU):

Set the dead time value.

General PWM Timer Dead time Buffer Register (GTDBU):

This register is GTDVU buffer.

General PWM Timer Buffer Enable Register (GTBER):

GTBER makes settings for buffer operation.
GTBER should be set while GTCNT operation is stopped.

From Fig. 3-4 The PR bits set 0x03 that GTPR is double buffer operation.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCRA[1:0]	GTCCRA Buffer Operation	b1 b0 0 0: Buffer operation is not performed 0 1: Single buffer operation (GPTn.GTCCRA ⇔ GPTn.GTCCRC) 1 x: Double buffer operation (GPTn.GTCCRA ⇔ GPTn.GTCCRC ⇔ GPTn.GTCCRD)	R/W
b3, b2	CCRB[1:0]	GTCCRB Buffer Operation	b3 b2 0 0: Buffer operation is not performed 0 1: Single buffer operation (GPTn.GTCCRB ⇔ GPTn.GTCCRE) 1 x: Double buffer operation (GPTn.GTCCRB ⇔ GPTn.GTCCRE ⇔ GPTn.GTCCRF)	R/W
b5, b4	PR[1:0]	GTPR Buffer Operation	b5 b4 0 0: Buffer operation is not performed 0 1: Single buffer operation (GPTn.GTPR ⇔ GPTn.GTPBR) 1 x: Double buffer operation (GPTn.GTPR ⇔ GPTn.GTPBR ⇔ GPTn.GTPDBR)	R/W

Figure 3-4 GTBER Setting

General PWM Timer Output Negate Control Register (GTONCR):

GTONCR controls negate of the GTIOCnA pin output and GTIOCnB pin output.

From Fig. 3-5 the OAE and OBE bits should set to 1, GTIOCnA and GTIOCnB Pin output enable.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBE	OAE	—	SWN	—	—	—	NFV	NFS[3:0]				NVB	NVA	NEB	NEA
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Figure 3-5 GTONCR Setting

4. Experiment Result

Fig. 4-1 to Fig. 4-3 the f_{sw} is 20 kHz. Dead time is 2*us*, Fig. 4-1 is GPT for 25% duty; Fig. 4-2 is GPT for 50% duty; and Fig. 4-3 is GPT for 75% duty.

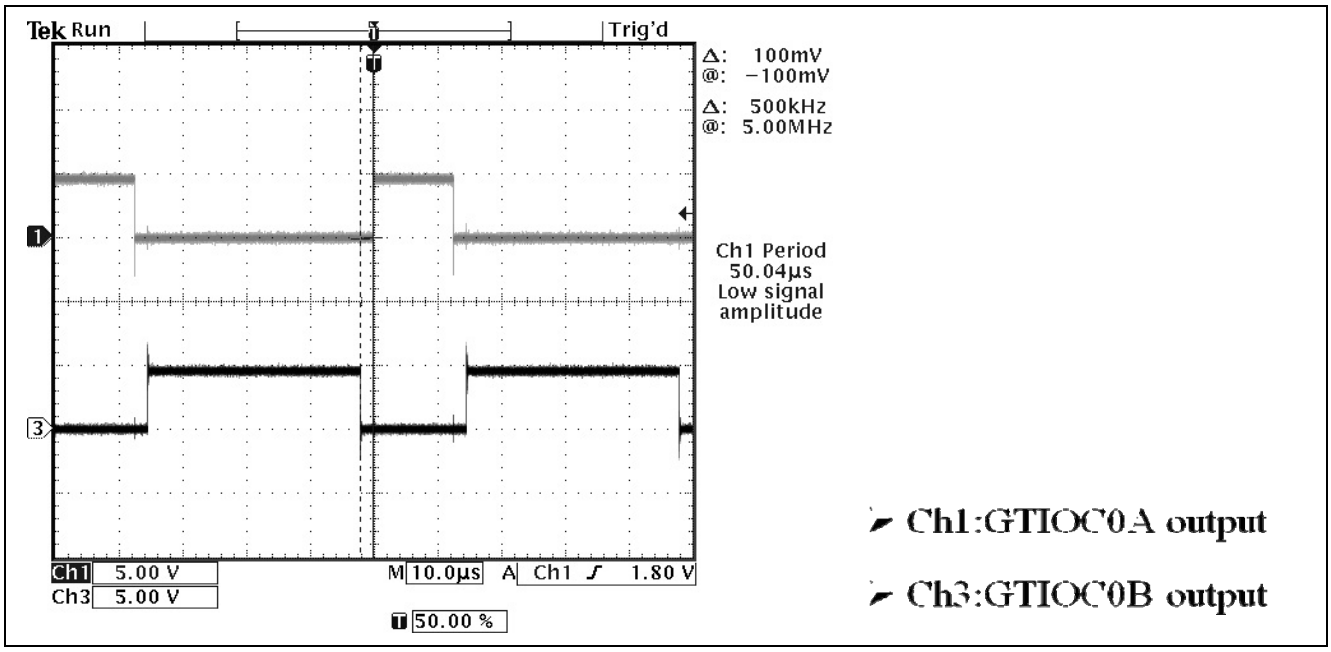


Figure 4-1 GPT output for 25% duty

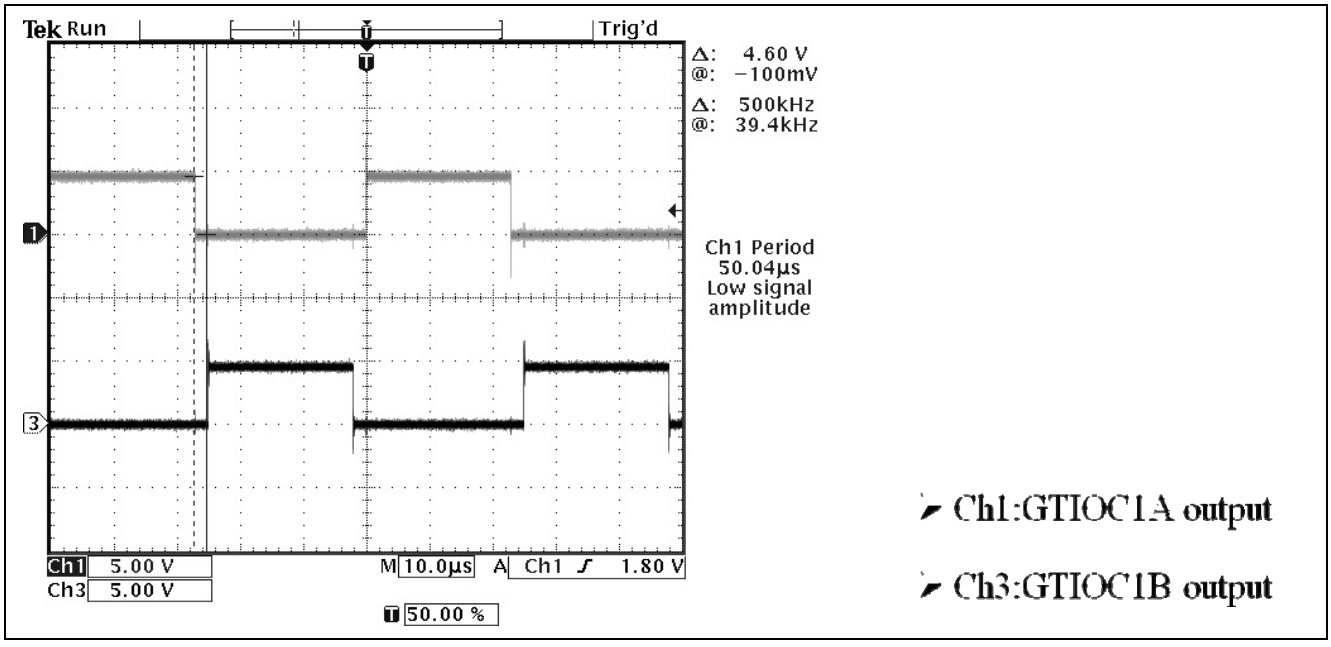
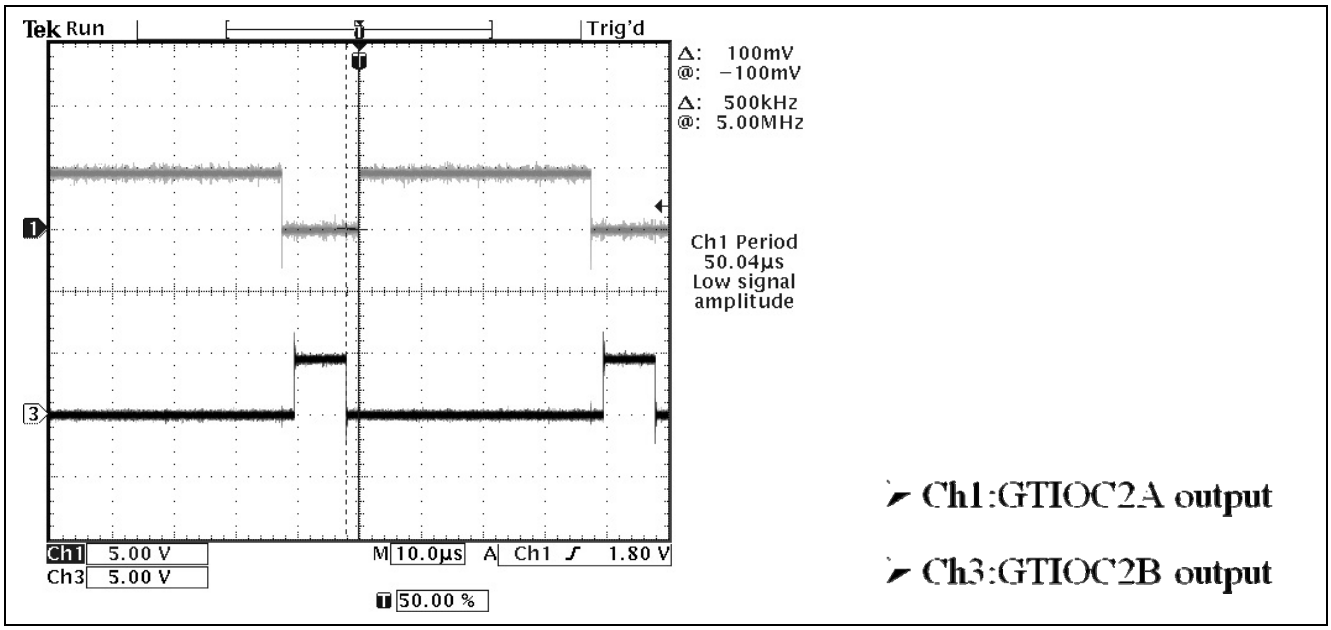
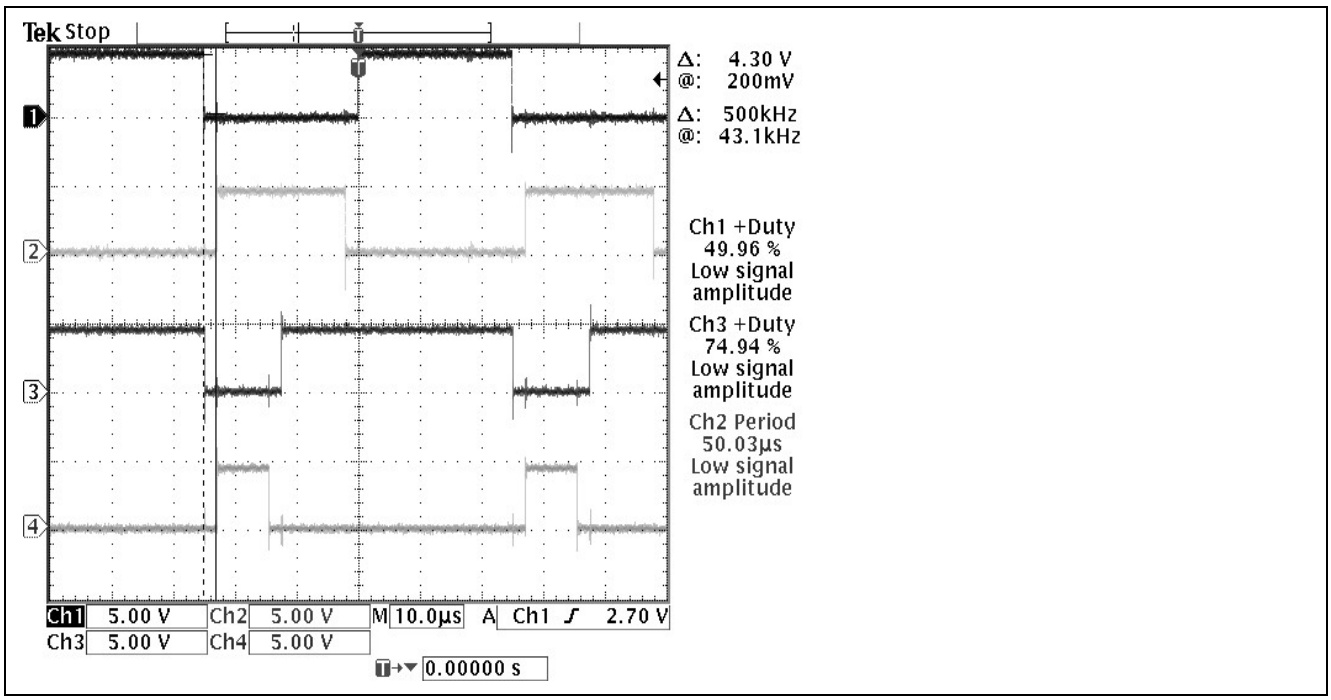


Figure 4-2 GPT output for 50% duty



4-3 GPT output for 75% duty

Fig. 4-4 shows the synchronized operation between GPT2 and GPT3.



4-4 Synchronized operation between GPT2 and GPT3

5. Conclusion

From experimental result, we can use General PWM Timer for Saw-Wave One-Shot Pulse Mode control.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	October.01.11	—	First edition issued

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