RX610 Group

Asynchronous SCI Reception Using DTC (Little Endian)

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Abstract

This application note presents an example of asynchronous serial communication using the serial communication interface (SCI) and data transfer controller (DTC) of a Renesas MCU.

Target Device

RX610 Group

Introduction

This application note applies to the following MCUs and conditions.

RX610 Group

The program can be used with other RX Family MCUs that have the same I/O registers (peripheral device control registers) as the RX610 Group. Check the latest version of the manual for any additions and modifications to the functions used by this application note. Careful evaluation is recommended before using this application note.

The program works with an endian specification of little endian only and with left or right specified as the bit order.

Contents

1. Specifications

The data transfer controller (DTC) and asynchronous serial communication function of the serial communication interface (SCI) are used to receive data. Figure 1 presents an overview of asynchronous serial data reception using the DTC.

1. Channel 1 of the SCI and the DTC are used.
2. The communication format is a bit length of 8 bits, one stop bit, and no parity.
3. In the reception operation, the DTC is started by a receive data full interrupt request, and the receive data is transferred from the receive data register (RDR) of the SCI to a pre-specified transfer destination.
4. After the specified number of transfers complete, preparation is made for the next receive operation.

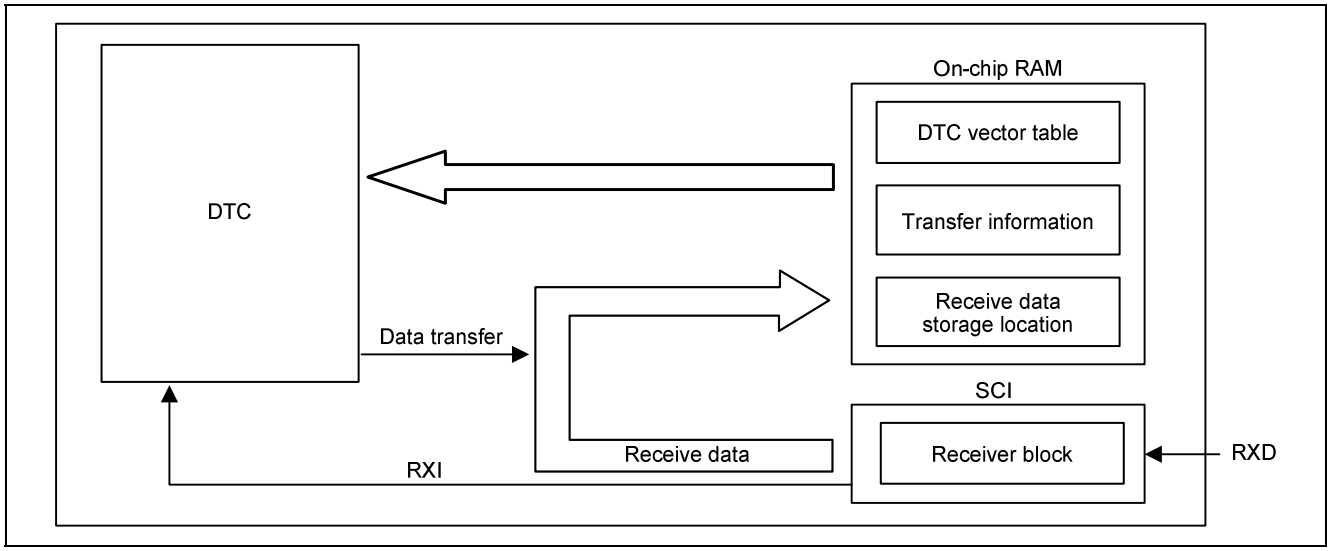

Figure 1 Overview of Asynchronous Serial Data Reception Using DTC

Functions Used

Serial communication interface (SCI)

Data transfer controller (DTC)

2. Description of Functions

In the sample program, the receive data full interrupt (RXI) source of the SCI is used to activate the DTC. Data transfer is performed in the specified transfer mode, resulting in asynchronous serial data reception.

2.1 Operation of Serial Communication Interface (SCI)

When the SCI operates in asynchronous mode, serial communication is accomplished by transmitting and receiving characters, each of which contains a start bit indicating the start of the transfer, a stop bit or bits indicating the end of the transfer, and data bits. Synchronization is by character unit. The transmitter block and receiver block each have a double-buffered structure, allowing data to be read and written during transmission and reception.

The communication line is normally held in the mark state (high level) during asynchronous serial communication. The SCI monitors the communications line, and when it detects a space state (low level) it treats it as a start bit and starts serial communication.

In serial communication, one character comprises a start bit (low level), data bits (LSB-first: starting from the lowest-order bit), a parity bit (high/low), and a stop bit or bits, in that order.

For details of the SCI, see the section Serial Communication Interface (SCI) in the *RX610 Group Hardware Manual*.

Table 1 provides an overview of asynchronous serial communication and figure 2 shows the data format used.

Table 1 Overview of Asynchronous Serial Communication

Item	Description
Channels	7 channels (SCI0 to SCI6)
Transfer speed	On-chip baud rate generator allowing setting of any bit rate
Clock sources	Internal clock: PCLK, PCLK/4, PCLK/16, PCLK/64 (PCLK: peripheral module clock) External clock: Clock input on SCKn pin
Data formats	Transfer data length: 7 bits/8 bits Transmit stop bits: 1 bit/2 bits Parity function: Even parity/odd parity/no parity Transfer order: LSB first/MSB first
Baud rates	Internal clock selected: 100 bps to 1,562,500 bps (PCLK = 50 MHz) External clock selected: Max. 781,250 bps (PCLK = 50 MHz)
Error detection	Parity error, overrun error, framing error
Interrupt requests	Transmit data empty interrupt (TXI) Receive data full interrupt (RXI) Receive error interrupt (ERI) Transmit error interrupt (TEI)
Clock source selection	Selectable between internal clock and external clock

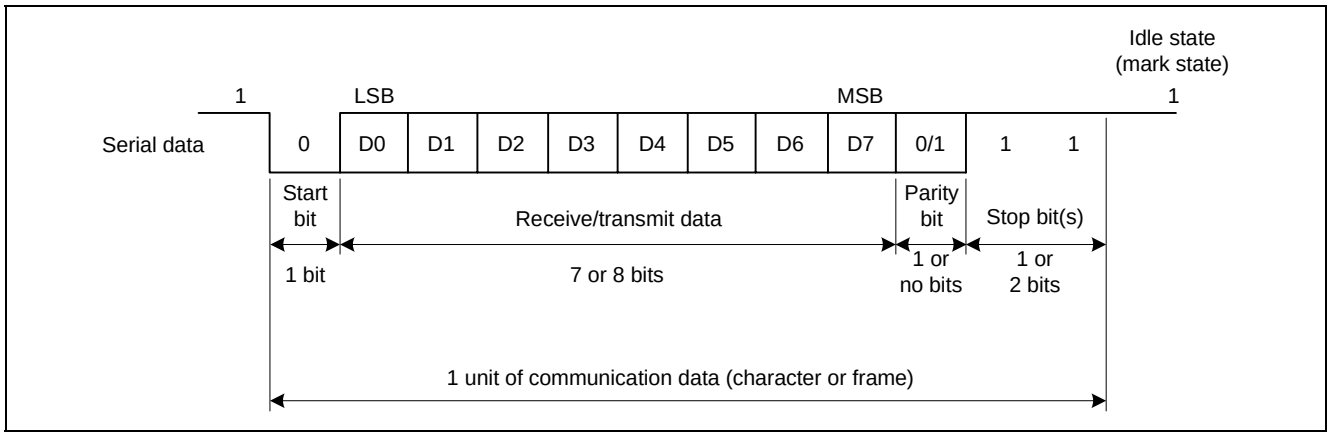

Figure 2 Asynchronous Serial Communication Data Format (8 Data Bits/Parity/2 Stop Bits)

Figure 3 is a block diagram of the SCI (SCI0 to SCI4). The registers are described below.

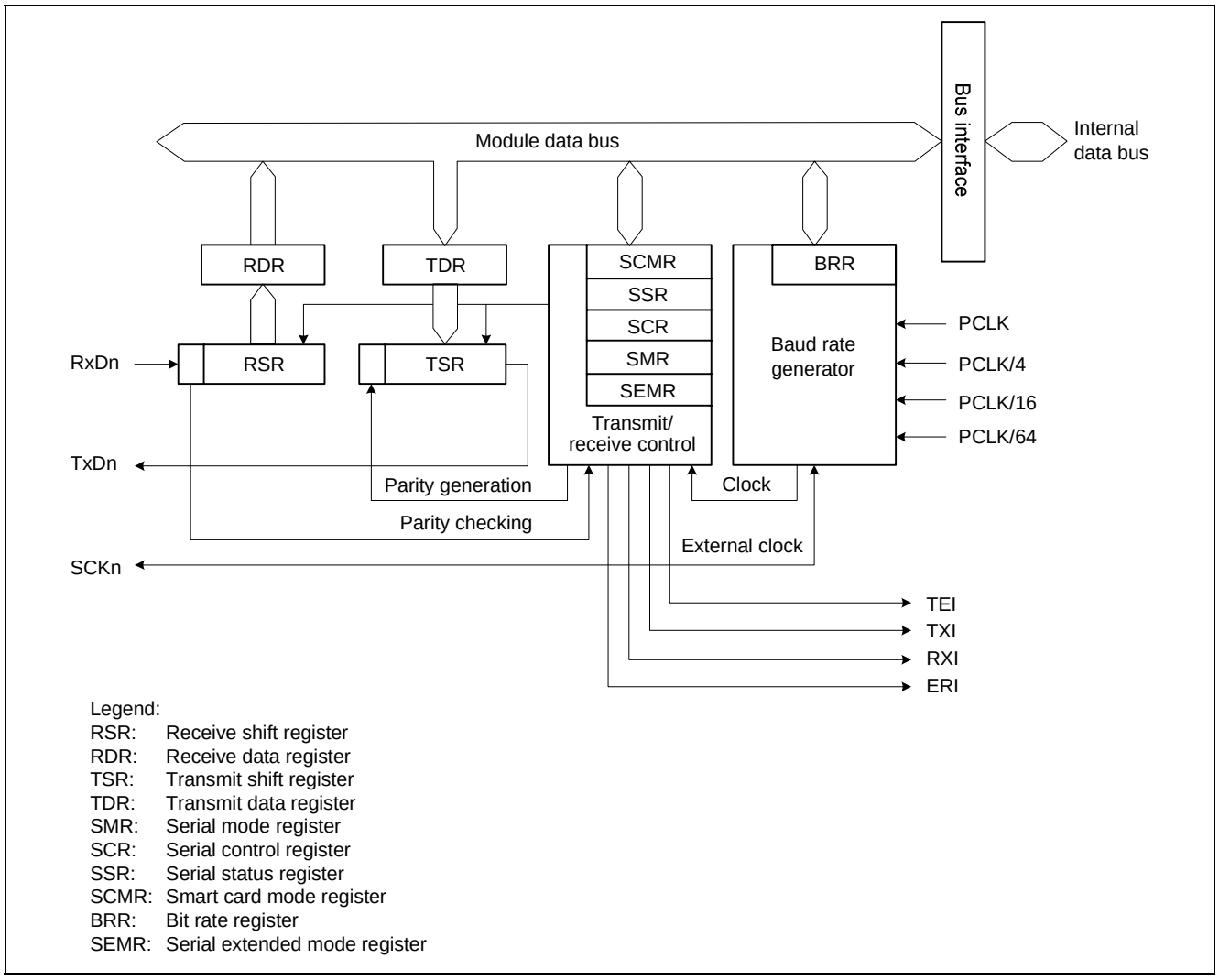

Figure 3 Block diagram of SCI (SCI0 to SCI4)

- Receive shift register (RSR)
  RSR is a shift register that converts to parallel data serial data input to the RxDn pin. When one frame of data has been received, it is transferred to RDR automatically.

- Receive data register (RDR)
  RDR is a register that stores receive data. When the SCI has received one frame of data, it transfers the receive data from RSR to RDR, allowing RSR to receive the next frame of data. RSR and RDR form a double-buffered structure, so continuous receive operations can be performed. Read RDR only once after a receive data full interrupt (RXI) request occurs. Note that an overrun error occurs if the next frame of data is received before the receive data in RDR is read. RDR cannot be written to by the CPU.

- Transmit data register (TDR)
  TDR is an 8-bit register that stores transmit data. When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission. TDR and TSR form a double-buffered structure, so continuous transmit operations can be performed. If after a frame of data is transmitted the next frame of transmit data has already been written to TDR, the SCI transfers it to TSR to continue transmission. The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each transmit data empty interrupt (TXI) request.

- Transmit shift register (TSR)
  TSR is a shift register for transmitting serial data. To perform serial data transmission, transmit data written to TDR is automatically transferred to TSR and then sent to the TxDn pin. TSR cannot be accessed directly by the CPU.

- Serial mode register (SMR)
  SMR is used to select the communication format and the clock source of the on-chip baud rate generator.

- Serial control register (SCR)
  SCR is used to select settings for transmit/receive control, interrupt control, and transmit/receive clock sources. For information on interrupts, see the Interrupt Control Unit (ICU) section in the *RX610 Group Hardware Manual*.

- Serial status register (SSR)
  SSR contains status flags for the SCI.

- Bit rate register (BRR)
  BRR is a register used to adjust the bit rate. The SCI performs baud rate generator control independently for each channel, different bit rates can be set for each channel.

- Serial extended mode register (SEMR)
  SEMR is a register used to select the clock for a 1-bit period in asynchronous mode.

- Smart card mode register (SCMR)
  SCMR is a register used to select the smart card interface mode and its format.

2.2 Operation of Data Transfer Controller (DTC)

The DTC is activated by an interrupt request, enabling it to perform data transfer. There are three transfer modes: normal transfer mode, repeat transfer mode, and block transfer mode. By storing the transfer information in a data area, data transfer can be performed using a user-defined number of channels. When the DTC is activated, the transfer information is read from a start address, according to the vector address determined for the individual DTC activation source, the user-defined transfer information is transferred to the DTC, and data transfer takes place. When data transfer finishes, write-back of the contents of the various registers takes place. For details of the DTC, see the Data Transfer Controller (DTC) section in the *RX610 Group Hardware Manual*. Table 2 presents an overview of the DTC.

Table 2 Overview of DTC

Item	Description
Transfer modes	Normal transfer mode Repeat transfer mode Block transfer mode
Transfer using user-defined number of channels	Data transfer using multiple channels is possible using a single activation source (chain transfer). Chain transfer execution can be specified following data transfer.
Short-address mode/ full-address mode	• The transfer information comprises three longwords in short-address mode and four longwords in full-address mode. • In short-address mode, the transfer source and transfer destination addresses are specified as 24-bit addresses, allowing direct addressing of a 16 MB address space. • In full-address mode, the transfer source and transfer destination addresses are specified as 32-bit addresses, allowing direct addressing of a 4 GB address space.
Data sizes	Byte, word, or longword can be specified.
Interrupt sources	• An interrupt request is issued to the CPU after a single data transfer finishes. • An interrupt request is issued to the CPU after the specified number of data transfers finish.
Read skip	• Reading of the transfer information can be omitted (read skip).
Write-back skip	• Write-back of transfer source addresses or transfer destination addresses for which fixed values have been chosen can be omitted (write-back skip).

Figure 4 is a block diagram of the DTC.

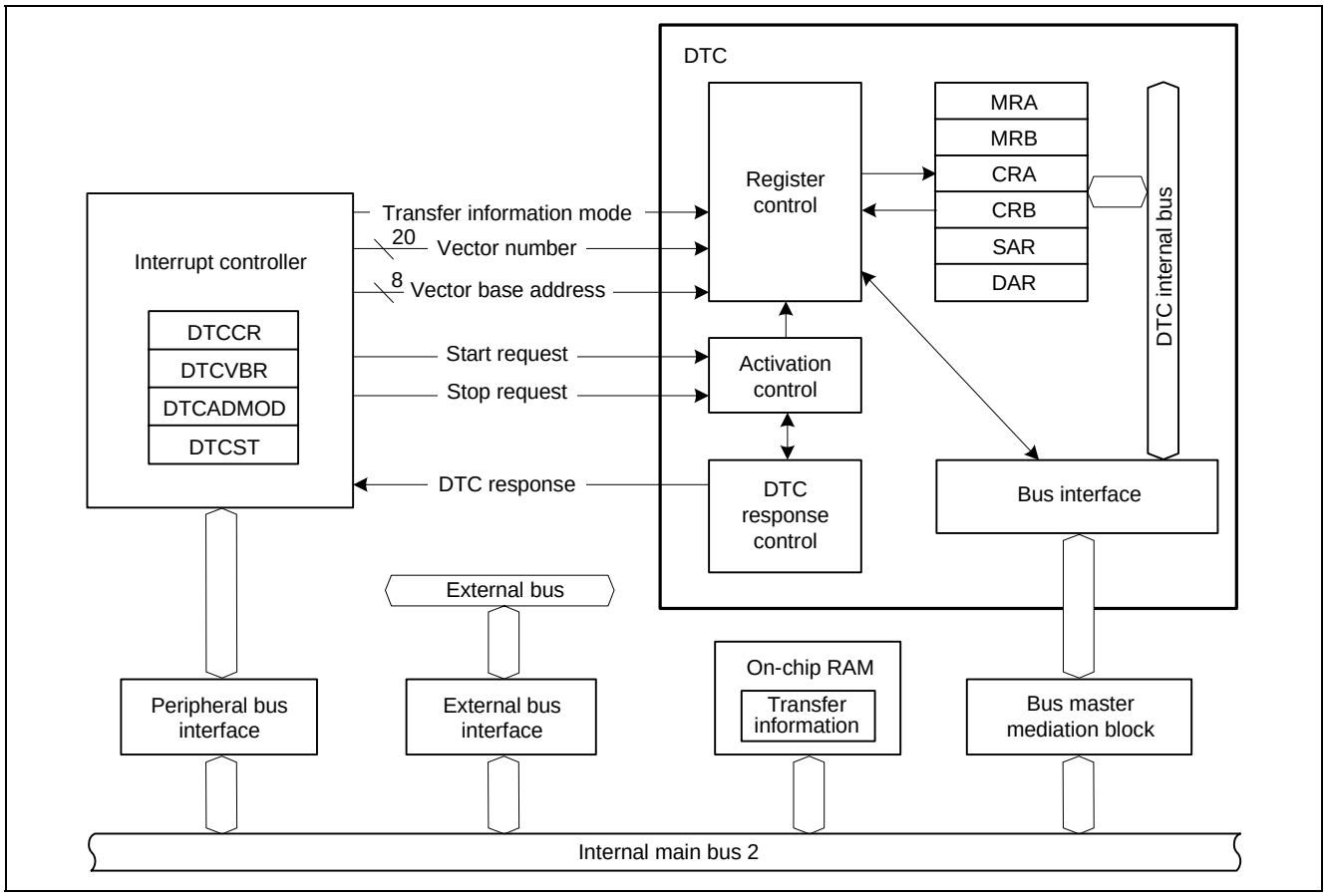

Figure 4 Block Diagram of DTC

- DTC mode register A (MRA)
  MRA is used to select the operating mode of the DTC. It cannot be accessed directly by the CPU.
- DTC mode register B (MRB)
  MRB is used to select the operating mode of the DTC. It cannot be accessed directly by the CPU.
- DTC transfer count register A (CRA)
  CRA is used to specify the number of data transfers to be performed by the DTC. It cannot be accessed directly by the CPU.
- DTC transfer count register B (CRB)
  CRB is used to specify the number of block data transfers to be performed by the DTC in block transfer mode. It cannot be accessed directly by the CPU.
- DTC source address register (SAR)
  SAR is used to specify the transfer source start address for data transfer by the DTC. It cannot be accessed directly by the CPU.
- DTC destination address register (DAR)
  DAR is used to specify the transfer destination start address for data transfer by the DTC. It cannot be accessed directly by the CPU.
- DTC control register (DTCCR)
  DTCCR is used to select DTC control settings.
- DTC vector base register (DTCVBR)
  DTCVBR is used to specify the base address for calculating the DTC vector table addresses.
- DTC address mode register (DTCADMOD)
  DTCADMOD is used to specify the areas that can be accessed by the DTC.
- DTC module start register (DTCST)
  DTCST is used to start and stop the DTC module.

2.2.1 Allocation of Transfer Information

Transfer information should be allocated in memory according to the endian specification as shown in figure 5.

When writing CRA and CRB setting data in 16-bit format, write the CRA setting data to low-order address 0 and the CRB setting data to low-order address 2 for big endian, and write the CRB setting data to low-order address 0 and the CRA setting data to low-order address 2 for little endian. When writing setting data in 32-bit format, write the CRA setting data to the MSB side and the CRB setting data to the LSB side of the 32-bit space at low-order address 0, regardless of the endian specification.

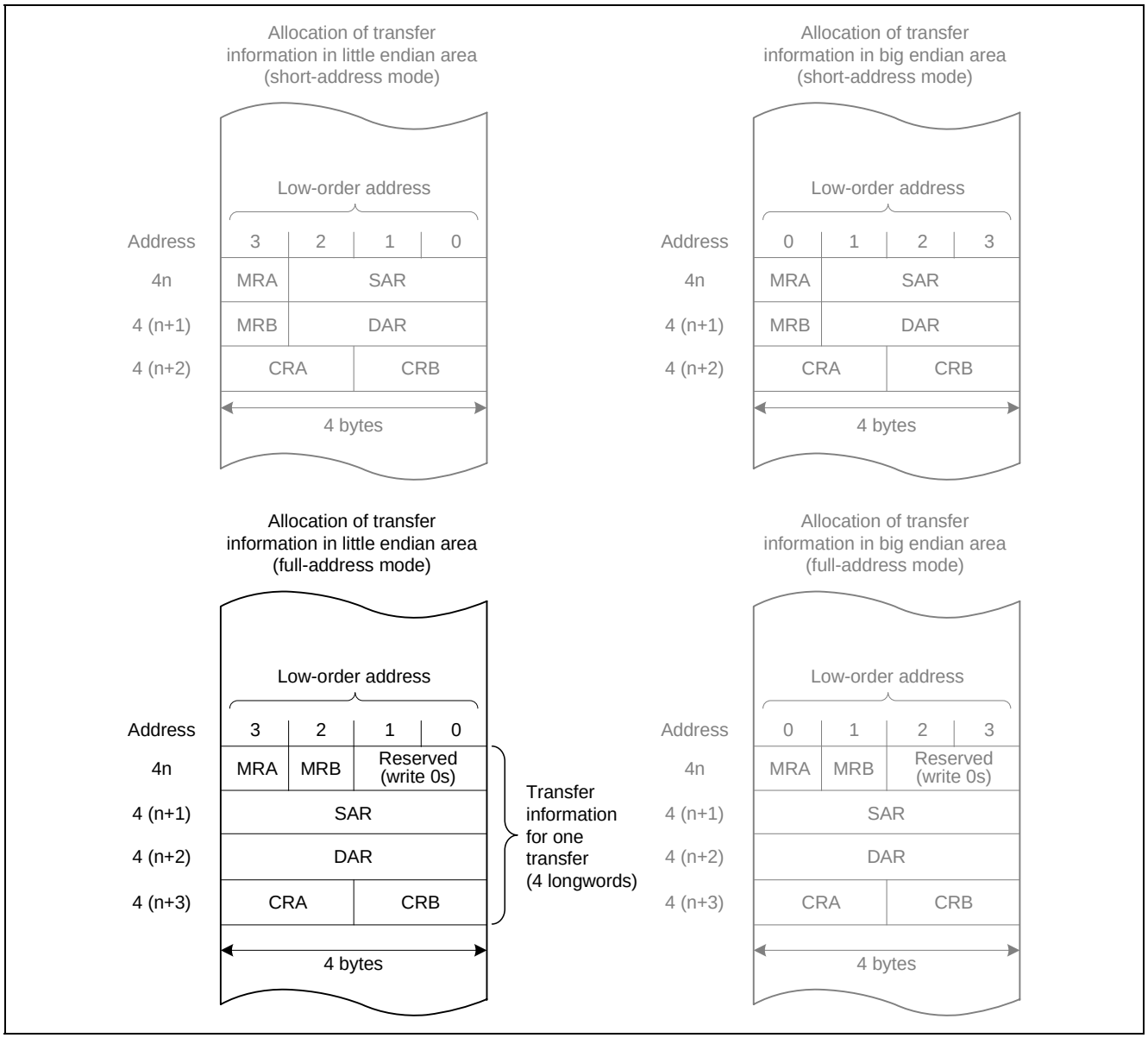

Figure 5 Allocation of Transfer Information

2.2.2 DTC Vector Table

For each activation source, the DTC reads the start address of the transfer information from a vector table and then reads the transfer information from this start address. Figure 6 shows the correspondence between the DTC vector table and the transfer information.

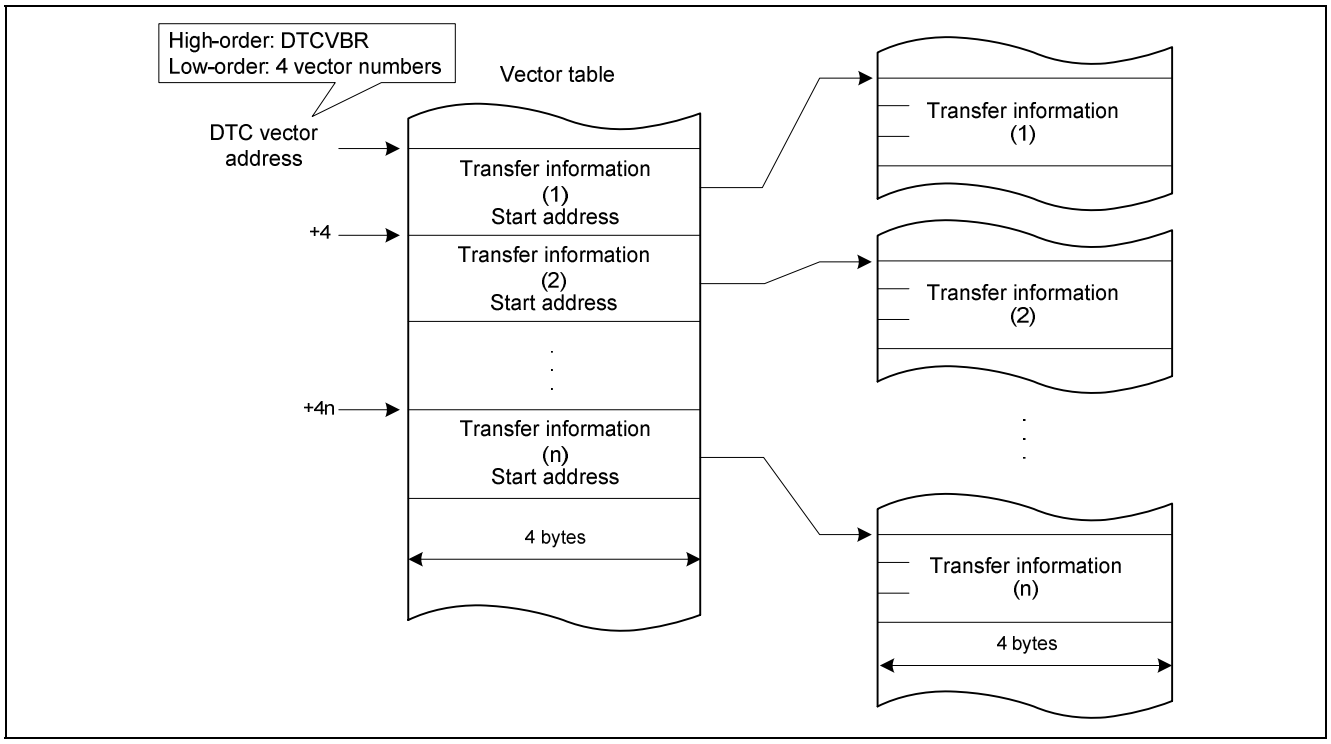

Figure 6 Correspondence Between DTC Vector Table and Transfer Information

2.2.3 Switching the Endian Specification

The RX610 Group supports two ways of arranging byte data: big endian, in which the highest-order byte is located at address 0, and little endian, in which the lowest-order byte is located at address 0. Switching between endian specifications is done by setting the mode pin (MDE) level at a power-on reset. Little endian is selected when the MDE pin is low-level, and big endian is selected when the MDE pin is high-level, at a power-on reset. The access operation differs depending on whether 8-, 16-, or 32-bit access is selected by an instruction and according to the little endian or big endian setting. For details on endian specifications, see the CPU (Endian) section in the *RX610 Group Hardware Manual*.

The sample program presented in this application note uses little endian operation. Therefore, the MDE should be driven low level to select the little endian setting.

3. Operation

Table 3 lists the settings conditions for the SCI communication function, and table 4 the DTC transfer conditions, used by the sample program. Figure 7 shows the operation timing.

Table 3 SCI Settings Conditions

Channel used	SCI1
Communication mode	Asynchronous mode
Interrupts	Receive data full interrupt (RXI) Receive error interrupt (ERI)
Communication speed	38,400 bps (PCLK = 50 MHz)
Data length	8 bits
Stop bits	1 stop bit
Parity	None

Table 4 DTC Transfer Conditions

Conditions	Transfer conditions of SCI reception-side DTC (RXI1)
Transfer information	Full-address mode
Transfer mode	Normal mode
Number of transfers	256 times
Transfer data	Size: Byte Data contents: Any 256 bytes
Transfer source	Receive data register (SCI1.RDR)
Transfer destination	On-chip RAM
Transfer source address	Transfer source is fixed.
Transfer destination address	Transfer destination address is incremented after each transfer.
Activation source	SCI receive data full interrupt
Interrupt	Interrupt to CPU enabled after specified data transfer finishes.

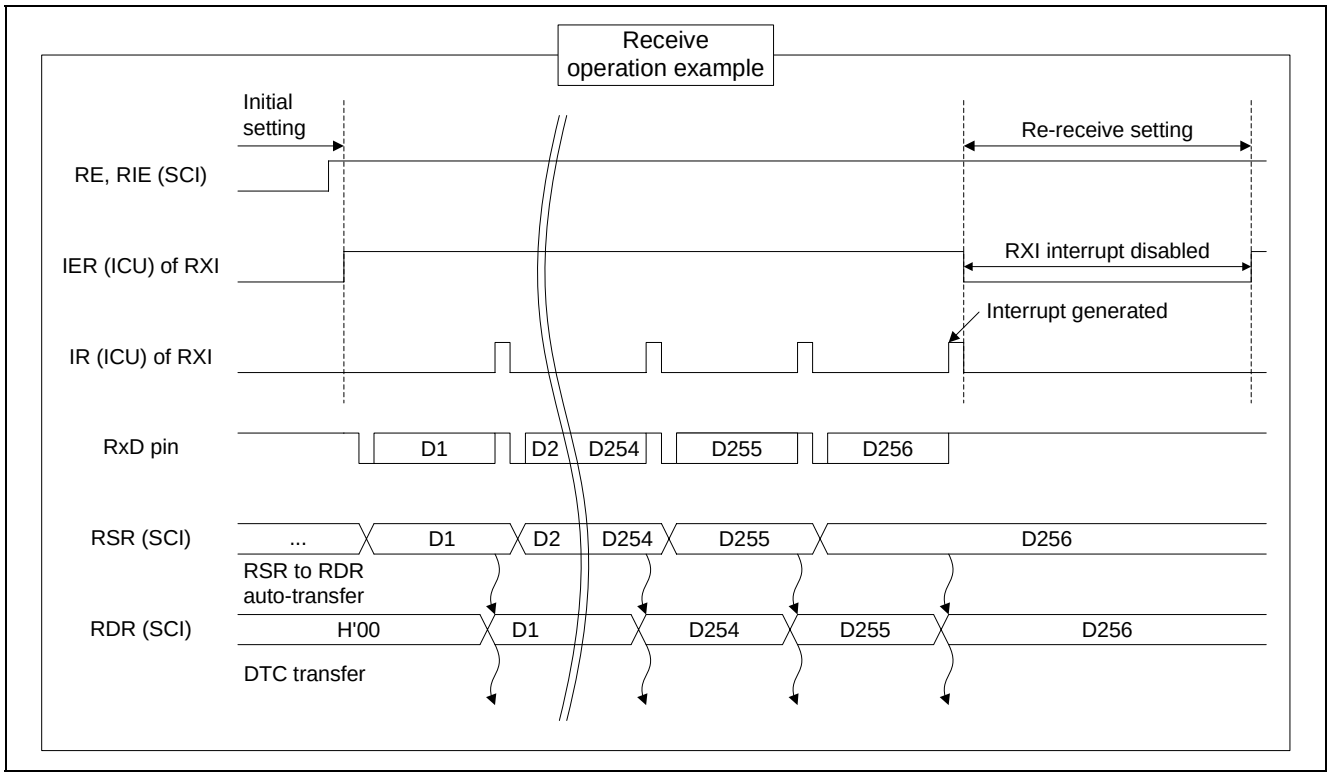

Figure 7 Operation Timing*

Note: Note: Care is required when the DTC module is used for reception operations. If the next transfer request occurs before the IR flag has been cleared automatically, the transfer request may be lost. For more information, see the article "Notes on DMAC/DTC Transfer Using the RX610 Group Communications Functions" under Technical Updates on the Renesas Electronics Corporation web site.

4. Software

4.1 List of Functions

Table 5 is a list of the functions used by the sample program.

Table 5 List of Functions

Function	Description
HardwareSetup	Initialization processing, clock setting, cancelling of module stop state
main	Main process
icu_init	Initial setting of ICU, interrupt level setting
sci_init	Initial setting of SCI, transfer clock setting
dtc_init	Initial setting of DTC, transfer information setting, DTC vector base register setting, DTC start enable
int_sci_rxi1	Receive interrupt
int_sci_eri1	Receive error interrupt

4.2 Variables Used

Table 6 lists the variables used by the sample program.

Table 6 List of Variables

Variable, Label	Description
recvBuf[256]	Array variable for storing serial receive data
dtc_rx	Structure variable for storing DTC transfer information for SCI reception
*dtc_table[256]	DTC vector table used to assign dtc_rx address in DTC transfer information

4.3 Processing Sequence

Figures 8 to 14 show the processing sequence of the sample program.

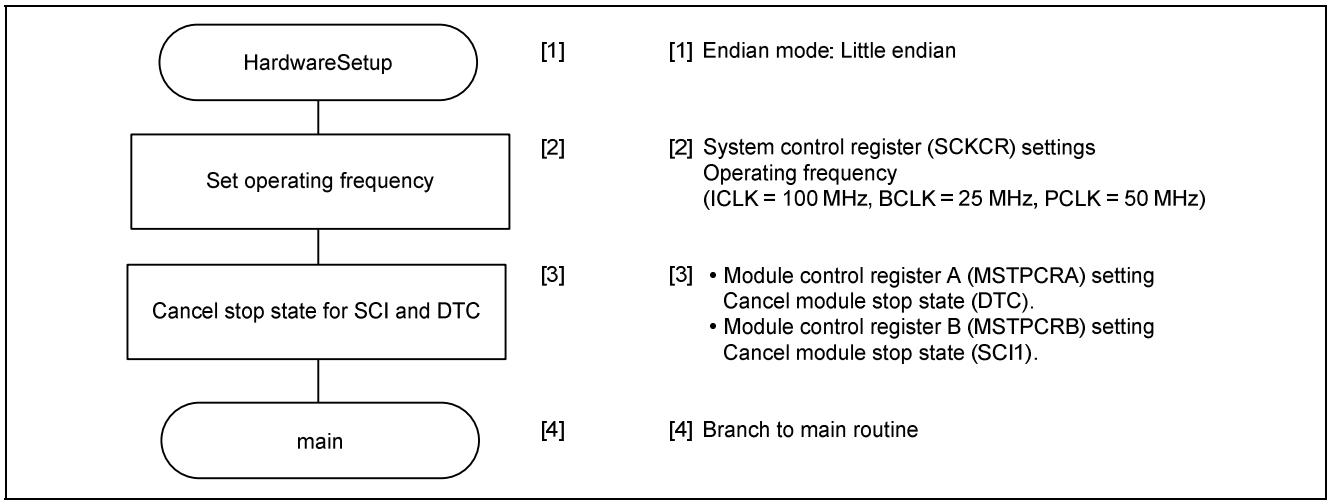

Figure 8 Initialization Processing

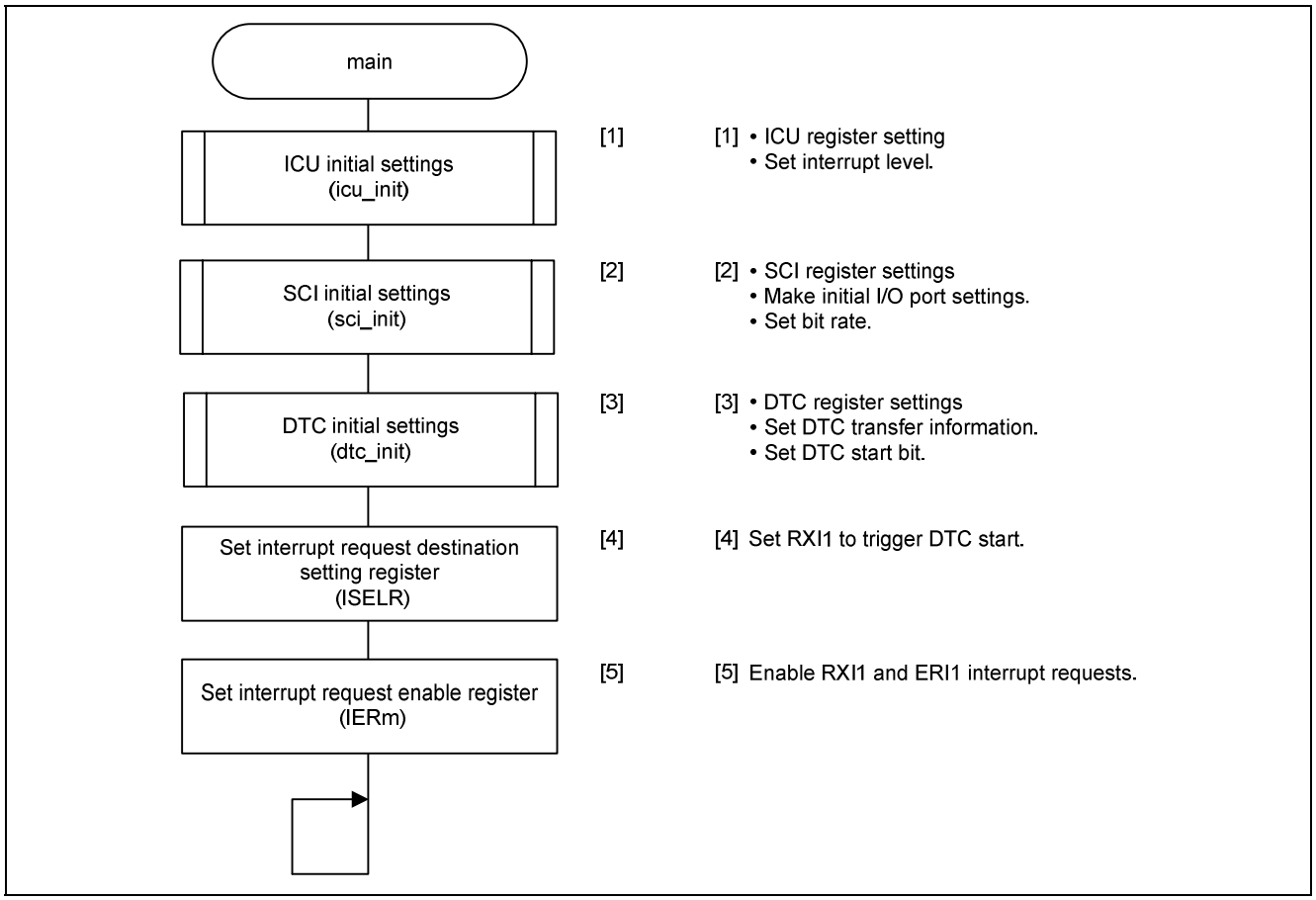

Figure 9 Main Process

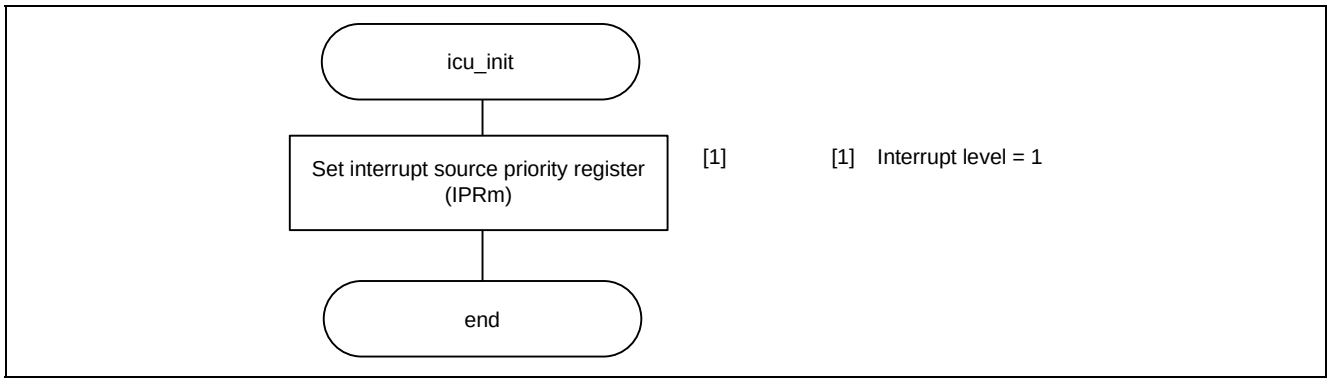

Figure 10 ICU Initial Setting

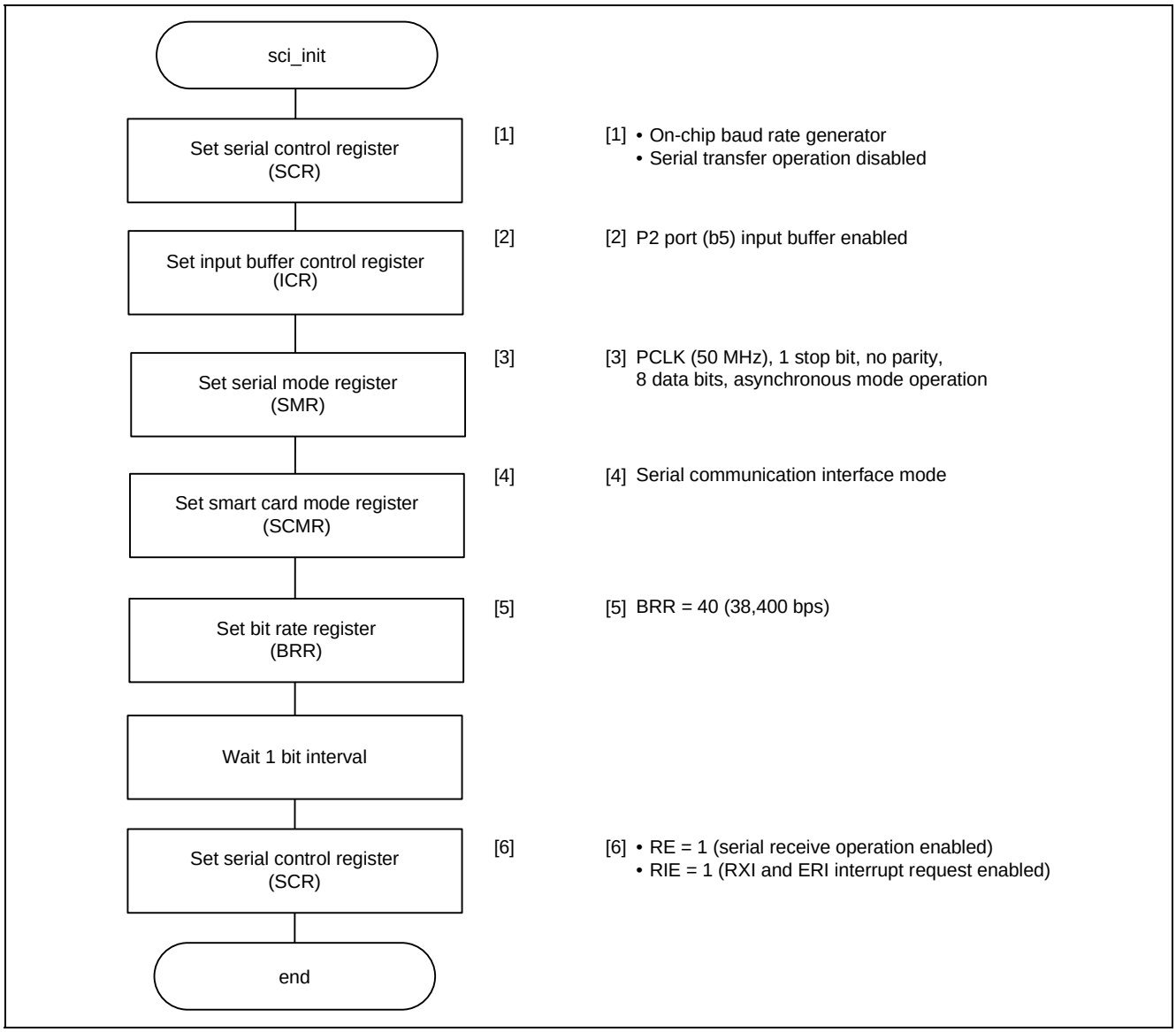

Figure 11 SCI Initial Settings

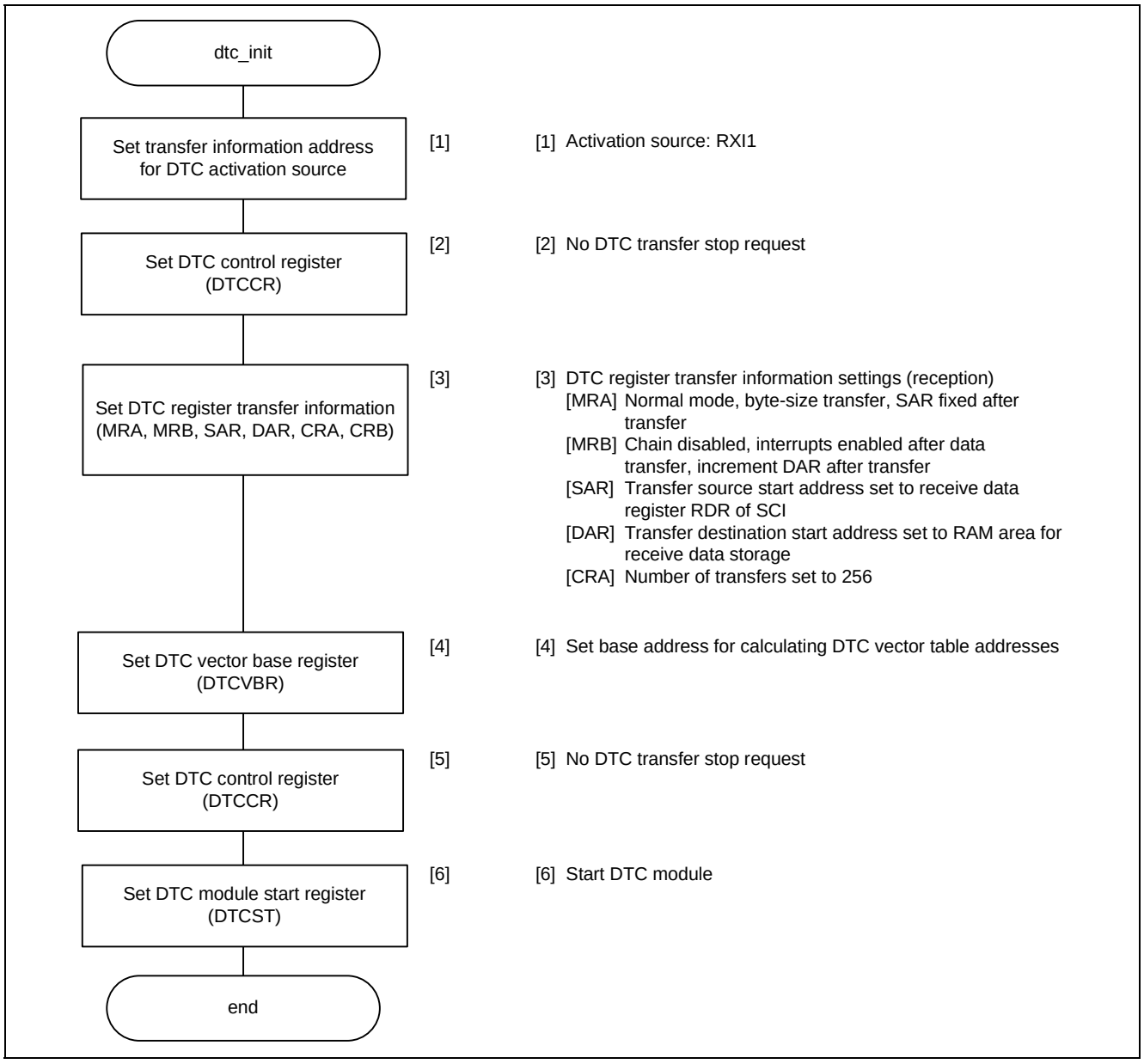

Figure 12 DTC Initial Settings

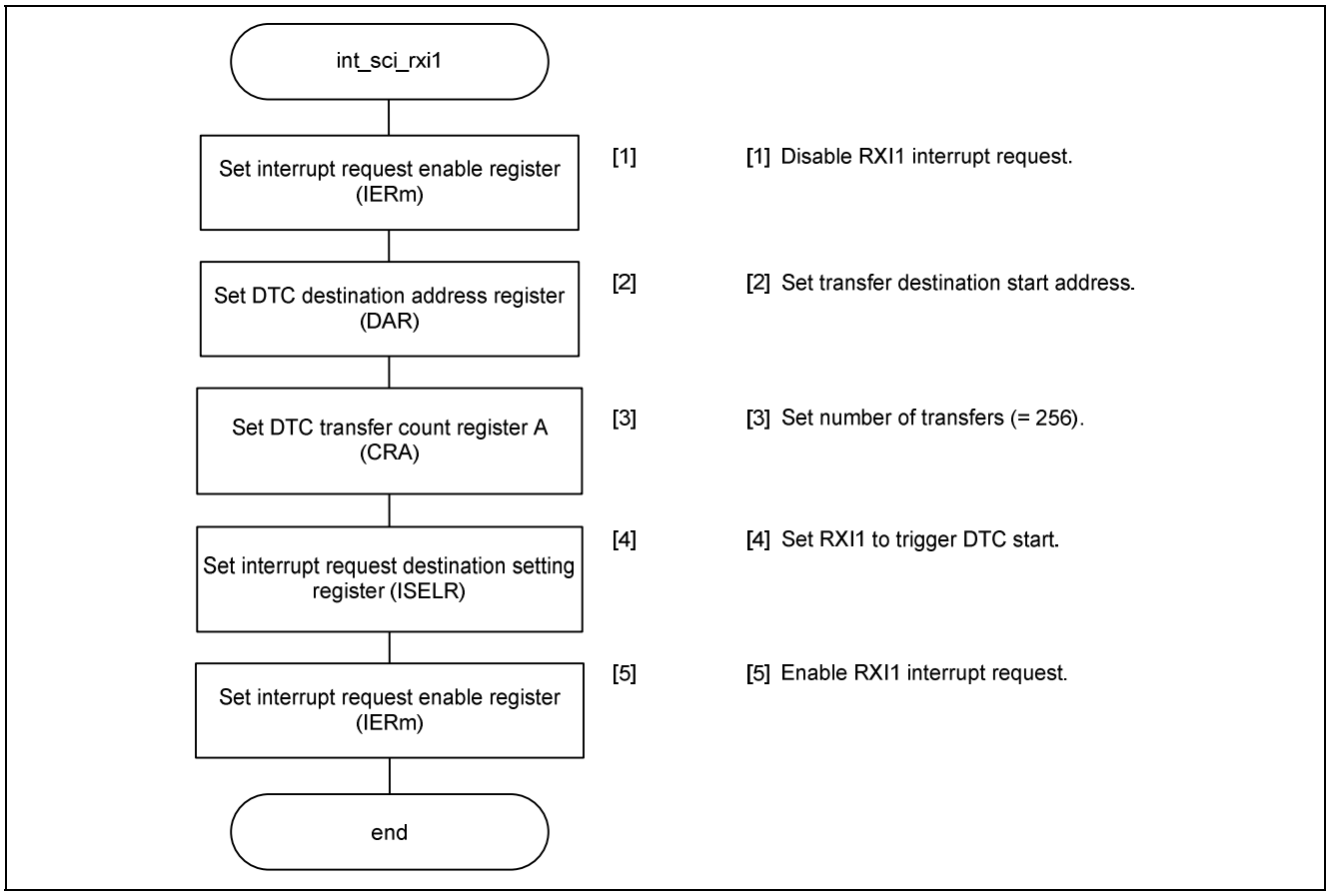

Figure 13 Receive Interrupt Handler

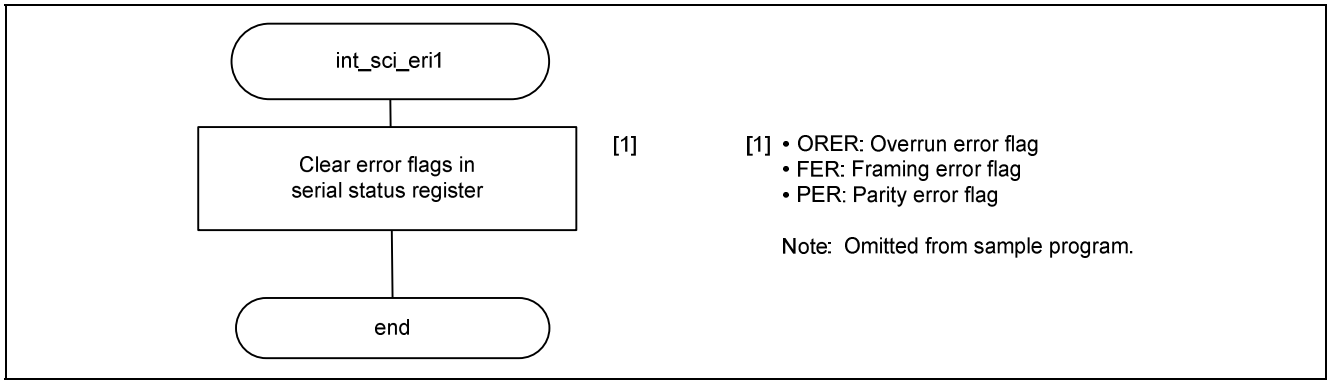

Figure 14 Receive Error Interrupt

5. Verified Operation Environment

Table 7 shows the environment in which operation of the sample program has been verified.

Table 7 Verified Operation Environment

Item	Name
Device	RX610 (R5F56108VNFP)
Board	Evaluation board
Power supply voltage	5.0 V (CPU operating voltage is 3.3 V)
Input clock	12.5 MHz (ICLK = 100 MHz, PCLK = 50 MHz, BCLK = 25 MHz)
Operating temperature	Room temperature
HEW	Version 4.07.00.007
Toolchain	RX Standard Toolchain (V.1.0.0.0) RX Family C/C++ Compile Driver V.1.00.00.001 RX Family C/C++ Compiler V.1.00.00.001 RX Family Assembler V.1.00.00.001 Optimizing Linkage Editor V.10.00.00.001 RX Family C/C++ Standard Library Generator V.1.00.00.001
Debugger	RX E20 SYSTEM V.1.00.00.000

6. Reference Documents

- Hardware Manual
  RX610 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Development Environment Manual
  RX Family C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.09.10	—	First edition issued

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1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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