RX Family

Sample Program to use DTC module for sequence transfer Firmware Integration Technology

R01AN3434EJ0100
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Introduction

This application note explains the sequence transfer applications using RX Family DTC module Firmware Integration Technology (FIT) and RX Code Generator (CG).

This application note has achieved “RX65N Group and RX651 Group DTCb sequence transfer Examples (R01AN3092EJ)” by DTC FIT module and CG. Refer to R01AN3092EJ for the basic function and the contents of the sequence transfer.

Target Device

RX65N Group, RX651 Group

When applying the information in this application note to a microcontroller other than the above, modifications should be made as appropriate to match the specification of the microcontroller and careful evaluation performed.

FIT-Related Documents

- RX65N Group and RX651 Group DTCb sequence transfer Examples (R01AN3092EJ)
- RX Family DTC Module Using Firmware Integration Technology (R01AN1819EJ)
- Firmware Integration Technology User’s Manual (R01AN1833EU)
- Board Support Package Module Using Firmware Integration Technology (R01AN1685EJ)
- Adding Firmware Integration Technology Modules to Projects (R01AN1723EU)
- Adding Firmware Integration Technology Modules to CS+ Projects (R01AN1826EJ)

Contents

1. Changes in the Application Note

This application note has achieved RX65N Group and RX651 Group DTCb Sequence Transfer Examples (R01AN3092EJ) by DTC FIT module and CG. Table 1-1 lists the changes in the application note. For the items not included in this application note, refer to R01AN3092EJ.

Table 1-1 Changes in the Application Note

	R01AN3092	R01AN3434 (This Application Note)	
Chapter	**Items**	**Corresponding chapter**	**Remarks**
1.	Basic Operation of Sequence transfer	None	Refer to R01AN3092EJ
2.	Specifications	2	Refer to R01AN3092EJ for “DTC Index Table Settings”
3.	Operation Confirmation Conditions	2.1	
4.	Related Applications	First page	
5.	Hardware Description	3	
6.	Software Description	4	
6.1	Operation Overview	None	Refer to R01AN3092EJ
6.2	Section Configuration	None	In the case of the DTC FIT module, there is no section setting description to secure the DTC vector table area using the malloc () function.
6.3	File Structure	4.3	
6.4	Option Setting Memory	None	Set the initial value (0xFFFFFFFF) in the CG
6.5	Constants List	4.5	
6.6	Struct/Union List	4.6	
6.7	Variables List	4.7	
6.8	Functions List	4.8	
6.9	Functions Specification	4.9	
6.10	Flow Chart	4.10	

2. Overview

This application note describes the asynchronous serial receiving by sequence transfer based on the receive FIFO full interrupt (RXI) as DTC activation source. The SCI used is channel 10.

The following sequence transfer is automatically started according to 1 byte data (sqnum) received first from external communication device.

- Sequence Transfer Example 1 (sqnum= “00h”) :
  Changes receive FIFO threshold to 4 bytes, receives 4 bytes data, and executes DTC transfer.
- Sequence Transfer Example 2(sqnum= ”01h”):
  Changes receive FIFO threshold to 8 bytes, receives 8 bytes data, and executes DTC transfer.
- Sequence Transfer Example 3(sqnum= “02h”):
  Changes receive FIFO threshold to 12 bytes, receives 12 byte data, and executes DTC transfer.
- Sequence Transfer Example 4(sqnum= “03h”):
  Changes receive FIFO threshold to 16 bytes, receives 16 bytes data, and executes DTC transfer.
- Sequence Transfer Example 5(sqnum>= “04h”):
  Process as invalid command.

2.1 Operating Environment

Table 2-1 lists the operation confirmation conditions.

Table 2-1 Operation Confirmation Conditions

Items	Contents
MCU used	RX65N Group (Program ROM 1MB/RAM 256KB)
Operating frequency	ICLK: 120MHz, PCLKA : 120MHz
Operating voltage	3.3V
Integrated development Environment	Renesas Electronics e2 studio V6.0.0
C compiler	Renesas Electronics C/C++ compiler for RX family V.2.07.00
	Compile Option: Add the following option to IDE default settings; -lang = c99
Endian order	Big endian/ Little endian
Software version	Ver.1.00
Board used	Renesas Starter Kit for RX65N (product No.: RTK500565NSxxxxxBE) Renesas Starter Kit for RX65N-2MB (product No.: RTK50565N2SxxxxxBE)

3. Hardware Description

Using the MCU's internal SCI, asynchronous serial receive with external communication device is performed.

3.1 Example of Hardware Configuration

Figure 3-1 shows the connection diagram.

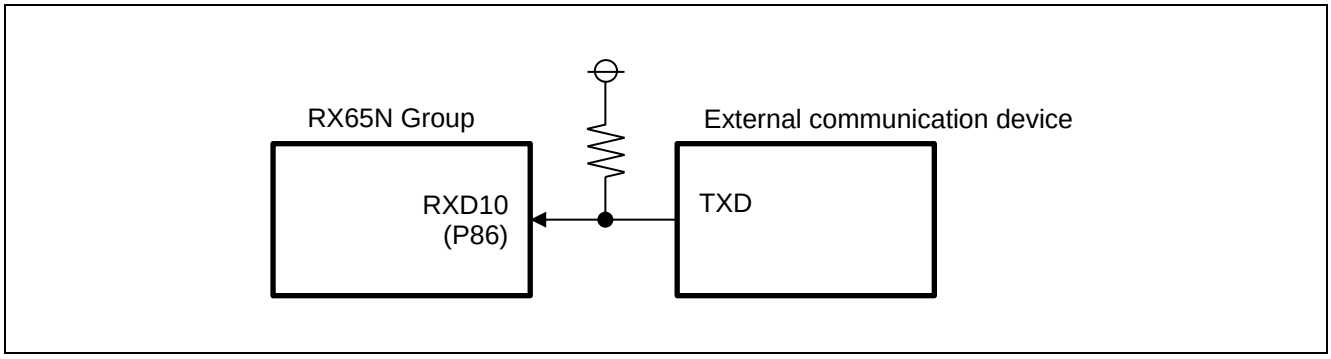

Figure 3-1 Connection Diagram

3.2 List of Pins Used

Table 3-1 lists the pins used and the functions.

Table 3-1 Pins Used and the Functions

Pin name	I/O	Contents
RXD10	Input	Input SCI10 receive data

4. Software Description

Initial setting for SCI10 and DTC is made after releasing the reset. Then, RX110 for DTC activation source is set. The following sequence transfers are automatically executed according to 1 byte data (sqnum) received first from external communication device. For operation details, refer to “RX65N Group and RX651 Group DTCb Sequence Transfer Examples (R01AN3092EJ)”.

- Sequence Transfer Example 1(sqnum=“00h”)

After receiving sqnum= ”00h” from external communication device, the receive FIFO threshold is changed to 4 bytes, then, 4 bytes data output from external communication device is received, and is stored in the RAM by DTC transfer.

- Sequence Transfer Example 2(sqnum=“01h”)

After receiving sqnum= ”01h” from external communication device, the receive FIFO threshold is changed to 8 bytes, then, 8 bytes data output from external communication device is received, and is stored in the RAM by DTC transfer.

- Sequence Transfer Example 3(sqnum=“02h”)

After receiving sqnum= ”02h” from external communication device, the receive FIFO threshold is changed to 12 bytes, then, 12 bytes data output from external communication device is received, and is stored in the RAM by DTC transfer.

- Sequence Transfer Example 4(sqnum=“03h”)

After receiving sqnum= “03h” from external communication device, the receive FIFO threshold is changed to 16 bytes, then, 16 bytes data output from external communication device is received, and is stored in the RAM by DTC transfer.

- Sequence Transfer Example 5(sqnum>=“04h”)

When receiving sqnum>= “04h”, it is determined as invalid command and generates interrupt request to CPU without sequence transfer.

In sequence transfer examples 1~4, interrupt request to CPU is not generated.

4.1 Peripherals Settings

The setting for the peripherals used is as follows;

Table 4-1 DTC Settings

Items	Settings
DTC activation source	Receive FIFO full receive (RXI10)
DTC address mode	Full address mode

Table 4-2 SCI Settings

Items	Settings
Channel using SCI	Channel 10
Communication mode	Asynchronous
Transfer speed	38400bps
Transmit/receive operation	Receive
Clock source	Internal baud rate generator
¥ data length	8 bits
Stop bit	2 bits (when receiving SCI, regardless of SMR.STOP bit setting, only 1st bit of the stop bit is checked. When 2nd bit is ”0”, it is regarded as the start bit of the next send frame)
Parity function	No parity
Data transfer direction	LSB first
Receive FIFO threshold	Variable
Interrupt	Enable receive FITO full interrupt (RXI10) Enable receive error interrupt (ERI10)

4.2 Software Configuration

Figure 4-1 shows the software configuration.

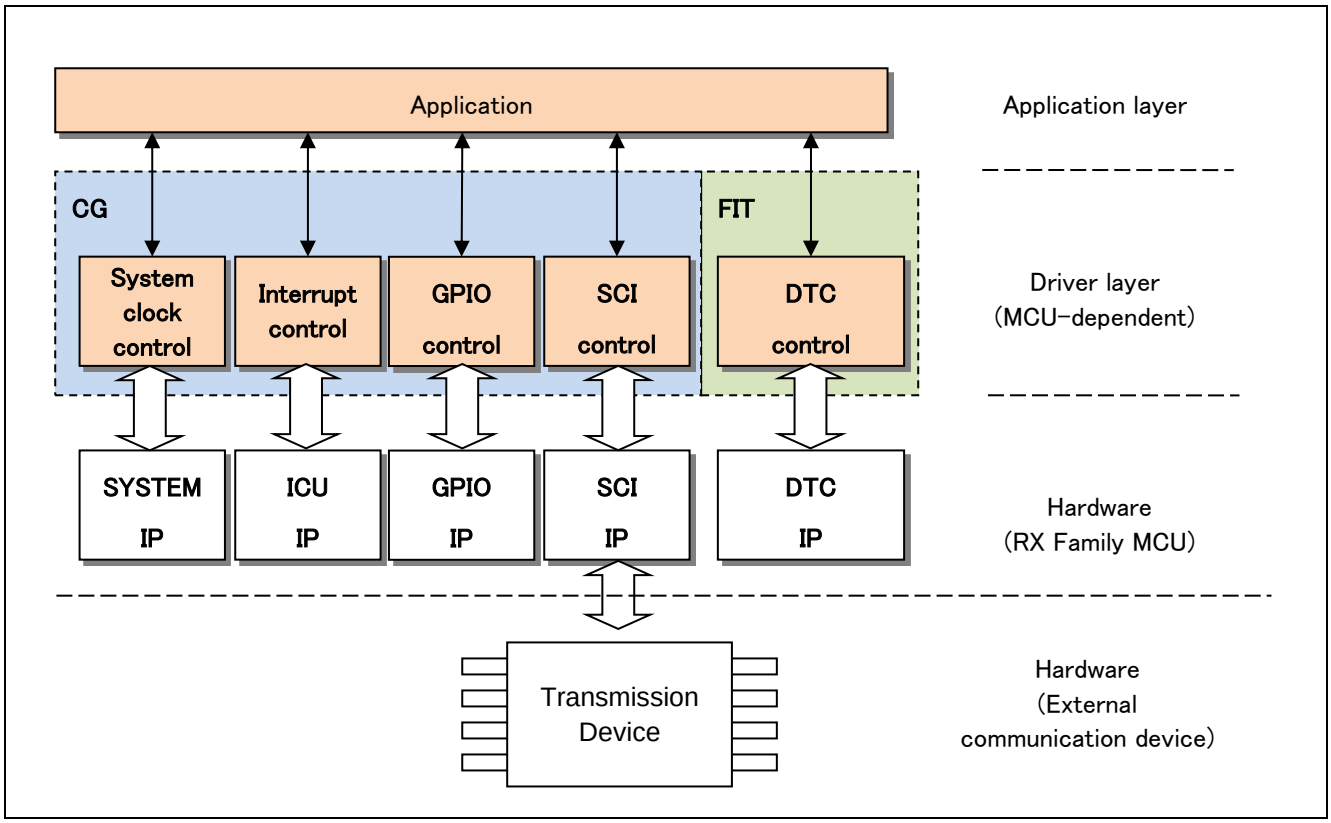

Figure 4-1 Software Configuration

(1) Application Layer (r_cg_main.c)

In this application note, application is configured based on r_cg_main.c output using RX64M CG.

(2) Driver Layer (CG control)

In this application note, the source code (r_cg_xxxx.c other than r_cg_main.c) output using RX64M CG is modified for use as RX65N.

(3) Driver Layer (FIT control)

This application note includes RX Family DTC module Firmware Integration Technology (R01AN1819EJ).
The latest version can be downloaded from the Renesas Electronics website.

4.3 File Structure

Table 4-3 lists the files used in the sample code. The files auto-generated in Integrated development environment (IDE) are not included.

Table 4-3 File structure

¥an-r01an3434ej0100-rx65n-dtc-dmac2	<DIR>	Sample project folder
¥r_config	<DIR>	FIT Module configuration fonder
r_dtc_rx_config.h		DTC FIT module configuration file
¥r_dtc_rx	<DIR>	DTC FIT module folder For the detail, refer to DTC FIT module application note.
¥src	<DIR>	CG and other file folders
iodefine.h		I/O register definition file
platform.c		FIT BSP module alternate source file
platform.h		FIT BSP module alternate header file
¥cg_src	<DIR>	CG folder
r_cg_cgc.c		CGC module source file
r_cg_cgc.h		CGC module header file
r_cg_cgc_user.c		CGC module user source file
r_cg_dbsct.c		Section definition source file
r_cg_hardware_setup.c		Hardware setup source file
r_cg_icu.c		ICU module source file
r_cg_icu.h		ICU module header file
r_cg_icu_user.c		ICU module user source file
r_cg_intprg.c		Interrupt definition source file
r_cg_macrodiver.h		CG macro definition header file
r_cg_main.c		Main source file (sample code)
r_cg_resetprg.c		Reset source file
r_cg_sbrk.c		Heap definition source file
r_cg_sbrk.h		Heap definition header file
r_cg_sci.c		SCI module source file
r_cg_sci.h		SCI module header file
r_cg_sci_user.h		SCI module user source file
r_cg_stacksct.h		Stack area definition header file
r_cg_userdfine.h		User definition header file
r_cg_vect.h		Vector table initialization header file
r_cg_vecttbl.c		Vector table initialization source file

4.4 Compile Settings

Table 4-4 lists the setting of DTC FIT module configuration file (r_dtc_rx_config.h).

Table 4-4 Compile settings

Configuration options in *r_dtc_rx_config.h*	
#define DTC_CFG_SHORT_ADDRESS_MODE *The default value is “DTC_DISABLE”	• DTC_DISABLE: Selects full address mode
#define DTC_CFG_TRANSFER_DATA_READ_SKIP_EN *The default value is “DTC_ENABLE”	• DTC_DISABLE: Disables transfer information read skip
#define DTC_CFG_USE_SEQUENCE_TRANSFER *The default value is "DTC_DISABLE”	• DTC_ENABLE: Uses sequence transfer. When defined as “DTC_ENABLE”, set DTC_CFG_SHORT_ADDRESS_MODE to “DTC_DISABLE”. When set to “DTC_ENABLE”, compiling error will be generated.

4.5 Constants List

Table 4-5 lists the constants used in r_cg_main (referred to as “sample code” below).

Table 4-5 Constants used in the sample code

Constants name	Settings	Description
SQNUM0_RCV_NUM	4	Receive data count for Sequence transfer example 1(sqnum=0)
SQNUM0_RCV_FIFO_TRG	4	Receive FIFO threshold for Sequence transfer example 1(sqnum=0)
SQNUM0_FCRH_DATA	0xF4	FCR.H register settings for Sequence transfer example 1(sqnum=0)
SQNUM0_INFO_NUM	3	Transfer information counts for Sequence transfer example 1(sqnum=0)
SQNUM1_RCV_NUM	8	Receive data count for Sequence Transfer Example 2(sqnum=1)
SQNUM1_RCV_FIFO_TRG	8	Receive FIFO threshold for Sequence Transfer Example 2(sqnum=1)
SQNUM1_FCRH_DATA	0xF8	FCR.H register settings for Sequence Transfer Example 2(sqnum=1)
SQNUM1_INFO_NUM	3	Transfer information counts for Sequence Transfer Example 2(sqnum=1)
SQNUM2_RCV_NUM	12	Receive data counts for Sequence Transfer Example 3(sqnum=2)
SQNUM2_RCV_FIFO_TRG	12	Receive FIFO threshold for Sequence Transfer Example 3(sqnum=2)
SQNUM2_FCRH_DATA	0xFC	FCR.H register settings for Sequence Transfer Example 3(sqnum=2)
SQNUM2_INFO_NUM	3	Transfer information counts for Sequence Transfer Example 3(sqnum=2)
SQNUM3_RCV_NUM	16	Receive data counts for Sequence Transfer Example 4(sqnum=3)
SQNUM3_RCV_FIFO_TRG	8	Receive FIFO threshold for Sequence Transfer Example 4(sqnum=3)
SQNUM3_FCRH_DATA	0xF8	FCR.H register settings for Sequence Transfer Example 4(sqnum=3)
SQNUM3_INFO_NUM	4	Transfer information counts for Sequence Transfer Example 4(sqnum=3)

4.6 Struct/Union List

None.

The structure defined in “RX65N Group and RX651 Group DTCb Sequence Transfer Examples (R01AN3092EJ)” has already been defined in the DTC FIT module. Definition in this sample code is not required.

4.7 Variables List

Table 4-6 lists global variables, Table 4-7 lists static variables, Table 4-8 lists const variables, and Table 4-9 lists static const variables. For DTC Vector table and DTC index table, DTC FIT module secures them in the heap. Therefore variables-specific definition is not required.

Table 4-6 Global Variables

Type	Variables name	Description
volatile uint16_t	g_dtc_rx_sqnum	Receive sequence number storage area
uint16_t	g_dtc_rx_buf0[4]	Receive data storage area for Sequence transfer Example 1 (sqnum=0)
uint16_t	g_dtc_rx_buf0[8]	Receive data storage area for Sequence transfer Example 2 (sqnum=1)
uint16_t	g_dtc_rx_buf0[12]	Receive data storage area for Sequence transfer Example 3 (sqnum=2)
uint16_t	g_dtc_rx_buf0[16]	Receive data storage area for Sequence transfer Example 4 (sqnum=3)

Table 4-7 static variables

Type	Variables name	Description
static dtc_transfer_data_cfg_t	g_dtc_pre_info_sqnum	Settings of DTC transfer information for sequence number receive
static dtc_transfer_data_cfg_t	g_dtc_pre_seqinfo_sqnum0[3]	DTC transfer information settings for Sequence Transfer Example 1(sqnum=0)
static dtc_transfer_data_cfg_t	g_dtc_pre_seqinfo_sqnum1[3]	DTC transfer information settings for Sequence Transfer Example 2(sqnum=1)
static dtc_transfer_data_cfg_t	g_dtc_pre_seqinfo_sqnum2[3]	DTC transfer information settings for Sequence Transfer Example 3(sqnum=2)
static dtc_transfer_data_cfg_t	g_dtc_pre_seqinfo_sqnum3[4]	DTC transfer information settings for Sequence Transfer Example 4(sqnum=3)
static dtc_transfer_data_t	g_dtc_info_sqnum	DTC transfer information for sequence number receive
static dtc_transfer_data_t	g_dtc_seqinfo_sqnum0[3]	DTC transfer information for Sequence Transfer 1(sqnum=0)
static dtc_transfer_data_t	g_dtc_seqinfo_sqnum1[3]	DTC transfer information for Sequence Transfer Example 2(sqnum=1)
static dtc_transfer_data_t	g_dtc_seqinfo_sqnum2[3]	DTC transfer information for Sequence Transfer Example 3 (sqnum=2)
static dtc_transfer_data_t	g_dtc_seqinfo_sqnum3[3]	DTC transfer information for Sequence Transfer Example 4 (sqnum=3)

Table 4-8 const variables

Type	Variables name	Description
const uint8_t	g_dtc_fcrh_sqnum	FCR.H register settings when receiving sequence number

Table 4-9 static const variables

Type	Variables name	Description
static const uint8_t	dtc_fcrh_data[4]	FCR.H register settings

4.8 Functions List

Table 4-10 lists the functions.

Table 4-10 Functions

Function name	Description
main()	Main processing
trap()	Error processing
R_DTC_FITInit()	DTC FIT module initial setting processing
dtc_rx_buf_clear()	DTC transfer destination area initial setting
dtc_pre_info_sqnum_init()	Configuration of DTC transfer information settings for Receive command
dtc_pre_seqinfo_sqnum0_init()	Configuration of DTC transfer information settings for Sequence Transfer Example 1 (sqnum=0)
dtc_pre_seqinfo_sqnum1_init()	Configuration of DTC transfer information settings for Sequence Transfer Example 2 (sqnum=1)
dtc_pre_seqinfo_sqnum2_init()	Configuration of DTC transfer information settings for Sequence Transfer Example 3 (sqnum=2)
dtc_pre_seqinfo_sqnum3_init()	Configuration of DTC transfer information settings for Sequence Transfer Example 4 (sqnum=3)

Note : The function configures DTC transfer information settings. Transfer information is set by setting the value to the argument of DTC FIT module API.

4.9 Functions Specification

Functions specification for sample code is shown as follows.

Main	
Overview	Main processing
Header	None
Declaration	void main(void)
Description	Initializes SCI10 and DTC, and starts asynchronous serial receive after the initial setting.
Argument	None
Return value	None

Trap	
Overview	Error processing
Header	None
Declaration	void trap(void)
Description	It is called when error occurs.
Argument	None
Return value	None

R_DTC_FITInit	
Overview	DTC FIT module initial setting processing
Header	None
Declaration	void R_DTC_FITInit(void)
Description	Initializes DTC FIT module and set sequence transfer information.
Argument	None
Return value	None

dtc_rx_buf_clear	
Overview	Initial setting for DTC transfer destination area
Header	None
Declaration	void dtc_rx_buf_clear(void)
Description	Zero-clears DTC transfer destination area
Argument	None
Return value	None

dtc_pre_info_sqnum_init	
Overview	DTC transfer information initial setting for receive command
Header	None
Declaration	void dtc_pre_info_sqnum_init(void)
Description	Configures the transfer information to DTC-transfer the command received from external communication device when starting sequence transfer. Transfer information can be set by setting the variables “g_dtc_pre_info_sqnum” specified in this process to third argument of R_DTC_Create() in DTC FIT module.
Argument	None
Return value	None

dtc_pre_seqinfo_sqnum0_init	
Overview	Configuration of DTC transfer information settings for Sequence Transfer Example 1 (sqnum=0)
Header	None
Declaration	void dtc_pre_seqinfo_sqnum0_init(void)
Description	Configures DTC transfer information for Sequence Transfer Example 1(sqnum=0). Transfer information can be set by setting the variables "g_dtc_pre_seqinfo_sqnum0[]" specified in this process to third argument of R_DTC_CreateSeq() in DTC FIT module.
Argument	None
Return value	None

dtc_pre_seqinfo_sqnum1_init	
Overview	Configuration of DTC transfer information settings for Sequence Transfer Example 2 (sqnum=1)
Header	None
Declaration	void dtc_pre_seqinfo_sqnum1_init(void)
Description	Configures DTC transfer information for Sequence Transfer Example 2(sqnum=1). Transfer information can be set by setting the variables "g_dtc_pre_seqinfo_sqnum1[]" specified in this process to third argument of R_DTC_CreateSeq() in DTC FIT module.
Argument	None
Return values	None

dtc_pre_seqinfo_sqnum2_init	
Overview	Configuration of DTC transfer information settings for Sequence Transfer Example 3 (sqnum=2)
Header	None
Declaration	void dtc_pre_seqinfo_sqnum2_init(void)
Description	Configures DTC transfer information for Sequence Transfer Example 3 (sqnum=2). Transfer information can be set by setting the variables "g_dtc_pre_seqinfo_sqnum2[]" specified in this process to third argument of R_DTC_CreateSeq() in DTC FIT module.
Argument	None
Return values	None

dtc_pre_seqinfo_sqnum3_init	
Overview	Configuration of DTC transfer information settings for Sequence Transfer Example 4 (sqnum=3)
Header	None
Declaration	void dtc_pre_seqinfo_sqnum3_init(void)
Description	Configures DTC transfer information for Sequence Transfer Example 4(sqnum=3). Transfer information can be set by setting the variables "g_dtc_pre_seqinfo_sqnum3[]" specified in this process to third argument of R_DTC_CreateSeq() in DTC FIT module.
Arguments	None
Return values	None

4.10 Flow Chart

4.10.1 Main Processing

Figure 4-2 shows the flow chart of main processing.

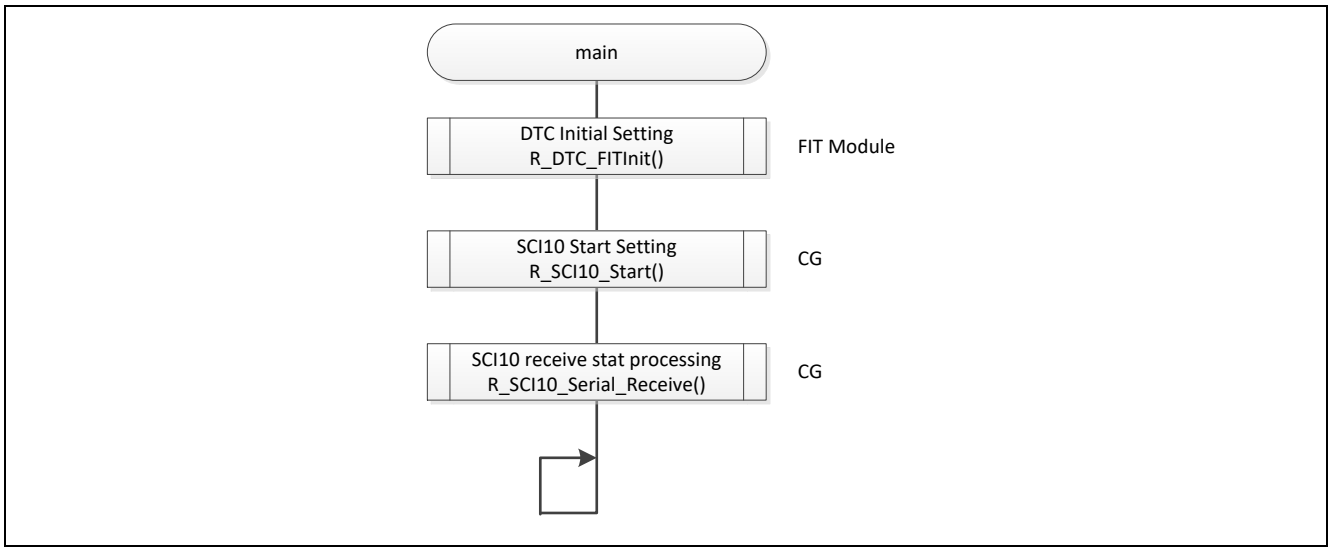

Figure 4-2 Main Processing

4.10.2 DTC FIT Module Initial Setting Processing

Figure 4-3 and Figure 4-4 show the flow chart of DTC FIT module initial setting processing.

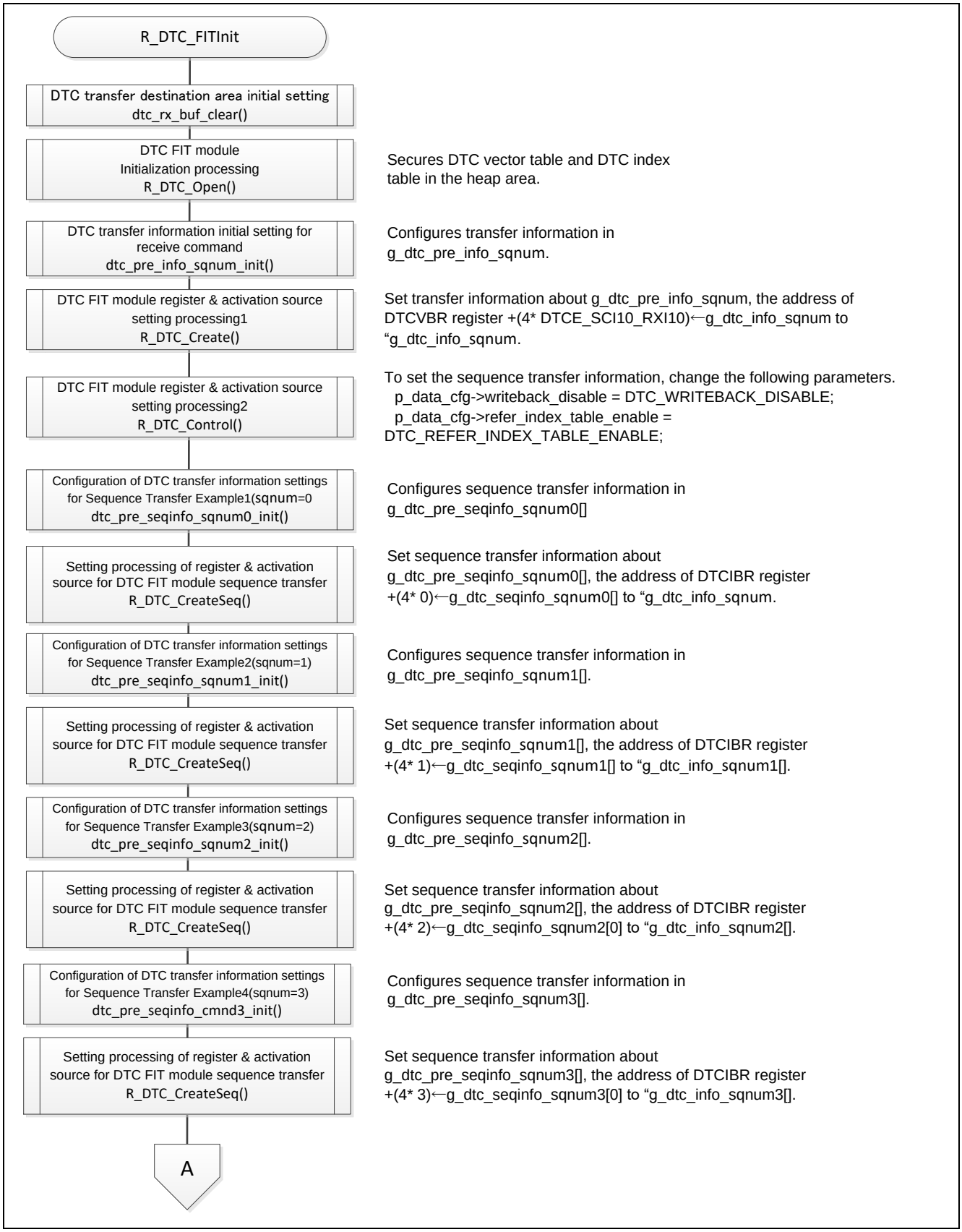

Figure 4-3 DTC FIT Module Initial Setting Processing 1

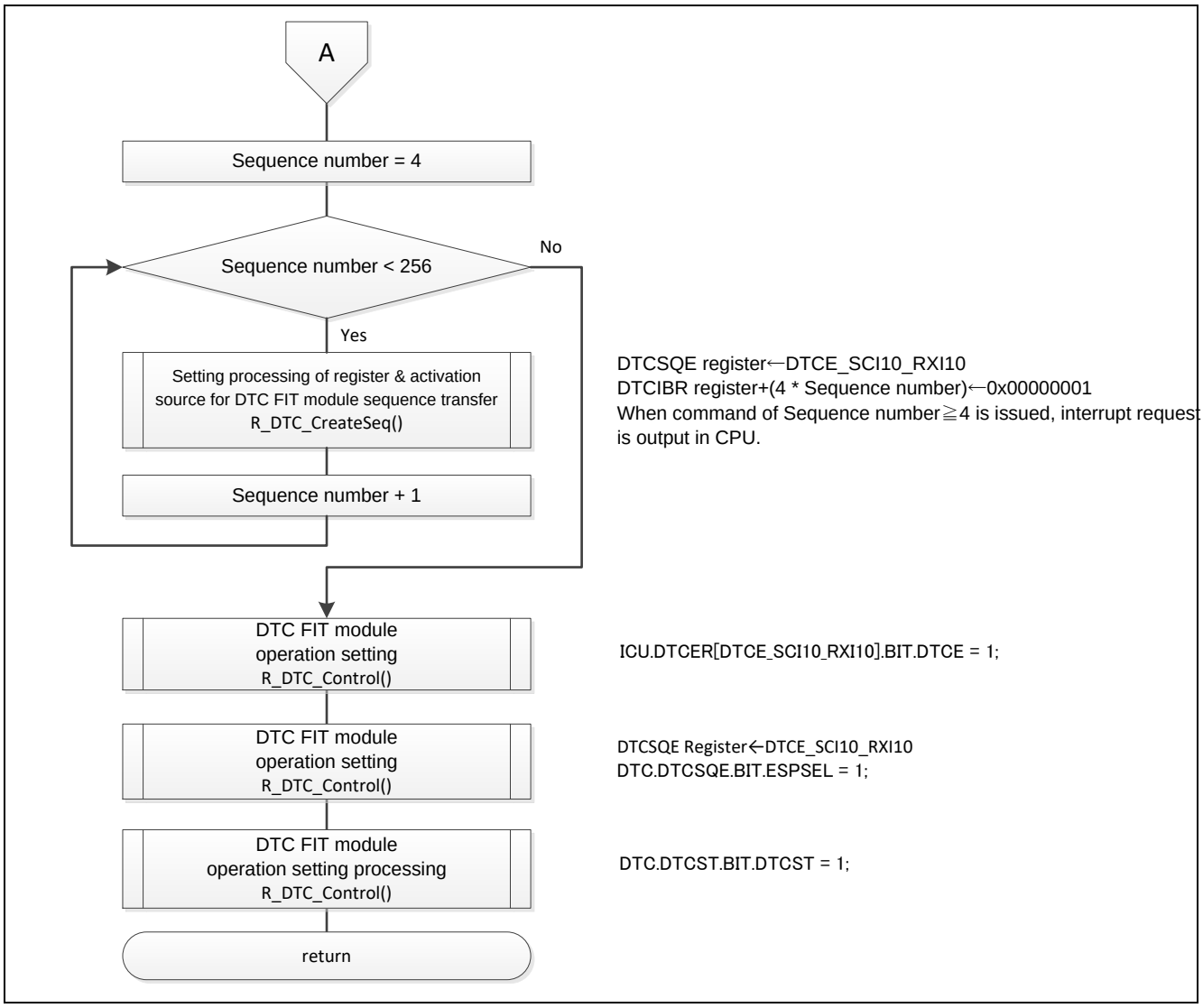

Figure 4-4 DTC FIT Module Initial Setting Processing 2

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Renesas Electronics Website

http://www.renesas.com/

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul 31, 2017	-	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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