# RL78/G14

## Timer RG in Phase Counting Mode CC-RL

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### Abstract

This document describes how to detect the phase difference between external input signals from pins TRGCLKA and TRGCLKB using the RL78/G14 timer RG in phase counting mode.


### Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

## Contents

## 1. Specifications

The RL78/G14 MCU detects the phase difference between external input signals from pins TRGCLKA and TRGCLKB and the counter starts counting.

Table 1.1 lists the peripheral function and its application and Figure 1.1 shows an operation overview of phase counting mode.

**Table 1.1 Peripheral Function and Its Application**

| Peripheral Function | Application |
|---|---|
| Timer RG | Detects the phase difference between pins TRGCLKA and TRGCLKB |

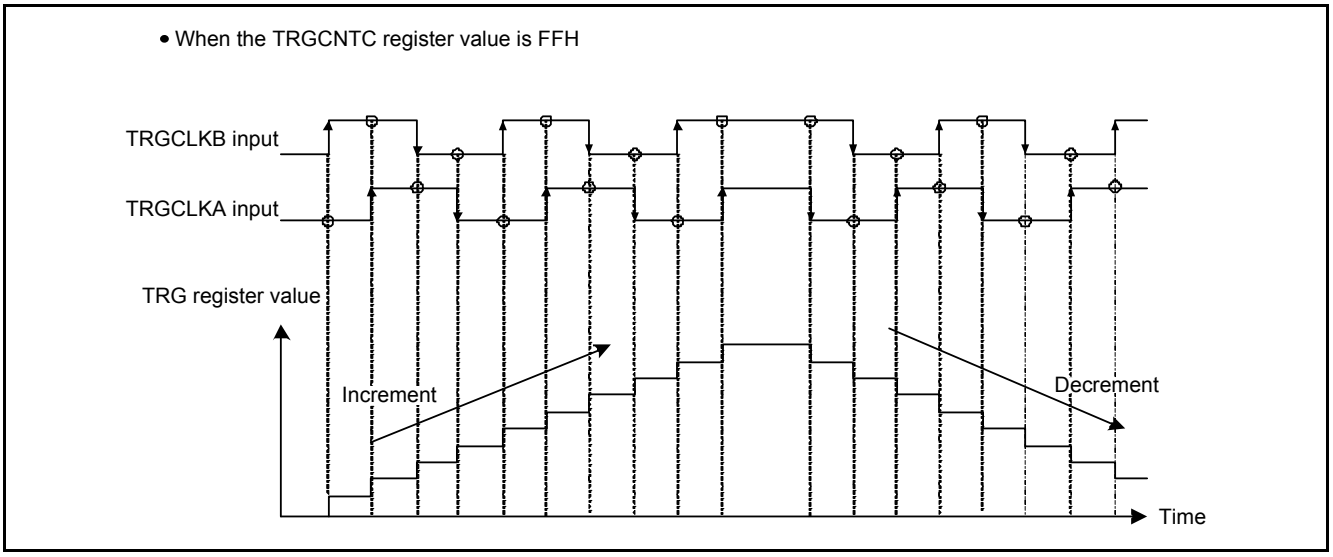



**Figure 1.1 Operation Overview of Phase Counting Mode**

## 2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

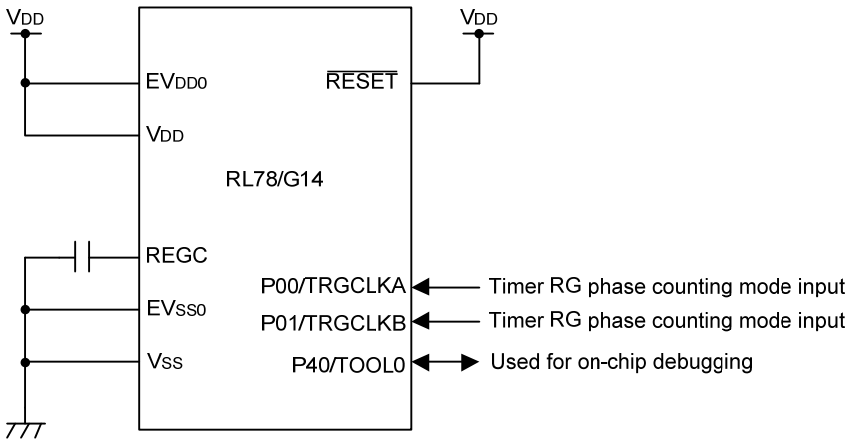
**Table 2.1 Operation Confirmation Conditions**

| Item | Contents |
|---|---|
| MCU used | RL78G14 (R5F104PJA) |
| Operating frequency | • High-speed on-chip oscillator clock ($f_{HOCO}$): 16 MHz (typ.)<br>• CPU/peripheral hardware clock ($f_{CLK}$): 16 MHz |
| Operating voltage | 5.0 V (operation enabled from 2.9 to 5.5 V)<br>LVD operation ($V_{LVD}$): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode |
| Integrated development environment (CS+) | Renesas Electronics Corporation<br>CS+ V3.01.00 |
| C compiler (CS+) | Renesas Electronics Corporation<br>CC-RL V1.01.00 |
| Integrated development environment ($e^2$ studio) | Renesas Electronics Corporation<br>$e^2$ studio V4.0.0.26 |
| C compiler ($e^2$ studio) | Renesas Electronics Corporation<br>CC-RL V1.01.00 |

## 3. Hardware

### 3.1 Hardware Configuration

Figure 3.1 shows the hardware configuration used in this application note.




Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either VDD or VSS via resistors).
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVD) specified by the LVD.

**Figure 3.1 Hardware Configuration**

## 3.2 Pins Used

Table 3.1 lists the pins used and their functions.

**Table 3.1 Pins Used and Their Functions**

| Pin Name | I/O | Function |
|---|---|---|
| P00/TRGCLKA | Input | Inputs an external signal |
| P01/TRGCLKB | Input | Inputs an external signal |

# 4. Software

## 4.1 Operation Overview

Use timer RG in phase counting mode to detect the phase difference between external input signals from pins TRGCLKA and TRGCLKB, and increment or decrement the TRG register.

Set timer RG as follows:

- Use timer RG in phase counting mode
- Do not clear the TRG register
- Digital filter is disabled in pins TRGCLKA and TRGCLKB
- Set 0000H in the TRG register as a default value
- Specify the counter enable bit to increment or decrement
- Enable overflow and underflow interrupts
- Set pins PM01 and PM00 to input mode

Table 4.1 lists increment or decrement conditions of the TRG register.

**Table 4.1 Increment or Decrement Conditions of the TRG Register**

| TRGCLKB pin | ↑ | H | ↓ | L | H | ↓ | L | ↑ |
|---|---|---|---|---|---|---|---|---|
| TRGCLKA pin | L | ↑ | H | ↓ | ↓ | L | ↑ | H |
| Bits CNTEN7 to CNTEN0 in the TRGCNTC register | CNTEN7 | CNTEN6 | CNTEN5 | CNTEN4 | CNTEN3 | CNTEN2 | CNTEN1 | CNTEN0 |
| Increment/decrement | +1 | +1 | +1 | +1 | −1 | −1 | −1 | −1 |

Figure 4.1 shows the operation of phase counting mode.

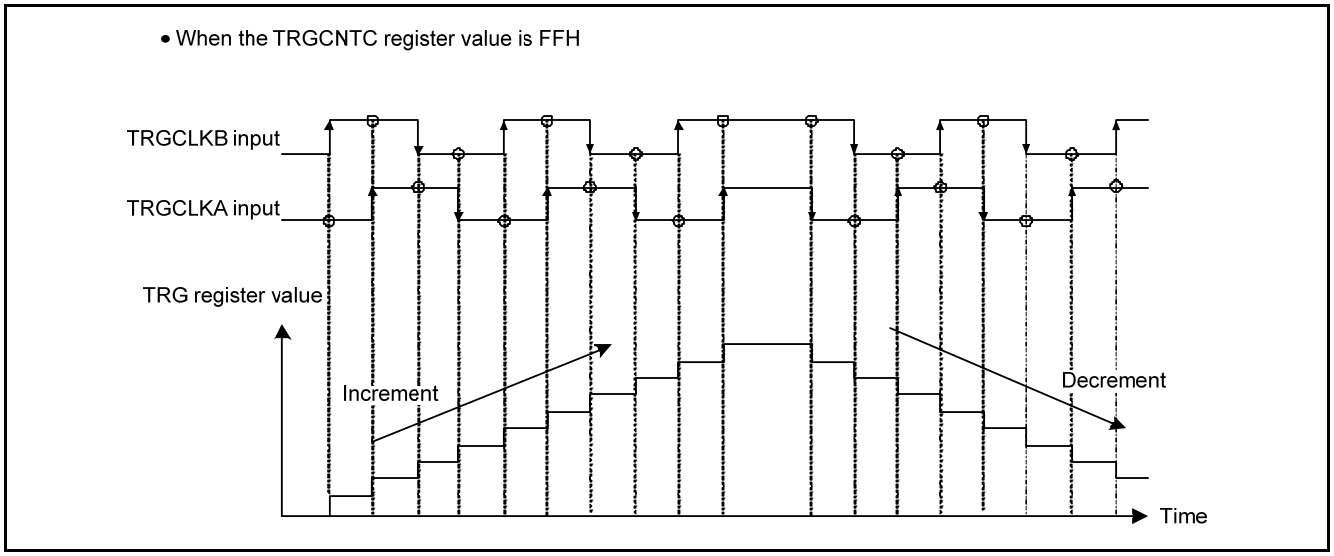



**Figure 4.1 Operation Example of Phase Counting Mode**

## 4.2 Setting Option Bytes

Table 4.2 lists the option byte setting.

**Table 4.2 Option Bytes**

| Address | Setting Value | Contents |
|---|---|---|
| 000C0H/010C0H | 11101111B | Stops the watchdog timer<br>(counting is stopped after a reset is released) |
| 000C1H/010C1H | 01111111B | Sets the LVD in reset mode<br>Detection voltage: 2.81 V at the rising edge,<br>2.75 V at the falling edge |
| 000C2H/010C2H | 11101001B | Sets the high-speed on-chip oscillator clock as 16 MHz, and the flash operating mode in HS (high-speed) mode |
| 000C3H/010C3H | 10000100B | Enables on-chip debugging |

## 4.3 Variables

Table 4.3 lists the global variables.

**Table 4.3 Global Variables**

| Type | Variable Name | Contents | Function Used |
|---|---|---|---|
| uint8_t | inttrg_over_cnt | Number of overflows | r_tmr_rg0_interrupt |
| uint8_t | inttrg_under_cnt | Number of underflows | r_tmr_rg0_interrupt |

## 4.4 Functions

Table 4.4 lists the functions.

**Table 4.4 Functions**

| Function Name | Outline |
|---|---|
| hdwinit | Initialization |
| R_Systeminit | Peripheral functions initialization |
| R_CGC_Create | CPU clock initialization |
| R_TMR_RG0_Create | Timer RG initialization |
| main | Main processing |
| R_TMR_RG0_Start | Timer RG start setting |
| r_tmr_rg0_interrupt | Timer RG interrupt handling |

## 4.5 Function Specifications

The following tables list the sample code function specifications.

| hdwinit | |
|---|---|
| **Outline** | Initialization |
| **Header** | None |
| **Declaration** | void hdwinit(void) |
| **Description** | Initializes the peripheral functions. |
| **Arguments** | None |
| **Return Value** | None |

| R_Systeminit | |
|---|---|
| **Outline** | Peripheral functions initialization |
| **Header** | None |
| **Declaration** | void R_Systeminit(void) |
| **Description** | Initializes the peripheral function used in this application note. |
| **Arguments** | None |
| **Return Value** | None |

| R_CGC_Create | |
|---|---|
| **Outline** | CPU clock initialization |
| **Header** | r_cg_cgc.h |
| **Declaration** | void R_CGC_Create(void) |
| **Description** | Initializes the CPU clock. |
| **Arguments** | None |
| **Return Value** | None |

| R_TMR_RG0_Create | |
|---|---|
| **Outline** | Timer RG Initialization |
| **Header** | r_cg_timer.h |
| **Declaration** | void R_TMR_RG0_Create(void) |
| **Description** | Initializes timer RG for use in phase counting mode. |
| **Arguments** | None |
| **Return Value** | None |

| main | |
|---|---|
| **Outline** | Main processing |
| **Header** | None |
| **Declaration** | void main(void) |
| **Description** | Performs main processing. |
| **Arguments** | None |
| **Return Value** | None |

| R_TMR_RG0_Start | |
|---|---|
| **Outline** | Timer RG start setting |
| **Header** | r_cg_timer.h |
| **Declaration** | void R_TMR_RG0_Start(void) |
| **Description** | Sets timer RG to start in phase counting mode. |
| **Arguments** | None |
| **Return Value** | None |

| r_tmr_rg0_interrupt | |
|---|---|
| **Outline** | Timer RG interrupt handling |
| **Header** | r_cg_timer.h |
| **Declaration** | static void __near r_tmr_rg0_interrupt(void) |
| **Description** | Counts the number of overflows when the timer overflows, or the number of underflows when the timer underflows. |
| **Arguments** | None |
| **Return Value** | None |

## 4.6 Flowcharts

### 4.6.1 Overall Flowchart

Figure 4.2 shows the overall flow.

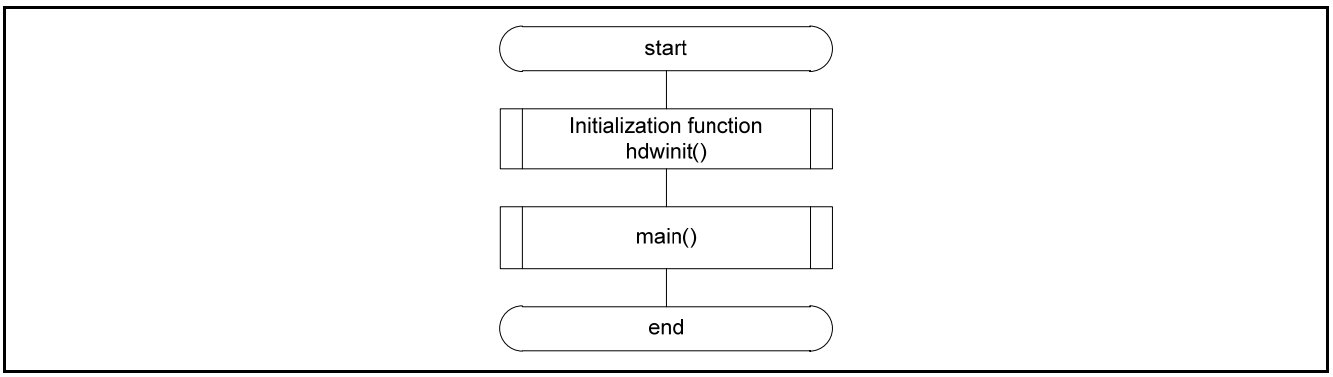



**Figure 4.2 Overall Flow**

### 4.6.2 Initialization

Figure 4.3 shows the initialization.

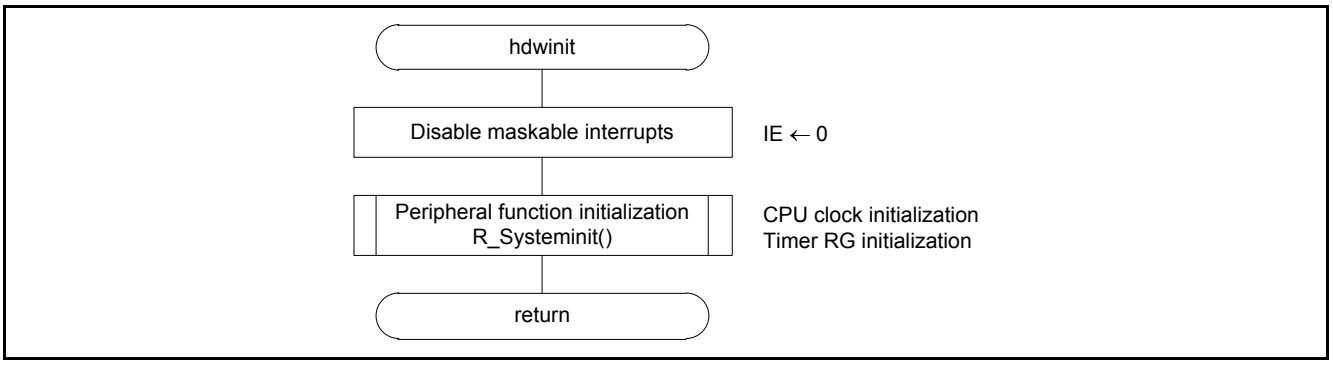



**Figure 4.3 Initialization**

### 4.6.3 Peripheral Function Initialization

Figure 4.4 shows the peripheral function initialization.

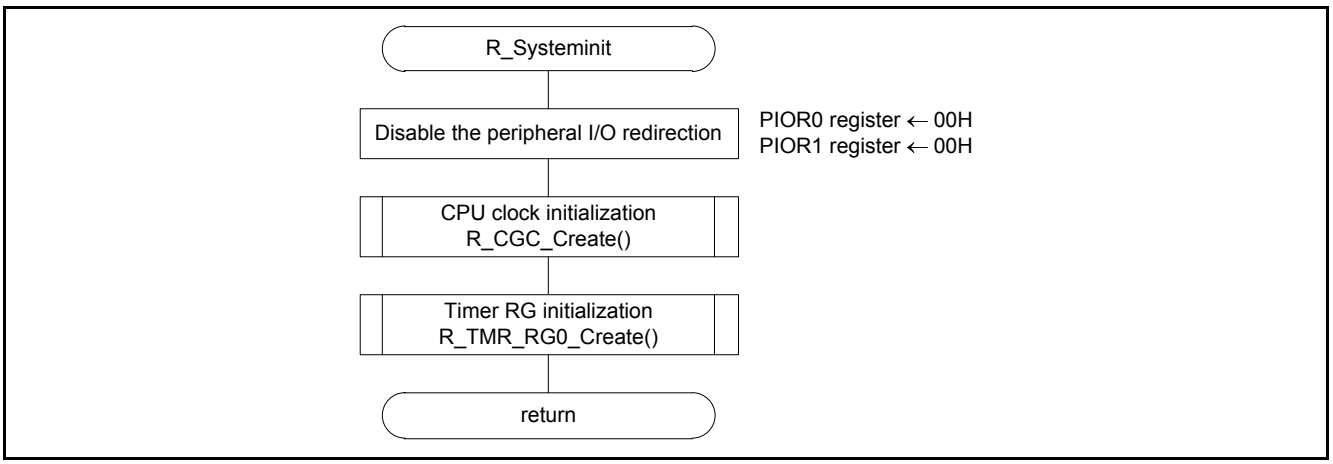



**Figure 4.4 Peripheral Function Initialization**

### 4.6.4 CPU Clock Initialization

Figure 4.5 shows the CPU clock initialization.

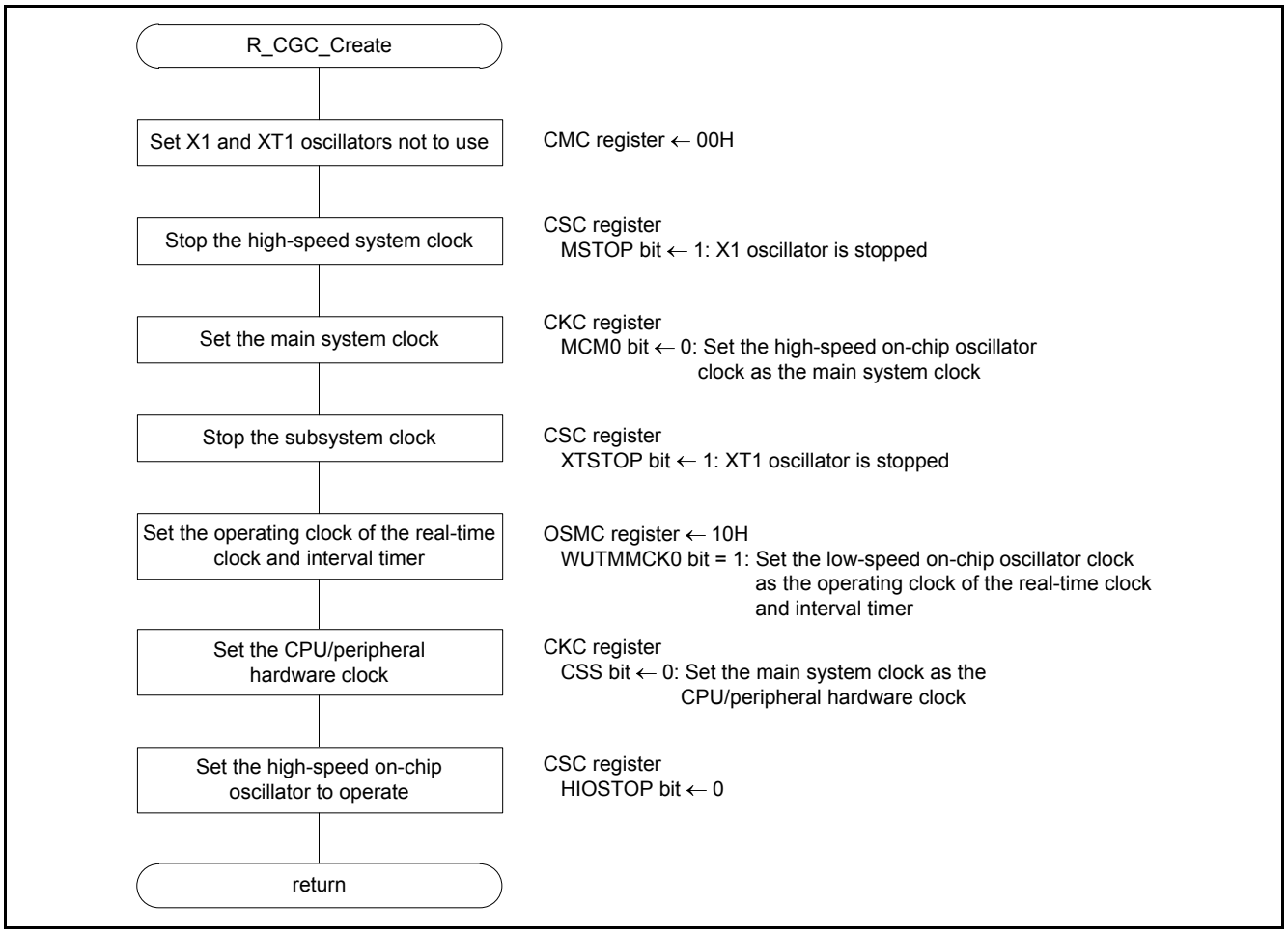



**Figure 4.5 CPU Clock Initialization**

### 4.6.5 Timer RG Initialization

Figure 4.6 shows the timer RG initialization.

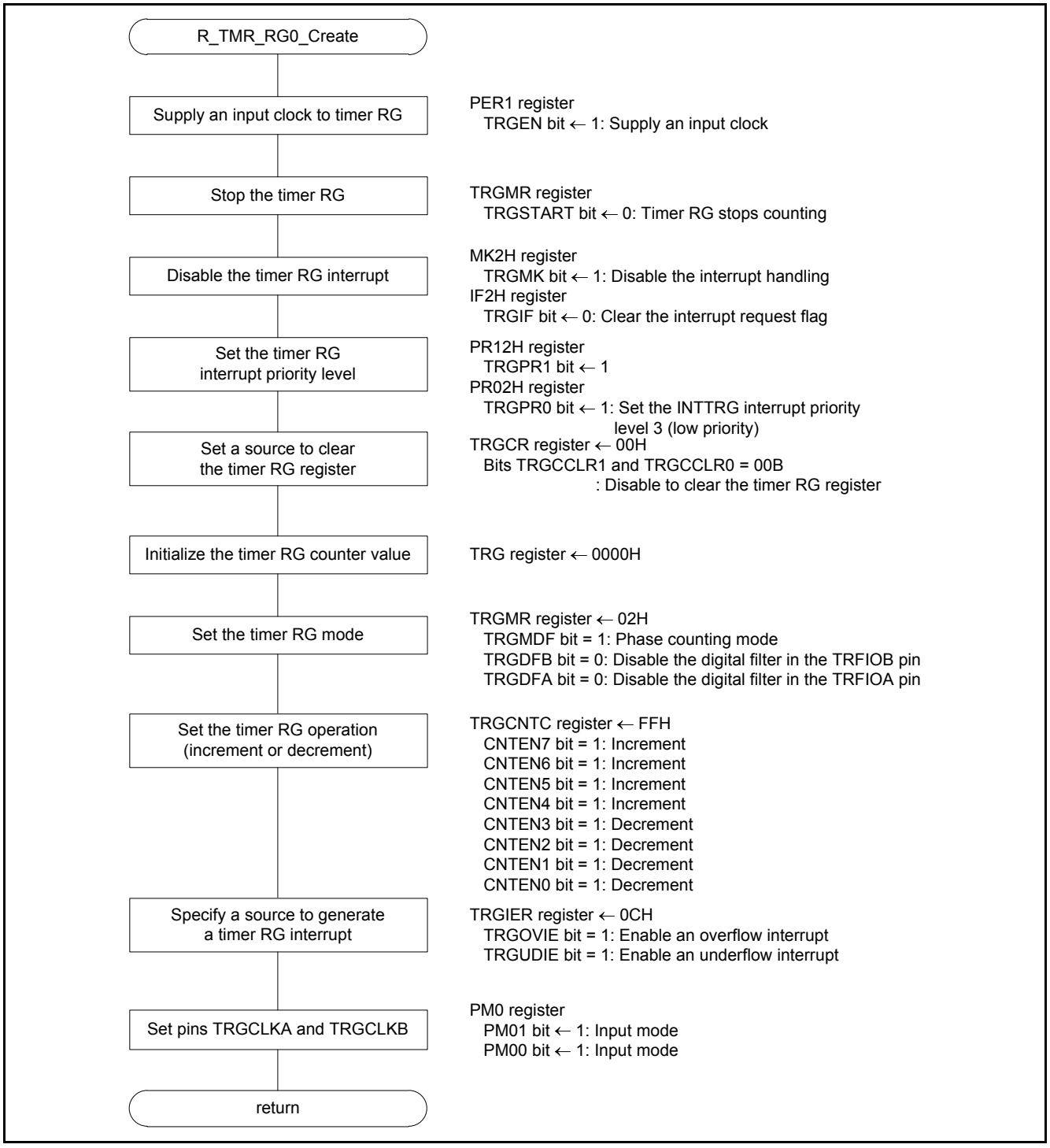



**Figure 4.6 Timer RG Initialization**

Supplying an input clock to timer RG

- Peripheral enable register 1 (PER1)
  Enables to supply the clock to timer RG

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PER1 | DACEN | TRGEN | CMPEN | TRD0EN | DTCEN | 0 | 0 | TRJ0EN |
| Value | × | 1 | × | × | × | – | – | × |

- Bit 6

| TRGEN | Function |
|---|---|
| 0 | Stops supplying an input clock to timer RG<br>• Writing to the SFR which is used by timer RG is disabled<br>• Timer RG is in reset status |
| 1 | Supplies an input clock to timer RG<br>• Reading or writing to the SFR which is used by timer RG is enabled |

Timer RG stops counting

- Timer RG mode register (TRGMR)
  Stops timer RG to count

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGMR | TRGSTART | TRGELCICE | TRGDFCK1 | TRGDFCK0 | TRGDFB | TRGDFA | TRGMDF | TRGPWM |
| Value | 0 | × | × | × | | | | × |

- Bit 7

| TRGSTART | Function |
|---|---|
| 0 | Stops the TRG to count, and initializes the PWM output signal (TRGIOA pin) in PWM mode |
| 1 | Sets the TRG to start counting |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Disabling timer RG interrupt

- Interrupt mask flag register (MK2H)
  Disables an INTTRG interrupt

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MK2H | FLMK | IICAMK1 | 1 | SREMK3<br>TMMK13H | TRGMK | TRDMK1 | TRDMK0 | PMK11<br>CMPMK1 |
| Value | × | × | – | × | 1 | × | × | × |

- Bit 3

| TRGMK | Function |
|---|---|
| 0 | Enables an interrupt handling |
| 1 | Disables an interrupt handling |

- Interrupt request flag register (IF2H)
  Clears the INTTRG interrupt request flag

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IF2H | FLIF | IICAIF1 | 0 | SREIF3<br>TMIF13H | TRGIF | TRGIF1 | TRDIF0 | PIF11<br>CMPIF1 |
| Value | × | × | – | × | 0 | × | × | × |

- Bit 3

| TRGIF | Function |
|---|---|
| 0 | Interrupt request signal is not generated |
| 1 | Interrupt request signal is generated and interrupt-requested status |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Setting the timer RG interrupt priority level

- Priority specification flag registers (PR12H, PR02H)
  Sets the timer RG interrupt priority to level 3 (low priority)

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PR12H | FLPR1 | IICAPR11 | 1 | SREPR13<br>TMPR113H | TRGPR1 | TRDPR11 | TRDPR10 | PPR111<br>CMPPR11 |
| Value | × | × | – | × | 1 | × | × | × |

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PR02H | FLPR0 | IICAPR01 | 1 | SREPR03<br>TMPR013H | TRGPR0 | TRDPR01 | TRDPR00 | PPR011<br>CMPPR01 |
| Value | × | × | – | × | 1 | × | × | × |

| TRGPR1 | TRGPR0 | Priority level |
|---|---|---|
| 0 | 0 | Specifies level 0 (high priority) |
| 0 | 1 | Specifies level 1 |
| 1 | 0 | Specifies level 2 |
| 1 | 1 | Specifies level 3 (low priority) |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Setting a source to clear timer RG

- Timer RG control register (TRGCR)
  Sets a source to clear the TRG register and count source

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGCR | – | TRGCCLR1 | TRGCCLR0 | TRGCKEG1 | TRGCKEG0 | TRGTCK2 | TRGTCK1 | TRGTCK0 |
| Value | – | 0 | 0 | × | × | × | × | × |

- Bits 6 and 5

| TRGCCLR1 | TRGCCLR0 | Function |
|---|---|---|
| 0 | 0 | Clearing the TRG register is disabled |
| 0 | 1 | Clears the register by the TRGGRA input capture/compare match |
| 1 | 0 | Clears the register by the TRGGRB input capture/compare match |
| 1 | 1 | Do not set |

Initializing the timer RG counter value

- Timer RG counter (TRG)
  Specifies the counter as an initial value

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRG | TRG15 | TRG14 | TRG13 | TRG12 | TRG11 | TRG10 | TRG9 | TRG8 | TRG7 | TRG6 | TRG5 | TRG4 | TRG3 | TRG2 | TRG1 | TRG0 |
| Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| TRG15 to TRG0 | Function | Setting Range |
|---|---|---|
| Bits 15 to 0 | Timer RG increments or decrements in phase counting mode | 0000H to FFFFH |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Setting timer RG mode

- Timer RG mode register (TRGMR)
  Sets timer RG in phase counting mode

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGMR | TRGSTART | TRGELCICE | TRGDFCK1 | TRGDFCK0 | TRGDFB | TRGDFA | TRGMDF | TRGPWM |
| Value | | × | × | × | 0 | 0 | 1 | × |

- Bit 3

| TRGDFB | Function |
|---|---|
| 0 | Disables the digital filter |
| 1 | Enables the digital filter |

- Bit 2

| TRGDFA | Function |
|---|---|
| 0 | Disables the digital filter |
| 1 | Enables the digital filter |

- Bit 1

| TRGMDF | Function |
|---|---|
| 0 | Specifies to increment |
| 1 | Specifies phase counting mode |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Setting the timer RG operation

- Timer RG count control register (TRGCNTC)
  Sets the count conditions in phase counting mode

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGCNTC | CNTEN7 | CNTEN6 | CNTEN5 | CNTEN4 | CNTEN3 | CNTEN2 | CNTEN1 | CNTEN0 |
| Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

- Bit 7

| CNTEN7 | Function |
|---|---|
| 0 | Disabled |
| 1 | Increments<br>(When the TRGCLKA input is at low level and the TRGCLKB input is at the rising edge) |

- Bit 6

| CNTEN6 | Function |
|---|---|
| 0 | Disabled |
| 1 | Increments<br>(When the TRGCLKB input is at high level and the TRGCLKA input is at the rising edge) |

- Bit 5

| CNTEN5 | Function |
|---|---|
| 0 | Disabled |
| 1 | Increments<br>(When the TRGCLKA input is at high level and the TRGCLKB input is at the falling edge) |

- Bit 4

| CNTEN4 | Function |
|---|---|
| 0 | Disabled |
| 1 | Increments<br>(When the TRGCLKB input is at low level and the TRGCLKA input is at the falling edge) |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

- Bit 3

| CNTEN3 | Function |
|---|---|
| 0 | Disabled |
| 1 | Decrements<br>(When the TRGCLKB input is at high level and the TRGCLKA input is at the falling edge) |

- Bit 2

| CNTEN2 | Function |
|---|---|
| 0 | Disabled |
| 1 | Decrements<br>(When the TRGCLKA input is at low level and the TRGCLKB input is at the falling edge) |

- Bit 1

| CNTEN1 | Function |
|---|---|
| 0 | Disabled |
| 1 | Decrements<br>(When the TRGCLKB input is at low level and the TRGCLKA input is at the rising edge) |

- Bit 0

| CNTEN0 | Function |
|---|---|
| 0 | Disabled |
| 1 | Decrements<br>(When the TRGCLKA input is at high level and the TRGCLKB input is at the rising edge) |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Specifying a source to generate a timer RG interrupt

- Timer RG interrupt enable register (TRGIER)
  Enables interrupts by bits TRGOVF and TRGUDF

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGIER | – | – | – | – | TRGOVIE | TRGUDIE | TRGIMIEB | TRGIMIEA |
| Value | – | – | – | – | 1 | 1 | × | × |

- Bit 3

| TRGOVIE | Function |
|---|---|
| 0 | Disables an interrupt by the TRGOVF bit |
| 1 | Enables an interrupt by the TRGOVF bit |

- Bit 2

| TRGUDIE | Function |
|---|---|
| 0 | Disables an interrupt by the TRGUDF bit |
| 1 | Enables an interrupt by the TRGUDF bit |

Setting pins TRGCLKA and TRGCLKB

- Port mode register 0 (PM0)
  Sets pins TRGCLKA and TRGCLKB in input mode

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM0 | 1 | PM06 | PM05 | PM04 | PM03 | PM02 | PM01 | PM00 |
| Value | – | × | × | × | × | × | 1 | 1 |

- Bit 1

| PM01 | Function |
|---|---|
| 0 | Output mode (output buffer is on) |
| 1 | Input mode (output buffer is off) |

- Bit 0

| PM00 | Function |
|---|---|
| 0 | Output mode (output buffer is on) |
| 1 | Input mode (output buffer is off) |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

### 4.6.6 Main Processing

Figure 4.7 shows the main processing.

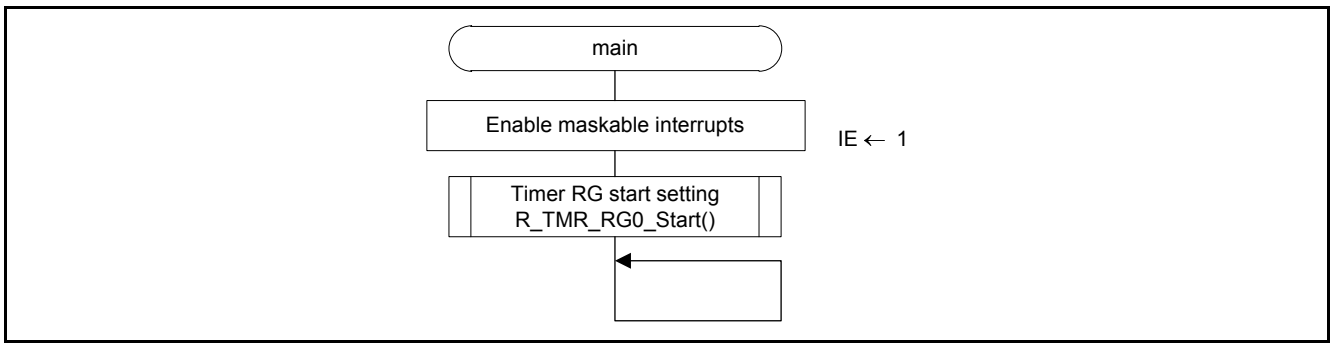



**Figure 4.7 Main Processing**

### 4.6.7 Setting Timer RG to Start

Figure 4.8 shows setting timer RG to start counting.

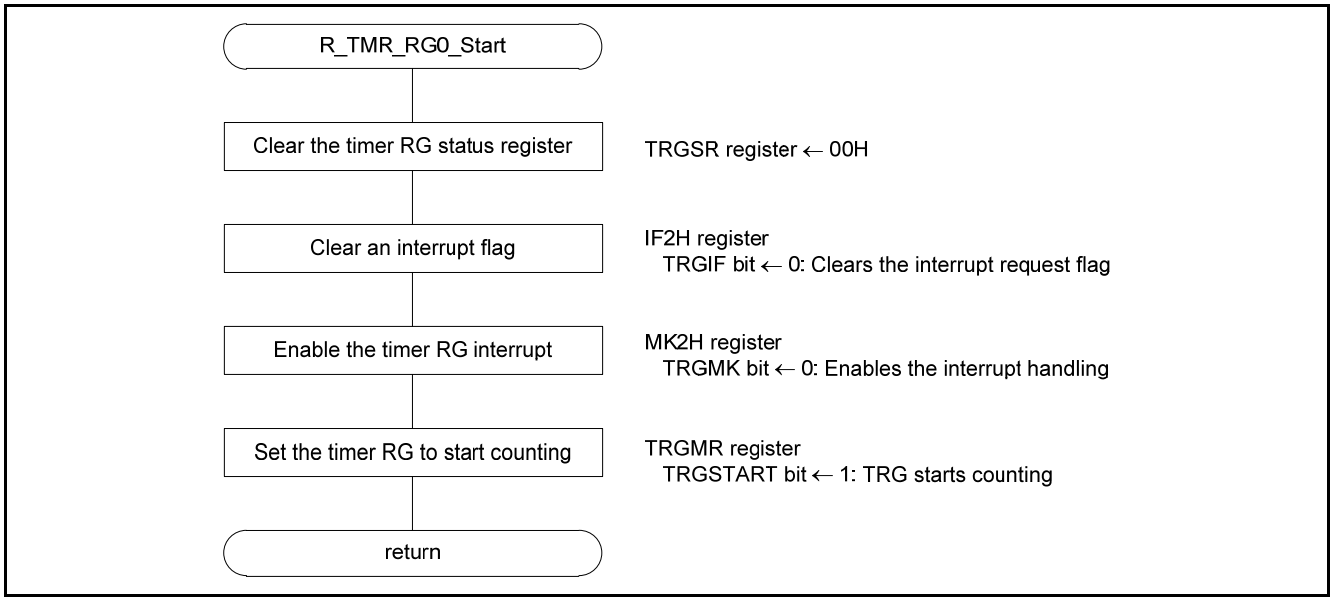



**Figure 4.8 Setting Timer RG to Start**

Clearing the timer RG status register

- Timer RG status register (TRGSR)
  Reads the timer RG status register, and clears flags overflow and underflow

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGSR | – | – | – | TRGDIRF | TRGOVF | TRGUDF | TRGIMFB | TRGIMFA |
| Value | – | – | – | × | 0 | 0 | × | × |

- Bit 3

| TRGOVF | Overflow flag | R/W |
|---|---|---|
| | Condition to be 0:<br>Write 0 after reading the bit | R/W |

- Bit 2

| TRGUDF | Underflow flag | R/W |
|---|---|---|
| | Condition to be 0:<br>Write 0 after reading the bit | R/W |

Clearing an interrupt flag

- Interrupt request flag register (IF2H)
  Clears the INTTRG interrupt request flag

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IF2H | FLIF | IICAIF1 | 0 | SREIF3<br>TMIF13H | TRGIF | TRDIF1 | TRDIF0 | PIF11<br>CMPIF1 |
| Value | × | × | – | × | 0 | × | × | × |

- Bit 3

| TRGIF | Function |
|---|---|
| 0 | Interrupt request signal is not generated |
| 1 | Interrupt request signal is generated and interrupt-requested status |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Enabling the timer RG interrupt

- Interrupt mask flag register (MK2H)
  Enables the INTTRG interrupt

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MK2H | FLMK | IICAMK1 | – | SREMK3<br>TMMK13H | TRGMK | TRDMK1 | TRDMK0 | PMK11<br>CMPMK1 |
| Value | × | × | – | × | 0 | × | × | × |

- Bit 3

| TRGMK | Function |
|---|---|
| 0 | Interrupt request is enabled |
| 1 | Interrupt request is disabled |

Sets timer RG to start counting

- Timer RG mode register (TRGMR)
  Sets timer RG to start counting

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGMR | TRGSTART | TRGELCICE | TRGDFCK1 | TRGDFCK0 | TRGDFB | TRGDFA | TRDMDF | TRGPWM |
| Value | 1 | × | × | × | | | | × |

- Bit 7

| TRGSTART | Function |
|---|---|
| 0 | Stops the TRG to count, and initializes the PWM output signal (TRGIOA pin) is in PWM mode |
| 1 | Sets the TRG to start counting |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

### 4.6.8 Timer RG Interrupt Handling

Figure 4.9 shows the timer RG interrupt handling.

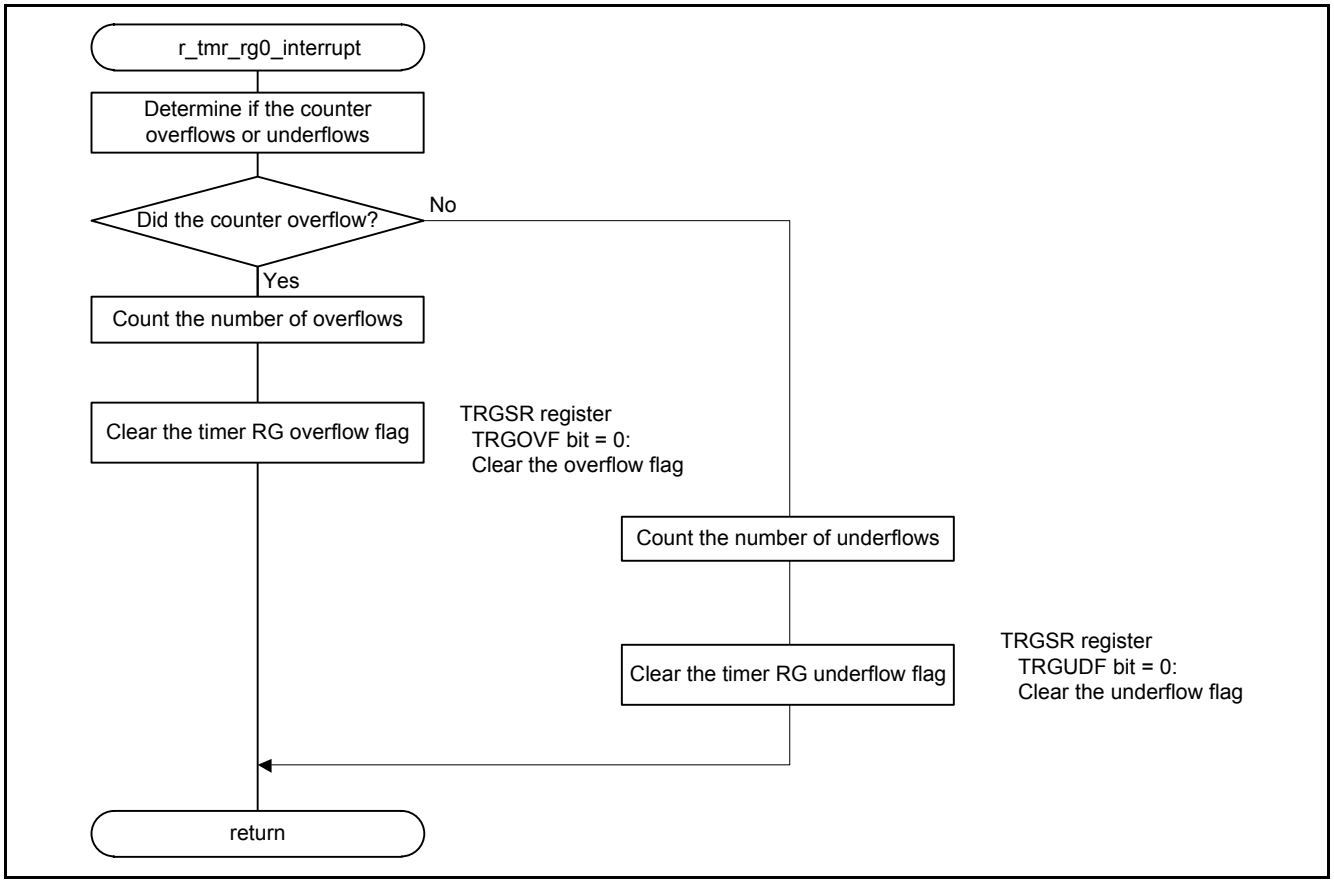



**Figure 4.9 Timer RG Interrupt Handling**

Clearing the timer RG overflow flag

- Timer RG status register (TRGSR)
  Clears the overflow flag after reading the timer RG status register

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGSR | – | – | – | TRGDIRF | TRGOVF | TRGUDF | TRDIMFB | TRGIMFA |
| Value | – | – | – | × | 0 | | × | × |

- Bit 3

| TRGOVF | Overflow flag | R/W |
|---|---|---|
| | Condition to be 0:<br>Write 0 after reading the bit | R/W |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

Clearing the timer RG underflow flag

- Timer RG status register (TRGSR)
  Clears the underflow flag after reading the timer RG status register

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TRGSR | – | – | – | TRGDIRF | TRGOVF | TRGUDF | TRDIMFB | TRGIMFA |
| Value | – | – | – | × | | 0 | × | × |

- Bit 2

| TRGUDF | Underflow flag | R/W |
|---|---|---|
| Condition to be 0:<br>Write 0 after reading the bit | | R/W |

For details on register setting, refer to the RL78/G14 User's Manual: Hardware.

Legend symbol:

×: Unused bit

Blank cell: Unchanged bit

–: Reserved bit or unallocated bit

## 5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

## 6. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186E)
RL78 Family User's Manual: Software (R01US0015E)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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| REVISION HISTORY | RL78/G14 Timer RG in Phase Counting Mode |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Oct. 01, 2015 | — | First edition issued |
| | | | |

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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