RL78/G14

Timer RD Using Input Capture Function and Output Compare Function

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Abstract

This document describes a method to use both the input capture function and output compare function of the RL78/G14 timer RD.

Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Use the input capture function in conjunction with the output compare function of timer RD channel 0 (hereinafter called timer RD0).
Measure the pulse width of the waveform input to the TRDIOA0 pin with the input capture function.
Change the output levels of pins TRDIOB0 and TRDIOD0 from low to high with the output compare function.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Operation Example Using the Input Capture Function in Conjunction with the Output Compare Function.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer RD (timer RD0)	Pulse width measurement and waveform output

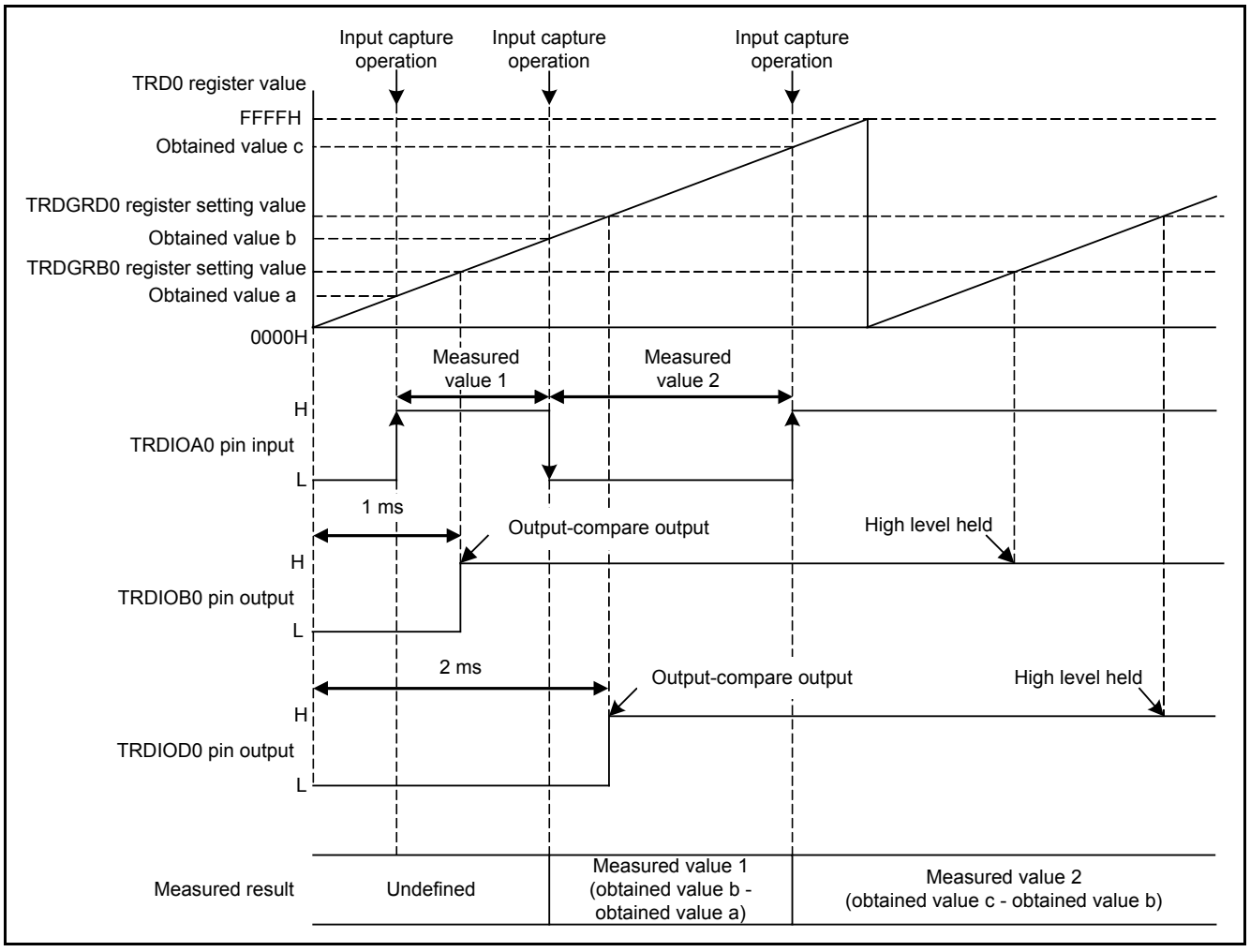


Figure 1.1 Operation Example Using the Input Capture Function in Conjunction with the Output Compare Function

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

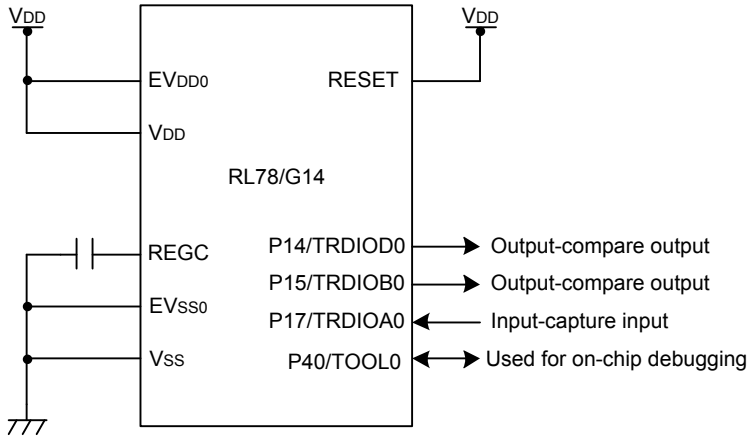
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 16 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 16 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVI}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.01.00
C compiler	Renesas Electronics Corporation CA78K0R V1.30
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.01

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either VDD or VSS via resistors).
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVI) specified by the LVD.

Figure 3.1 Hardware Configuration

3.2 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Function
P14/TRDIOD0	Output	Output-compare output
P15/TRDIOB0	Output	Output-compare output
P17/TRDIOA0	Input	Input-capture input

4. Software

4.1 Operation Overview

Use the input capture function in conjunction with the output compare function of timer RD0. Assign the input capture function to the TRDIOA0 pin and the output compare function to the TRDIOD0 pin.

The timer RD0 settings are shown below.

Settings:
- Use fCLK (16 MHz) as the count source.
- Operate timer TRD0 and timer TRD1 independently.
- Use the TRD0 counter to disable clear (free-running operation).
- Set the OVF bit to enable the OVI interrupt and the IMFA bit to enable the IMIA interrupt.
- Set the IMFB bit to disable the IMIB interrupt and the IMFD bit to disable the IMID interrupt.
- Use the TRDGRC0 register as the buffer register of the TRDGRA0 register.
- Use the digital filter function for the TRDIOA0 pin.
- Select the count source (fCLK) for the sampling clock of the TRDIOA0 pin digital filter.
- Detect the input capture to the TRDIOA0 pin at both edges.
- Use the TRDGRD0 register as the general register.
- Disable output for pins TRDIOA0 and TRDIOC0, and enable output for pins TRDIOB0 and TRDIOD0.
- Select low initial output for output levels of pins TRDIOB0 and TRDIOD0.
- Output high for the TRDIOB0 pin at the compare match with the TRDGRB0 register.
- Output high for the TRDIOD0 pin at the compare match with the TRDGRD0 register.

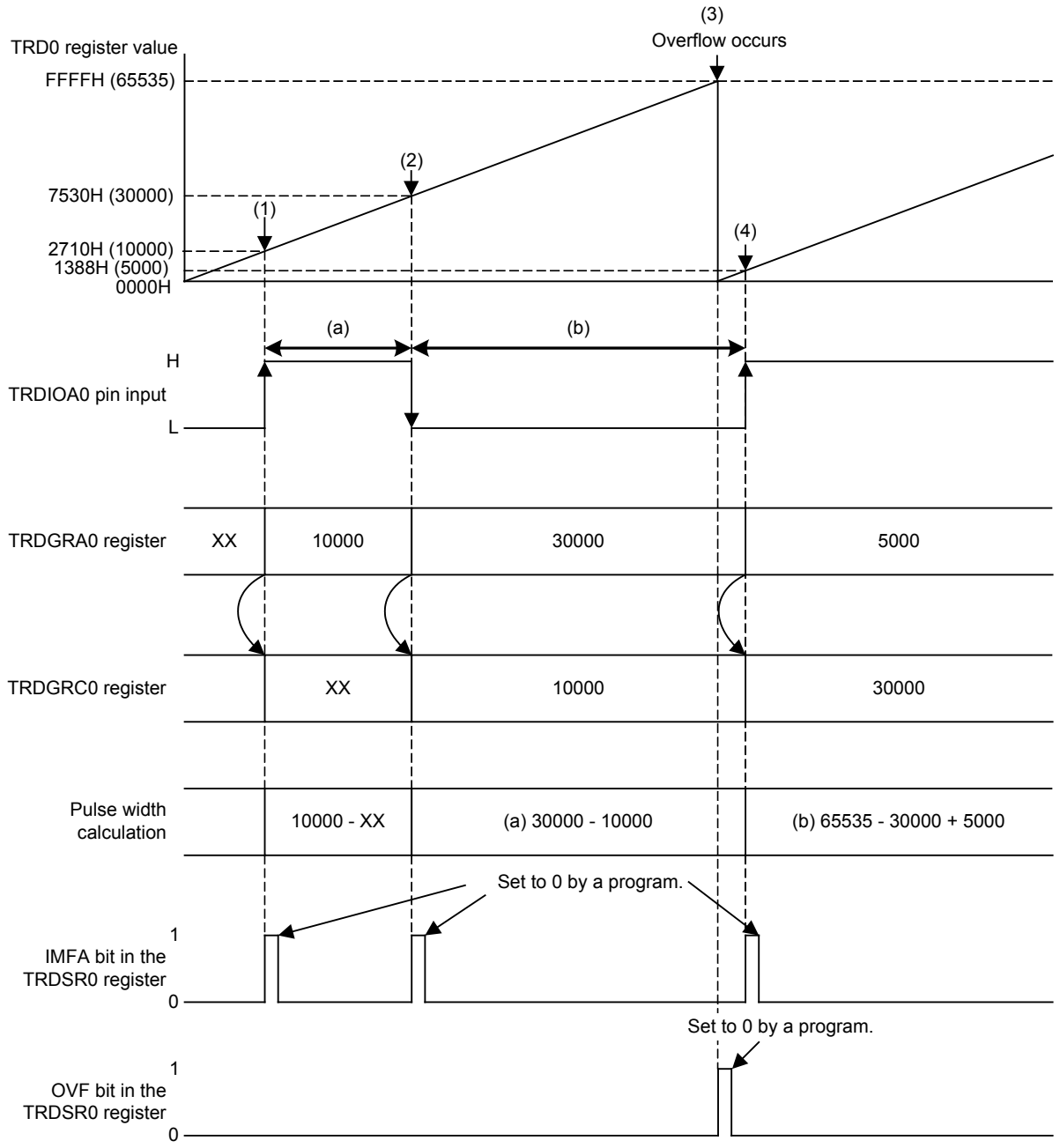
4.1.1 Descriptions of Input Capture Function

Detect the rising/falling edge input to the TRDIOA0 pin using the input capture function and calculate the pulse width (from rising edge to falling edge or falling edge to rising edge) based on the detected result.

When the TRD0 register does not overflow:
(1) When detecting the rising edge input to the TRDIOA0 pin, a timer RD0 interrupt is generated. Obtain the values of registers TRDGRA0 and TRDGRC0 in a timer RD0 interrupt service routine and set the capture flag. After returning to main processing from the timer RD0 interrupt service routine, calculate the pulse width based on the calculation formula when the TRD0 register does not overflow and clear the capture flag.
(2) When detecting the falling edge input to the TRDIOA0 pin, a timer RD0 interrupt is generated. Obtain the values of registers TRDGRA0 and TRDGRC0 in a timer RD interrupt service routine and set the capture flag. After returning to main processing from the timer RD0 interrupt service routine, calculate the pulse width based on the calculation formula when the TRD0 register does not overflow and clear the capture flag.

When the TRD0 register overflows:
(3) When the TRD0 register overflows, a timer RD0 interrupt is generated. Increment the value of the overflow counter in a timer RD0 interrupt service routine.
(4) When detecting rising edge input to the TRDIOA0 pin, a timer RD0 interrupt is generated. Obtain the values of registers TRDGRA0 and TRDGRC0 in the timer RD0 interrupt service routine and set the capture flag. After returning to main processing from the timer RD0 interrupt service routine, calculate the pulse width based on the calculation formula when the TRD0 register overflows, and clear the overflow counter and capture flag.

Figure 4.1 shows an Operation Example of Input Capture.



XX: Previous obtained value of the TRDGRA0 register

(a) Calculation example of the pulse width when the TRD0 register does not overflow:
Pulse width = time per count (1/16 MHz = 62.5 ns) × (current measured value – previous measured value)
= 62.5 ns × (30000 – 10000)
= 1.25 ms

(b) Calculation example of the pulse width when the TRD0 register overflows one time:
Pulse width = time per count (1/16 MHz = 62.5 ns) ×
(overflow count (1 time) × 10000H (65535) – previous measured value + current measured value)
= 62.5 ns × (65535 – 30000 + 10000)
= 2.844 ms

Figure 4.1 Operation Example of Input Capture

4.1.2 Descriptions of Output Compare Function

Using the output compare function, wait 1 ms after the timer RD0 count starts before changing the TRDIOB0 pin output level from low to high, and wait 2 ms before changing the TRDIOD0 pin output level from low to high. Subsequently, pins TRDIOB0 and TRDIOD0 are held high.

(1) Start the timer RD0 count.
(2) Change the output level of the TRDIOB0 pin from low to high at the compare match of registers TRD0 and TRDGRB0.
(3) Change the output level of the TRDIOD0 pin from low to high at the compare match of registers TRD0 and TRDGRD0.
(4) A TRD0 register overflow occurs and the TRD0 register is cleared to 0000H.
(5) Although registers TRD0 and TRDGRB0 are compare matched, the output level is held since the output level of the TRDGRB0 pin is high.
(6) Although registers TRD0 and TRDGRD0 are compare matched, the output level is held since the output level of the TRDGRD0 pin is high.

Figure 4.2 shows an Operation Example of Output Compare.

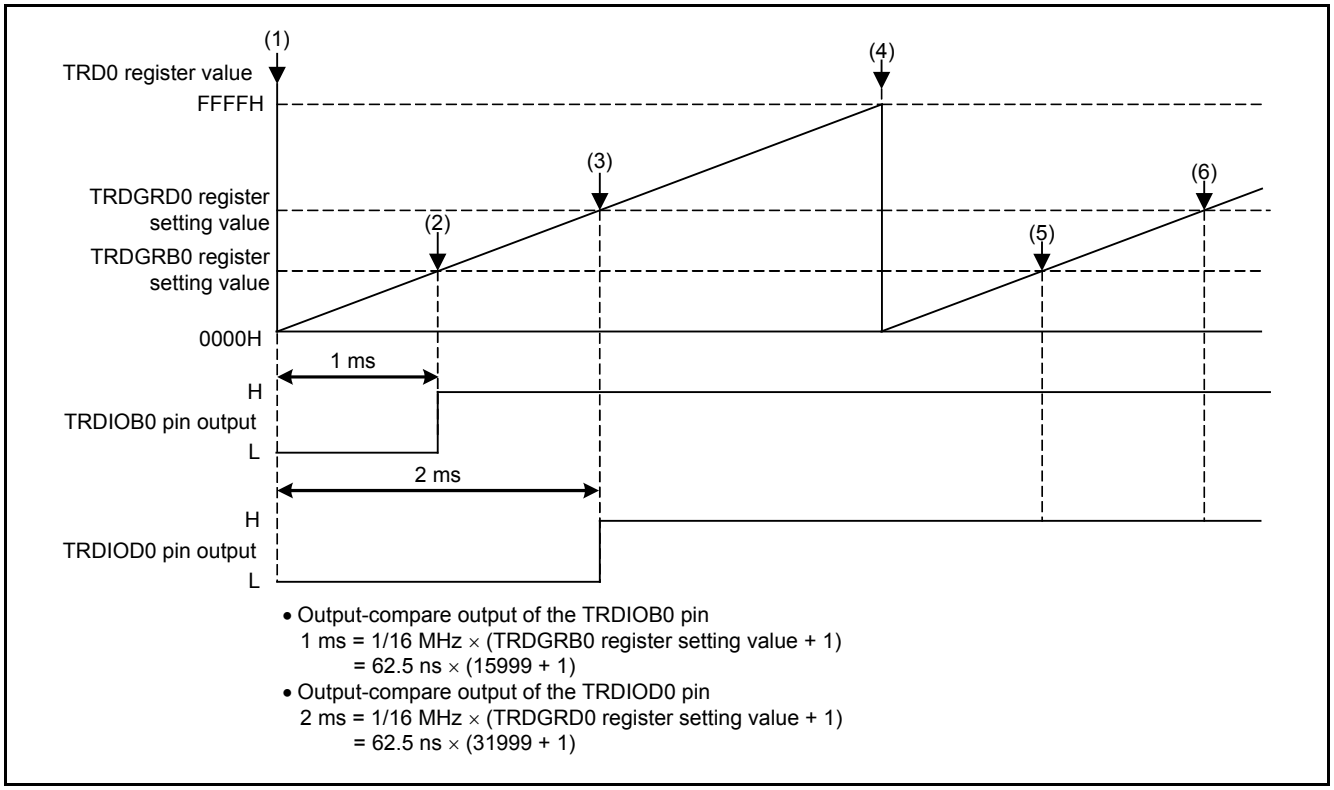


Figure 4.2 Operation Example of Output Compare

4.2 Option-Setting Memory

Table 4.1 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 4.1 Option-Setting Memory Configured in the Sample Code

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Variables

Table 4.2 lists the Global Variables.

Table 4.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	f_capture	Capture flag	main, r_tmr_rd0_interrupt
unsigned short	ovf_cnt	Overflow counter	main, r_tmr_rd0_interrupt
unsigned short	general_register	Current measured value	main, r_tmr_rd0_interrupt
unsigned short	buffer_register	Previous measured value	main, r_tmr_rd0_interrupt
unsigned long	measurement_value	Calculation result of pulse width	main

4.4 Functions

Table 4.3 lists the Functions.

Table 4.3 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of the CPU
timer_rd0_init	Initial setting of timer RD
main	Main processing
timer_rd0_start	Timer RD count start setting
r_tmr_rd0_interrupt	Timer RD0 interrupt

4.5 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	Initial setting of the CPU
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

timer_rd0_init	
Outline	Initial setting of timer RD
Header	None
Declaration	void timer_rd0_init(void)
Description	Perform the initial setting for the input capture function and output compare function of timer RD.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	• Perform main processing. • Calculate the pulse width.
Argument	None
Return Value	None

timer_rd0_start	
Outline	Timer RD count start setting
Header	None
Declaration	void timer_rd0_start(void)
Description	Perform timer RD count start setting.
Argument	None
Return Value	None

r_tmr_rd0_interrupt	
Outline	Timer RD0 interrupt
Header	None
Declaration	void r_tmr_rd0_interrupt(void)
Description	• Perform timer RD0 interrupt service routine. • When the edge is input to the TRDIOA0 pin, read the value of the general register and buffer register. • When detecting an overflow, update the overflow counter.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Overall Flowchart

Figure 4.3 shows the Overall Flowchart.

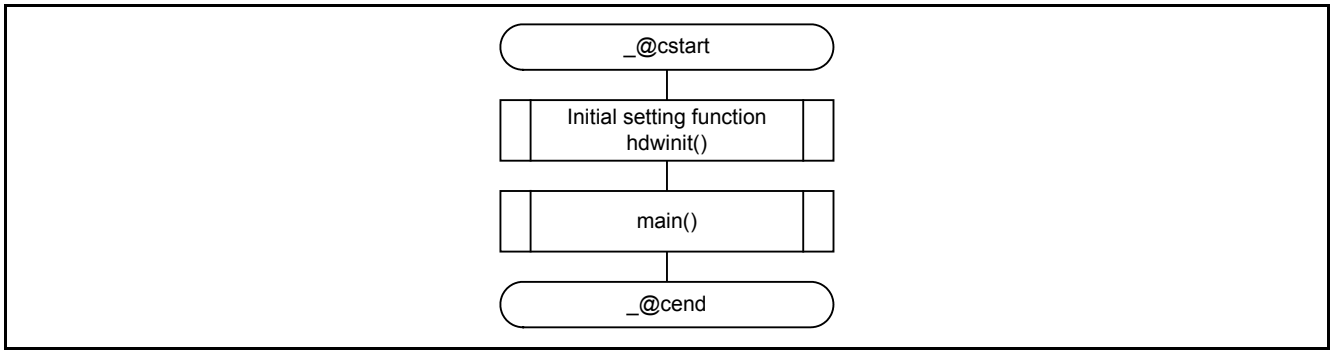


Figure 4.3 Overall Flowchart

4.6.2 Initial Setting

Figure 4.4 shows the Initial Setting.

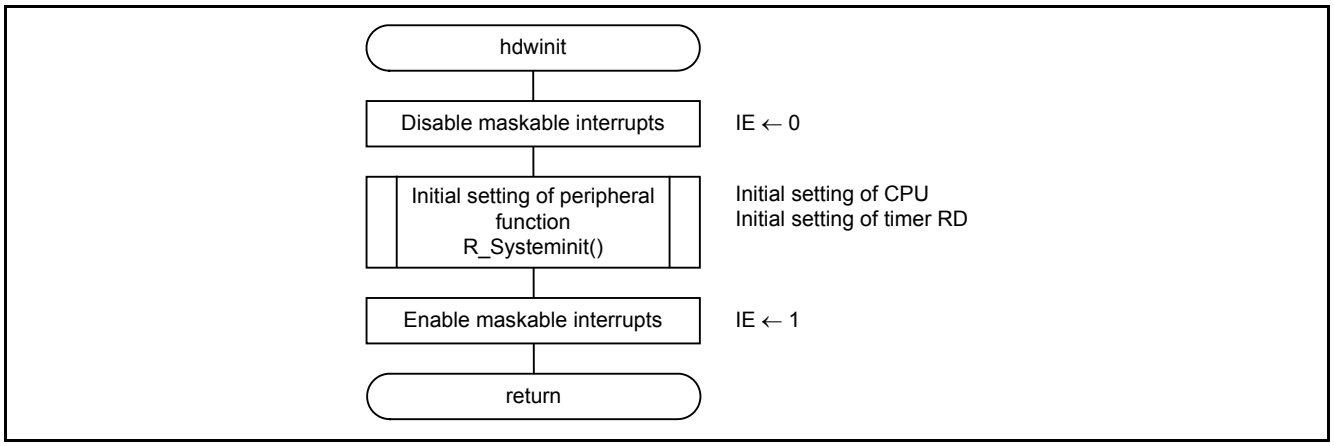


Figure 4.4 Initial Setting

4.6.3 Initial Setting of Peripheral Functions

Figure 4.5 shows the Initial Setting of Peripheral Functions.

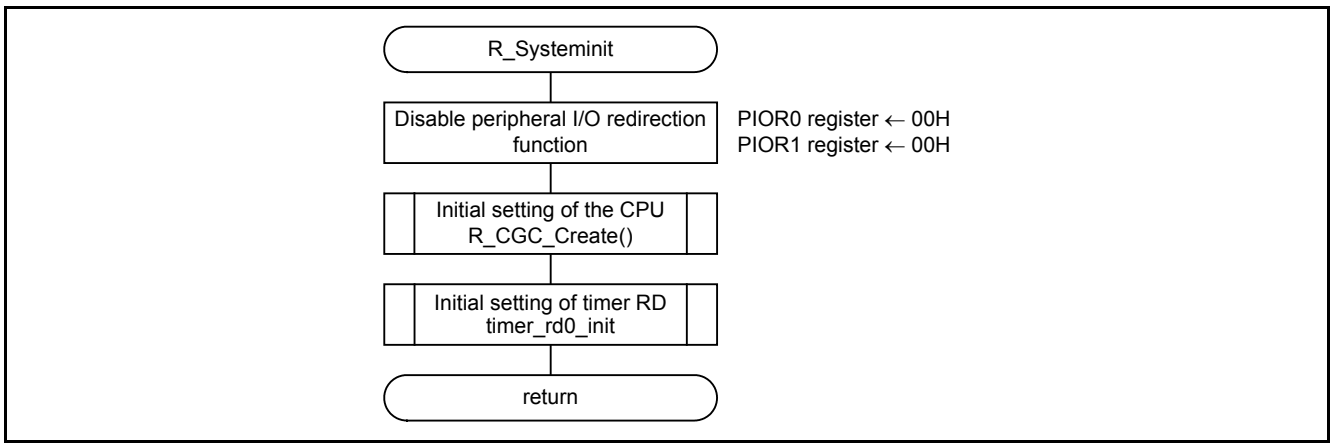


Figure 4.5 Initial Setting of Peripheral Functions

4.6.4 Initial Setting of the CPU

Figure 4.6 shows the Initial Setting of the CPU.

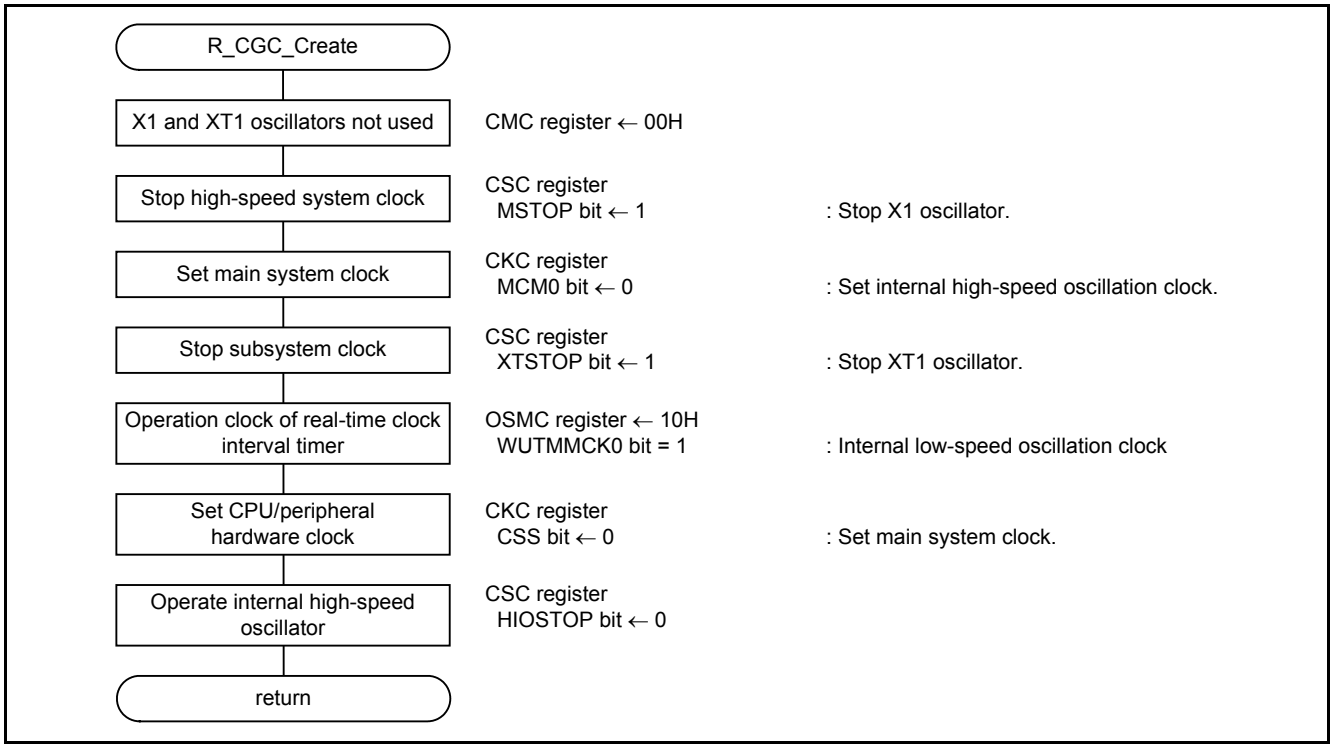


Figure 4.6 Initial Setting of the CPU

4.6.5 Initial Setting of Timer RD

Figure 4.7 shows the Initial Setting of Timer RD.

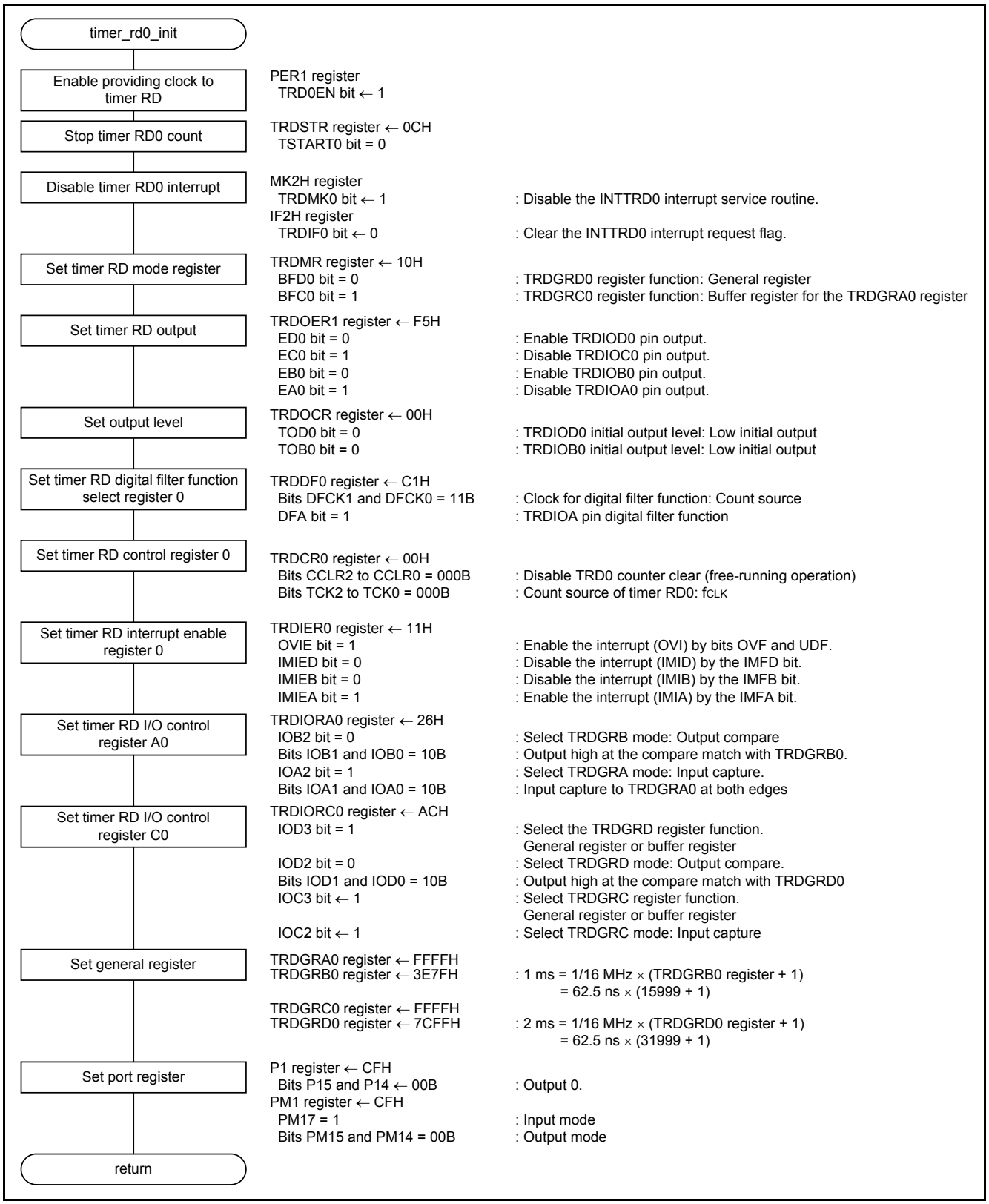


Figure 4.7 Initial Setting of Timer RD

Enable providing a clock to timer RD.

- Peripheral Enable Register 1 (PER1)
  Enable providing a clock to timer RD.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	x	x	1	x	—	—	x

Bit 4

TRD0EN	Control of timer RD input clock supply
0	Stops input clock supply. • SFR used by timer RD cannot be written. • Timer RD is in the reset status.
1	Enables input clock supply. • SFR used by timer RD can be read and written.

Stop the timer RD0 count.

- Timer RD Mode Register (TRDSTR)
  Stop the timer RD0 count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—	x		x	0

Bit 2

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	Count continues after compare match with TRDGRA0 register

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Disable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	x	1	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD mode register.

- Timer RD Mode Register (TRDMR)
  Use the TRDGRD0 register as the general register and TRDGRC0 register as the buffer register of the TRDGRA0 register.

Symbol	7	6	5	4	3	2	1	0
TRDMR	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
Setting Value	x	x	0	1	—	—	—	

Bit 5

BFD0	TRDGRD0 register function select
0	General register
1	Buffer register for TRDGRB0 register

Bit 4

BFC0	TRDGRC0 register function select
0	General register
1	Buffer register for TRDGRA0 register

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RD output.

- Timer RD Output Master Enable Register 1 (TRDOER1)
  Disable output of pins TRDIOC0 and TRDIOA0, and enable output of pins TRDIOB0 and TRDIOD0.

Symbol	7	6	5	4	3	2	1	0
TRDOER1	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
Setting Value	x	x	x	x	0	1	0	1

Bit 3

ED0	TRDIOD0 output disable
0	Output enabled
1	Output disabled (TRDIOD0 pin functions as an I/O port.)

Bit 2

EC0	TRDIOC0 output disable
0	Output enabled
1	Output disabled (TRDIOC0 pin functions as an I/O port.)

Bit 1

EB0	TRDIOB0 output disable
0	Output enabled
1	Output disabled (TRDIOB0 pin functions as an I/O port.)

Bit 0

EA0	TRDIOA0 output disable
0	Output enabled
1	Output disabled (TRDIOA0 pin functions as an I/O port.)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set output levels.

- Timer RD Output Control Register (TRDOCR)
  Set low for initial output of pins TRDIOD0 and TRDIOB0.

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Setting Value	x	x	x	x	0	x	0	x

Bit 3

TOD0	TRDIOD0 initial output level select
0	Low initial output
1	High initial output

Bit 1

TOB0	TRDIOB0 initial output level select
0	Low initial output
1	High initial output

Set timer RD digital filter function select register 0.

- Timer RD Digital Filter Function Select Register 0 (TRDDF0)
  Use the TRDIOA0 pin digital filter function.

Symbol	7	6	5	4	3	2	1	0
TRDDF0	DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
Setting Value	1	1	x	x	x	x	x	1

Bits 7 and 6

DFCK1	DFCK0	Clock select for digital filter function
0	0	$f_{CLK}/32$
0	1	$f_{CLK}/8$
1	0	f_{CLK}
1	1	Count source (clock selected by bits TCK0 to TCK2 in the TRDCR0 register)

Bit 0

DFA	TRDIOA pin digital filter function select
0	Function is not used
0	Function is used
If the digital filter is enabled, edge detection is performed after five or more cycles of the digital filter sampling clock have elapsed.	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RD control register 0.

- Timer RD Control Register 0 (TRDCR0)
  Disable counter clear of timer RD0 and set f_{CLK} to the count source.

Symbol	7	6	5	4	3	2	1	0
TRDCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
Setting Value	0	0	0	x	x	0	0	0

Bits 7 to 5

CCLR2	CCLR1	CCLR0	TRD0 counter clear select
0	0	0	Clear disabled (free-running operation)
0	0	1	Clear by input capture/compare match with TRDGRA0
0	1	0	Clear by input capture/compare match with TRDGRB0
0	1	1	Synchronous clear (clear simultaneously with other timer RDi counter)
1	0	0	Do not set.
1	0	1	Clear by input capture/compare match with TRDGRC0
1	1	0	Clear by input capture/compare match with TRDGRD0
1	1	1	Do not set.

Bits 2 to 0

TCK2	TCK1	TCK0	Count source select
0	0	0	f_{CLK}, f_{HOCO}
0	0	1	$f_{CLK}/2$
0	1	0	$f_{CLK}/4$
0	1	1	$f_{CLK}/8$
1	0	0	$f_{CLK}/32$
1	0	1	TRDCLK input
1	1	0	Do not set.
1	1	1	Do not set.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RD interrupt enable register 0.

- Timer RD Interrupt Enable Register 0 (TRDIER0)
  Set the OVF bit to enable the interrupt (OVI) and the IMFA bit to enable the interrupt (IMIA). Set the IMFD bit to disable the interrupt (IMID) and the IMFB bit to disable the interrupt (IMIB).

Symbol	7	6	5	4	3	2	1	0
TRDIER0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
Setting Value	—	—	—	1	0	x	0	1

Bit 4

OVIE	Overflow/underflow interrupt enable
0	Interrupt (OVI) by bits OVF and UDF disabled
1	Interrupt (OVI) by bits OVF and UDF enabled

Bit 3

IMIED	Input capture/compare match interrupt enable D
0	Interrupt (IMID) by the IMFD bit is disabled
1	Interrupt (IMID) by the IMFD bit is enabled

Bit 1

IMIEB	Input capture/compare match interrupt enable B
0	Interrupt (IMIB) by the IMFB bit is disabled
1	Interrupt (IMIB) by the IMFB bit is enabled

Bit 0

IMIEA	Input capture/compare match interrupt enable A
0	Interrupt (IMIA) by the IMFA bit is disabled
1	Interrupt (IMIA) by the IMFA bit is enabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RD I/O control register A0.

- Timer RD I/O Control Register A0 (TRDIORA0)
  Output high at the compare match with the TRDGRB0 register.

Symbol	7	6	5	4	3	2	1	0
TRDIORA0	0	IOB2	IOB1	IOB0	0	IOA2	IOA1	IOA0
Setting Value	—	0	1	0	—	1	1	0

Bit 6

IOB2	TRDGRB mode select
Set to 0 (output compare) in the output compare function.	

Bits 5 and 4

IOB1	IOB0	TRDGRB control
0	0	Pin output by compare match is disabled (TRDIOB0 pin functions as an I/O port)
0	1	Low output by compare match with TRDGRB0
1	0	High output by compare match with TRDGRB0
1	1	Toggle output by compare match with TRDGRB0

Bit 2

IOA2	TRDGRA mode select
Set to 1 (input capture) in the input capture function.	

Bits 1 and 0

IOA1	IOA0	TRDGRA control
0	0	Input capture to TRDGRA0 at the rising edge
0	1	Input capture to TRDGRA0 at the falling edge
1	0	Input capture to TRDGRA0 at both edges
1	1	Do not set.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RD I/O control register C0.

- Timer RD I/O Control Register C0 (TRDIORC0)
  Do not use the TRDGRD register as the TRDIOB output register.

Symbol	7	6	5	4	3	2	1	0
TRDIORC0	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Setting Value	1	0	1	0	1	1	x	x

Bit 7

IOD3	TRDGRD register function select
0	TRDIOB output register
1	General register or buffer register

Bit 6

IOD2	TRDGRD mode select
Set to 0 (output compare) in the output compare function.	

Bits 5 and 4

IOD1	IOD0	TRDGRD control
0	0	Pin output by compare match is disabled
0	1	Low output by compare match with TRDGRD0
1	0	High output by compare match with TRDGRD0
1	1	Toggle output by compare match with TRDGRD0

Bit 3

IOC3	TRDGRC register function select
Set to 1 (general register or buffer register) in the input capture function.	

Bit 2

IOC2	TRDGRC mode select
Set to 1 (input capture) in the input capture function.	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set general registers.

- Timer RD General Register A0 (TRDGRA0)
  Set FFFFH to the TRDGRA0 register.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRA0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.5 General Register Functions in the Input Capture Function.	0000H to FFFFH

- Timer RD General Register B0 (TRDGRB0)
  Set 3E7FH to change the TRDIOB0 pin output in 1 ms after the count starts.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRB0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.4 General Register Functions in the Output Compare Function.	0000H to FFFFH

- Timer RD General Register C0 (TRDGRC0)
  Set FFFFH to the TRDGRC0 register.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRC0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.5 General Register Functions in the Input Capture Function.	0000H to FFFFH

- Timer RD General Register D0 (TRDGRD0)
  Set 7CFFH to change the TRDIOB0 pin output in 2 ms after the count starts.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRB0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.4 General Register Functions in the Output Compare Function.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Table 4.4 General Register Functions in the Output Compare Function

Register	Setting		Register Function		Output-Compare Output Pin
	BFj0	IOj3			
TRDGRA0	—	—	General register. Write the compare value.		TRDIOA0
TRDGRB0					TRDIOB0
TRDGRC0	0	1	General register. Write the compare value.		TRDIOC0
TRDGRD0					TRDIOD0
TRDGRC0	1	1	Buffer register. Write the next compare value.		TRDIOA0
TRDGRD0					TRDIOB0
TRDGRC0	0	0	TRDIOA0 output control	(See 8.3.3 (2) Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi.)	TRDIOA0
TRDGRD0			TRDIOB0 output control		TRDIOB0

j = A, B, C, or D

Table 4.5 General Register Functions in the Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRA0	—	General register. The value of the TRD0 register can be read at input capture.	TRDIOA0
TRDGRB0			TRDIOB0
TRDGRC0	BFC0 = 0	General register. The value of the TRD0 register can be read at input capture.	TRDIOC0
TRDGRD0	BFD0 = 0		TRDIOD0
TRDGRC0	BFC0 = 1	Buffer register. The value of the TRD0 register can be read at input capture.	TRDIOA0
TRDGRD0	BFD0 = 1		TRDIOB0

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the port registers.

• Port Register 1 (P1)
Set port register 1.

Symbol	7	6	5	4	3	2	1	0
P1	P17	P16	P15	P14	P13	P12	P11	P10
Setting Value		x	0	0	x	x	x	x

Bit 5

P15	Output data control
0	Output 0
1	Output 1

Bit 4

P14	Output data control
0	Output 0
1	Output 1

• Port Mode Register 1 (PM1)
Set the P17 pin to input mode and pins P15 and P14 to output mode.

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
Setting Value	1	x	0	0	x	x	x	x

Bit 7

PM17	P17 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 5

PM15	P15 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 4

PM14	P14 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.6.6 Main Processing

Figure 4.8 shows the Main Processing.

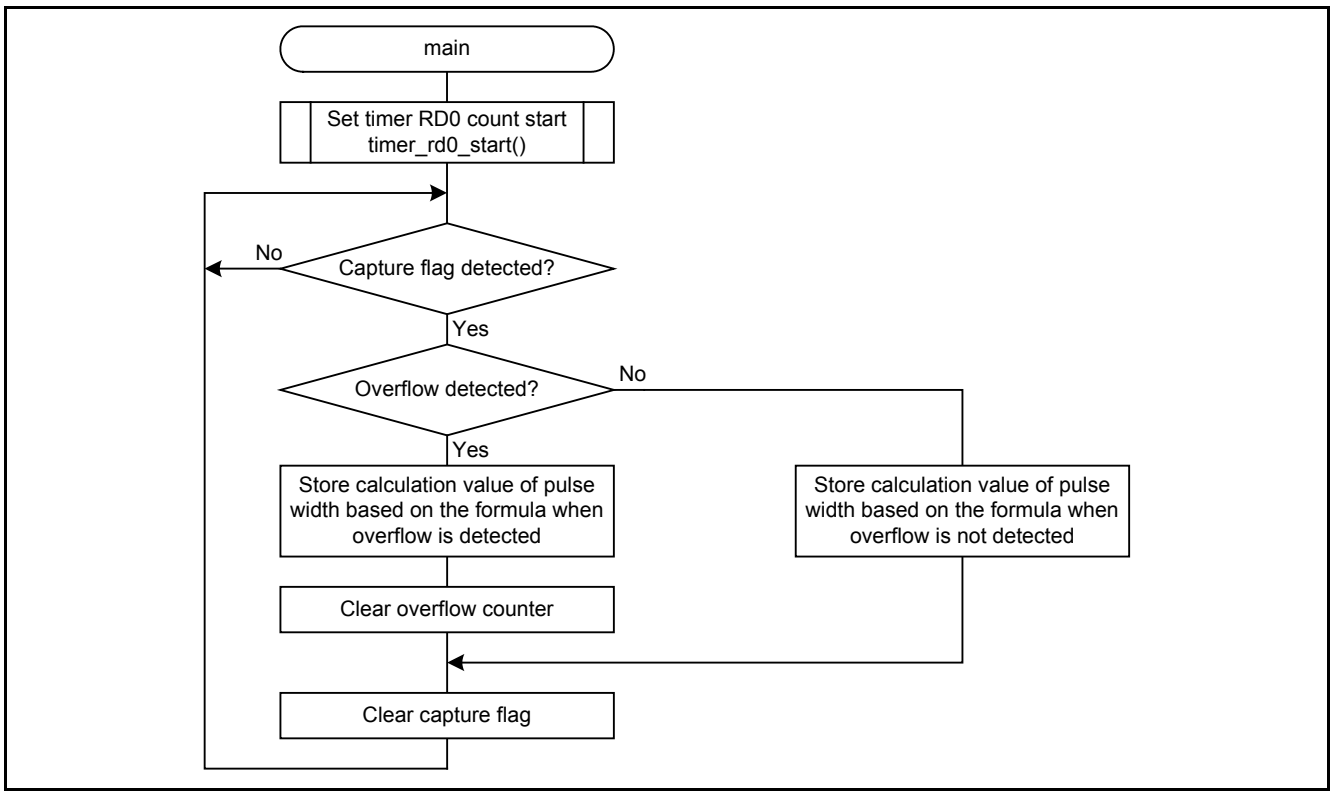


Figure 4.8 Main Processing

4.6.7 Timer RD Count Start Setting

Figure 4.9 shows the Timer RD0 Count Start Setting.

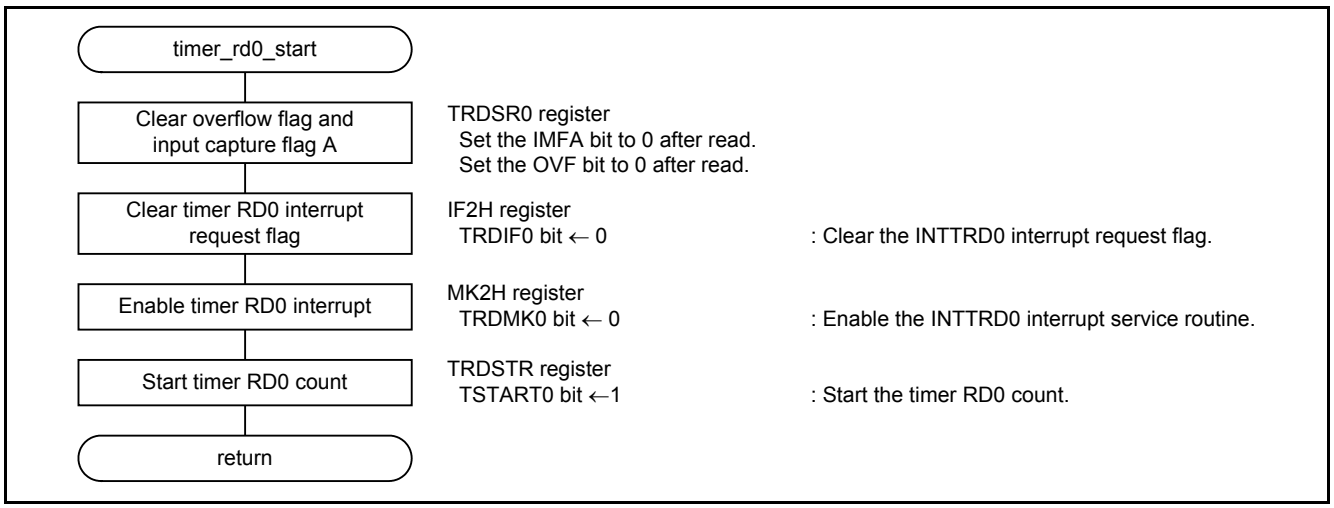


Figure 4.9 Timer RD0 Count Start Setting

Clear compare match flag A.

- Timer RD Status Register 0 (TRDSR0)
  Clear the overflow flag and input capture flag A after reading timer RD status register 0.

Symbol	7	6	5	4	3	2	1	0
TRDSR0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA
Setting Value	—	—	—	0	x	x	x	0

Bit 4

OVF	Overflow flag
[Source for setting to 0] Write 0 after reading. [Source for setting to 1] When the TRD0 register overflows	

Bit 0

IMFA	Input capture/compare match flag A
[Source for setting to 0] Write 0 after reading. [Source for setting to 1] Input edge of TRDIOA0 pin	

Clear the timer RD0 interrupt request flag.

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Enable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Enable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Start the timer RD0 count.

- Timer RD Mode Register (TRDSTR)
  Start the timer RD0 count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—	x		x	1

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.6.8 Timer RD0 Interrupt

Figure 4.10 shows the Timer RD0 Interrupt.

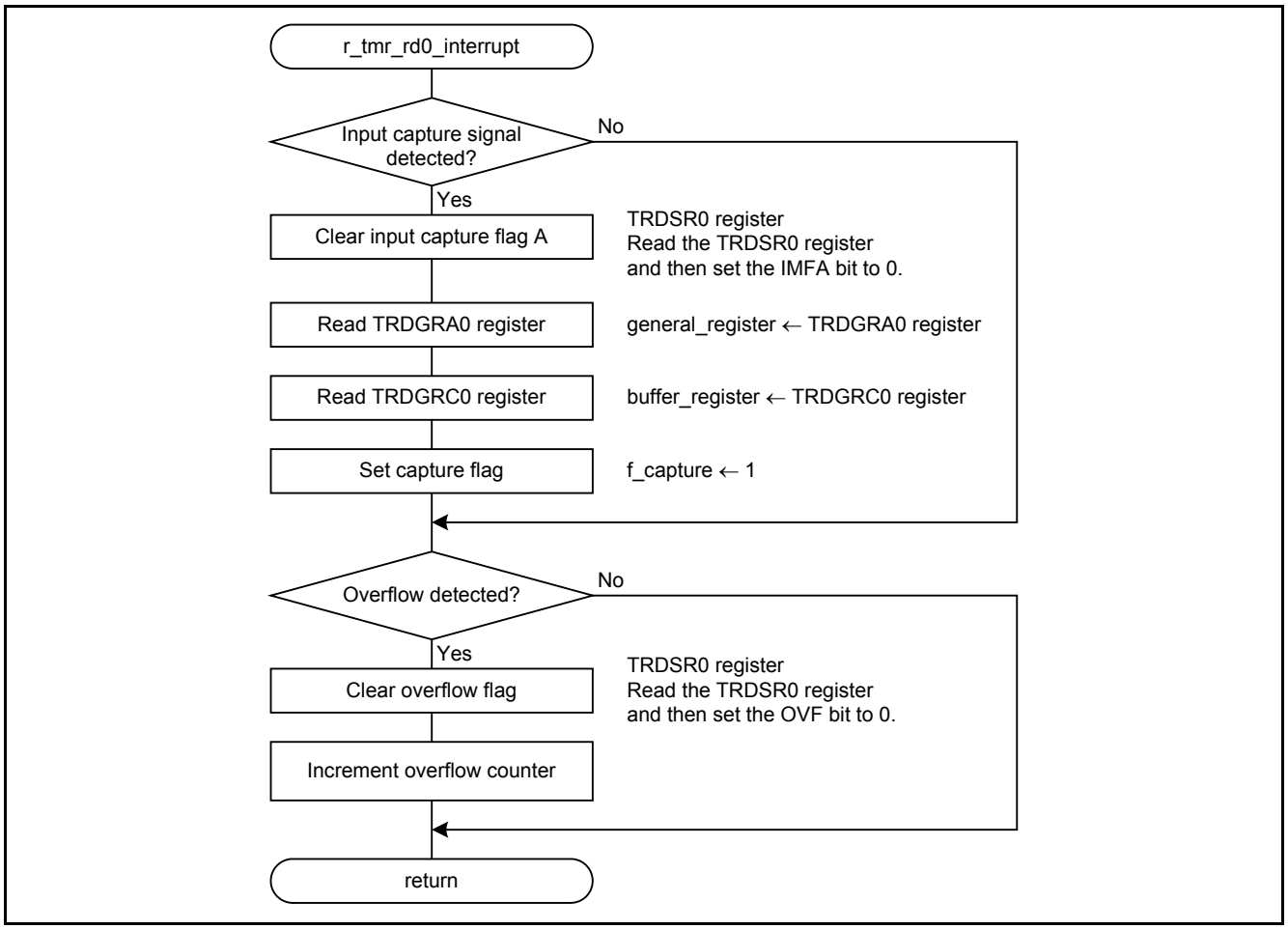


Figure 4.10 Timer RD0 Interrupt

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RL78/G14 Group User's Manual: Hardware Rev.0.02
RL78 Family User's Manual: Software Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14 Timer RD Using Input Capture Function and Output Compare Function

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 29, 2012	—	First edition issued
1.10	June 1, 2013	4	Fixed typo in Table 2.1
		5	Fixed typo in Figure 3.1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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