

## RL78/G14

R01AN0868EJ0110

Rev. 1.10

June 1, 2013

---

### Timer RD in PWM3 Mode

---

#### Abstract

This document describes a method to output a PWM waveform using timer RD of the RL78/G14 in PWM3 mode.

#### Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

## Contents

1. Specifications .....	3
2. Operation Confirmation Conditions .....	4
3. Hardware .....	5
3.1 Hardware Configuration .....	5
3.2 Pins Used .....	5
4. Software .....	6
4.1 Operation Overview .....	6
4.1.1 Output Waveform .....	6
4.2 Option-Setting Memory .....	8
4.3 Functions .....	8
4.4 Function Specifications .....	9
4.5 Flowcharts .....	11
4.5.1 Overall Flowchart .....	11
4.5.2 Initial Setting .....	11
4.5.3 Initial Setting of Peripheral Functions .....	12
4.5.4 Initial Setting of the CPU .....	12
4.5.5 Initial Setting of Timer RD .....	13
4.5.6 Main Processing .....	28
4.5.7 Timer RD Count Start Setting .....	28
4.5.8 Timer RD0 Interrupt .....	30
5. Sample Code .....	31
6. Reference Documents .....	31

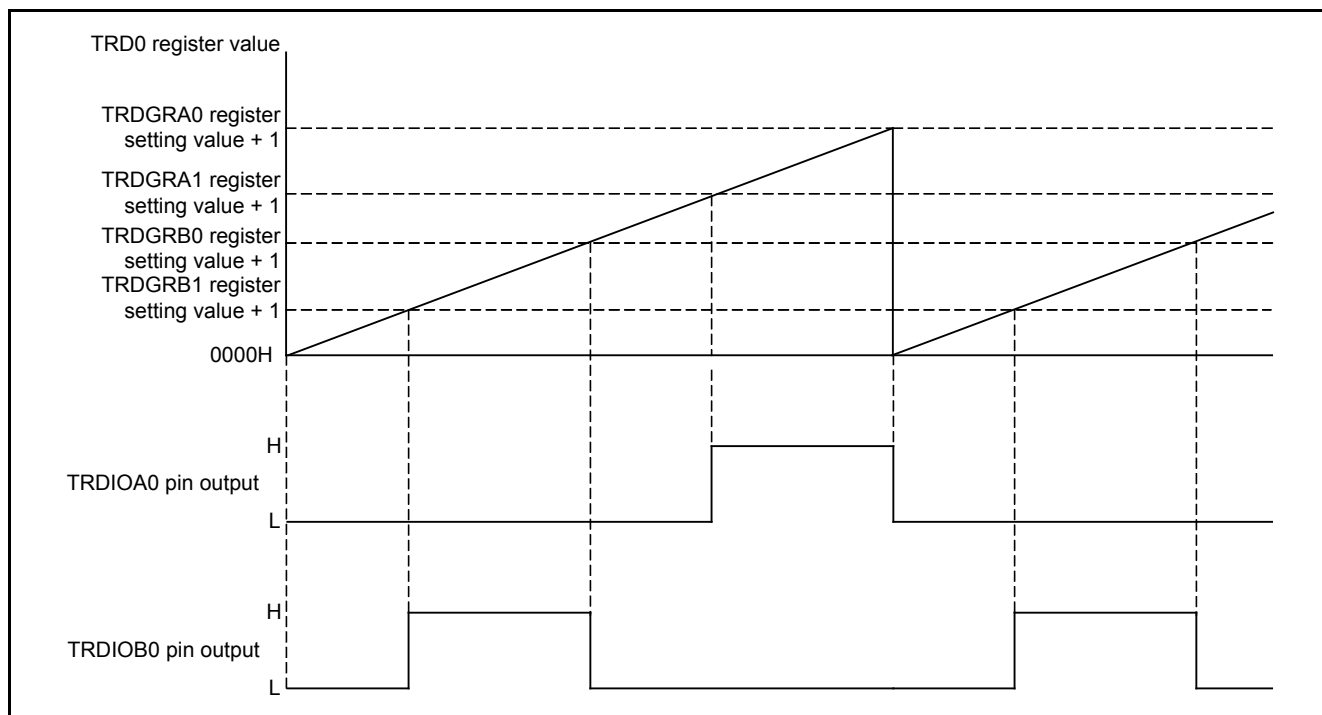
## 1. Specifications

Two PWM waveforms with 200  $\mu$ s periods are output.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Output Timing Diagram.

**Table 1.1 Peripheral Function and Its Application**

Peripheral Function	Application
Timer RD (timer RD0, timer RD1)	PWM waveform output



**Figure 1.1 Output Timing Diagram**

## 2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

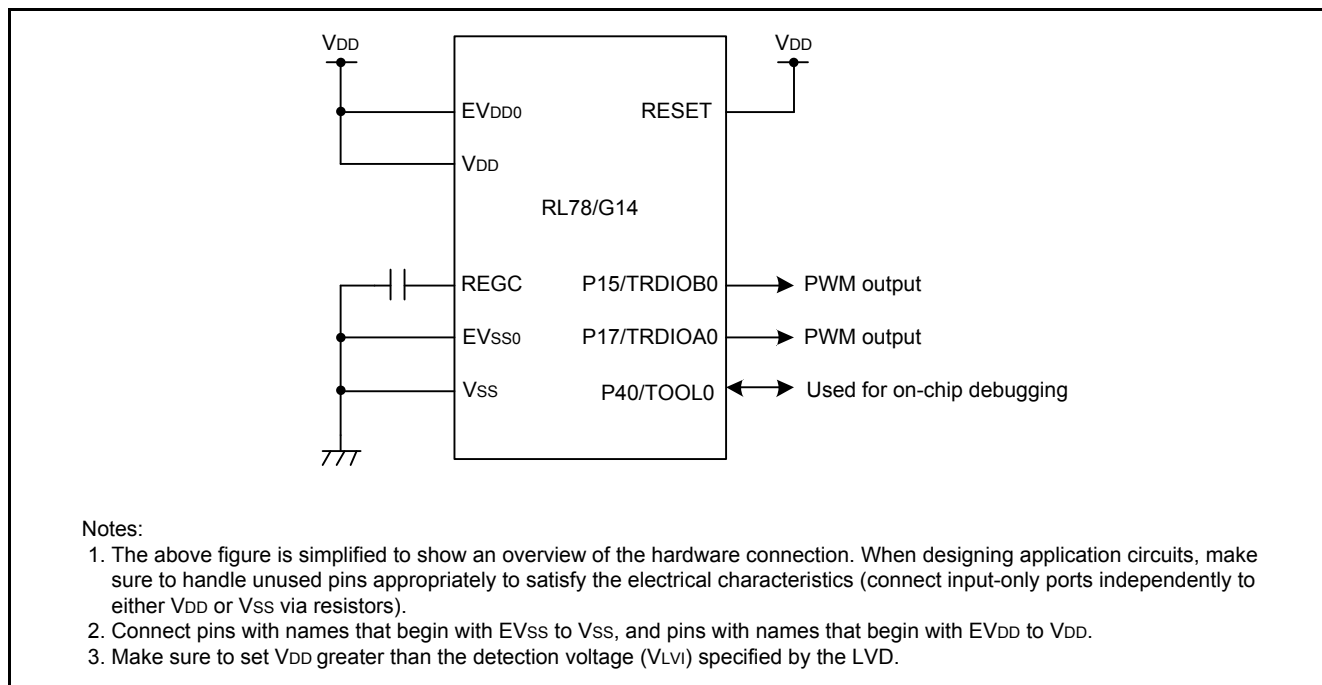
**Table 2.1 Operation Confirmation Conditions**

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	<ul style="list-style-type: none"><li>• High-speed on-chip oscillator clock (fHOCO): 16 MHz (typical)</li><li>• CPU/peripheral hardware clock (fCLK): 16 MHz</li></ul>
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (VLVI): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.01.00
C compiler	Renesas Electronics Corporation CA78K0R V1.30
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.01

### 3. Hardware

#### 3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.



**Figure 3.1 Hardware Configuration**

#### 3.2 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

**Table 3.1 Pins Used and Their Functions**

Pin Name	I/O	Function
P15/TRDIOB0	Output	PWM output
P17/TRDIOA0	Output	PWM output

## 4. Software

### 4.1 Operation Overview

Two PWM waveforms with 200  $\mu$ s periods are output using PWM3 mode.

Output signals are as follows:

- TRDIOA0 pin: Low inactive level period (140  $\mu$ s)  $\rightarrow$  High active level period (60  $\mu$ s)
- TRDIOB0 pin: Low inactive level period (40  $\mu$ s)  $\rightarrow$  High active level period (60  $\mu$ s)  $\rightarrow$  Low inactive level period (100  $\mu$ s)

The timer RD settings are shown below.

Settings:

- Use fCLK (16 MHz) as the count source.
- Clear the TRD0 register at the compare match with the TRDGRA0 register.
- Continue counting the TRD0 register after the compare match with the TRDGRA0 register.
- Use the TRDGRC1 register as the buffer register of the TRDGRA1 register.
- Use the TRDGRD1 register as the buffer register of the TRDGRB1 register.
- Use the TRDGRC0 register as the buffer register of the TRDGRA0 register.
- Use the TRDGRD0 register as the buffer register of the TRDGRB0 register.
- Enable output for pins TRDIOA0 and TRDIOB0.
- Disable output for pins TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.
- Select TRDIOA0 and TRDIOB0 pin output levels as high active level and the initial output level as low inactive level.
- Do not use the pulse output forced cutoff input function.
- Enable the compare match interrupt for registers TRD0 and TRDGRA0.

#### 4.1.1 Output Waveform

Below is a description for calculating the PWM period and PWM waveform output from each pin.

##### (1) PWM period

Calculate the PWM period as follows:

$$\begin{aligned} 200 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA0} + 1) \\ &= 62.5 \text{ ns} \times 3200 \end{aligned}$$

##### (2) TRDIOA0 pin output

Calculate the high active level period and low inactive level period of the PWM waveform output from the TRDIOA0 pin as follows:

$$\begin{aligned} \text{High active level period: } 60 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA0} + 1) - 1/16 \text{ MHz} \times (\text{TRDGRA1} + 1) \\ &= 62.5 \text{ ns} \times 3200 - 62.5 \text{ ns} \times 2240 \end{aligned}$$

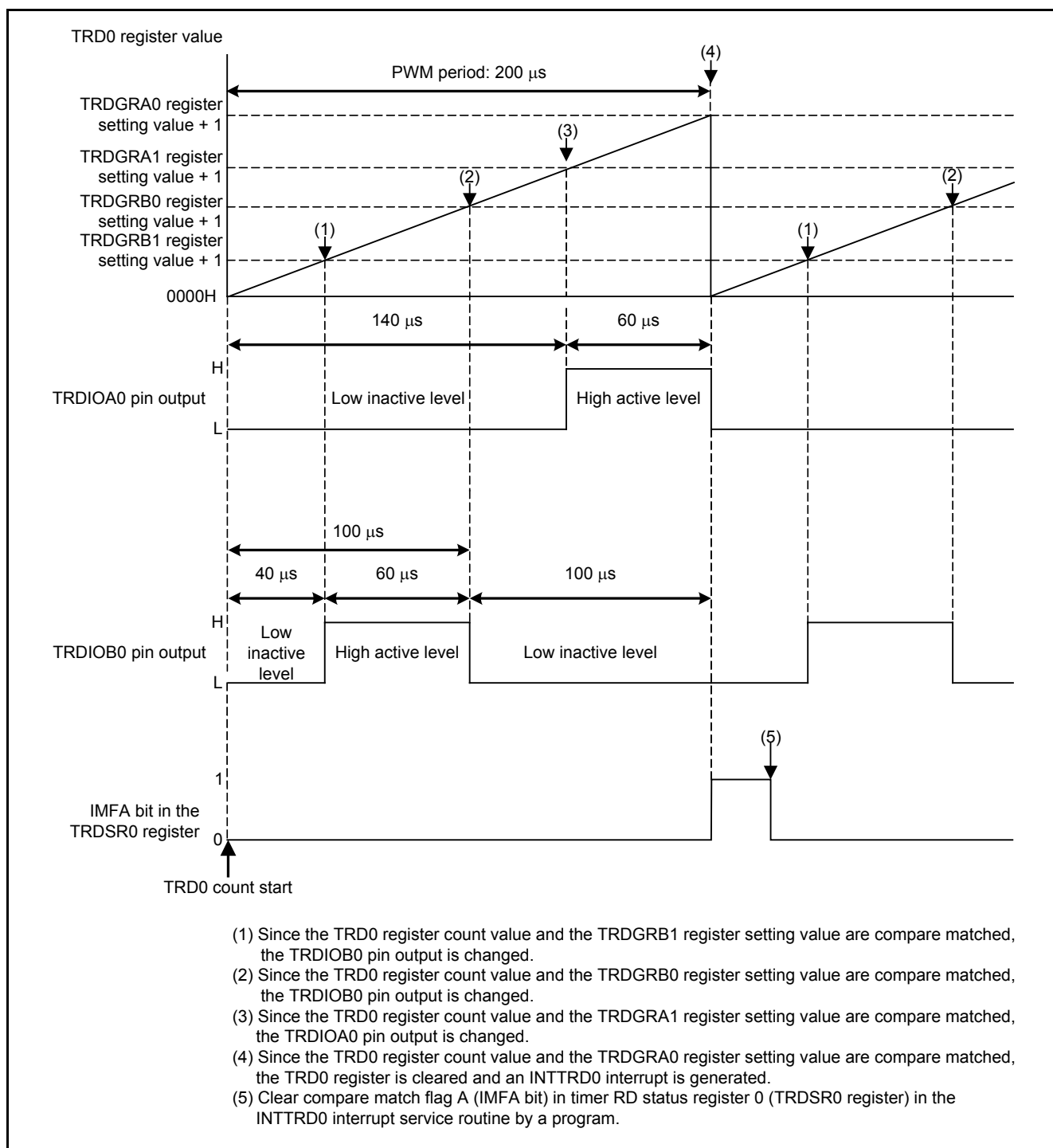
$$\begin{aligned} \text{Low inactive level period: } 140 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA1} + 1) \\ &= 62.5 \text{ ns} \times 2240 \end{aligned}$$

##### (3) Calculate the high active level period and low inactive level period of the PWM waveform output from the TRDIOB0 pin as follows:

$$\begin{aligned} \text{High active level period: } 60 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRB0} + 1) - 1/16 \text{ MHz} \times (\text{TRDGRB1} + 1) \\ &= 62.5 \text{ ns} \times 1600 - 62.5 \text{ ns} \times 640 \end{aligned}$$

$$\begin{aligned} \text{Low inactive level period (between TRD0 count start and high active level period start)} \\ : 40 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRB1} + 1) \\ &= 62.5 \text{ ns} \times 640 \end{aligned}$$

Figure 4.1 shows the PWM Output Waveform.



**Figure 4.1 PWM Output Waveform**

## 4.2 Option-Setting Memory

Table 4.1 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

**Table 4.1 Option-Setting Memory Configured in the Sample Code**

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

## 4.3 Functions

Table 4.2 lists the Functions.

**Table 4.2 Functions**

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of the CPU
R_TMR_RD0_Create	Initial setting of timer RD
main	Main processing
timer_rd0_start	Timer RD count start setting
r_tmr_rd0_interrupt	Timer RD0 interrupt

#### 4.4 Function Specifications

The following tables list the sample code function specifications.

<b>hdwinit</b>	
<b>Outline</b>	Initial setting
<b>Header</b>	None
<b>Declaration</b>	void hdwinit(void)
<b>Description</b>	Perform the initial setting of peripheral functions.
<b>Argument</b>	None
<b>Return Value</b>	None

<b>R_Systeminit</b>	
<b>Outline</b>	Initial setting of peripheral functions
<b>Header</b>	None
<b>Declaration</b>	void R_Systeminit(void)
<b>Description</b>	Perform the initial setting of peripheral functions used in this document.
<b>Argument</b>	None
<b>Return Value</b>	None

<b>R_CGC_Create</b>	
<b>Outline</b>	Initial setting of the CPU
<b>Header</b>	None
<b>Declaration</b>	void R_CGC_Create(void)
<b>Description</b>	Perform the initial setting of the CPU.
<b>Argument</b>	None
<b>Return Value</b>	None

<b>R_TMR_RD0_Create</b>	
<b>Outline</b>	Initial setting of timer RD
<b>Header</b>	None
<b>Declaration</b>	void R_TMR_RD0_Create(void)
<b>Description</b>	Perform the initial setting to use PWM3 mode of timer RD.
<b>Argument</b>	None
<b>Return Value</b>	None

<b>main</b>	
<b>Outline</b>	Main processing
<b>Header</b>	None
<b>Declaration</b>	void main(void)
<b>Description</b>	Perform main processing.
<b>Argument</b>	None
<b>Return Value</b>	None

---

**timer\_rd0\_start**

---

<b>Outline</b>	Timer RD count start setting
<b>Header</b>	None
<b>Declaration</b>	void timer_rd0_start(void)
<b>Description</b>	Perform timer RD count start setting.
<b>Argument</b>	None
<b>Return Value</b>	None

---

**r\_tmr\_rd0\_interrupt**

---

<b>Outline</b>	Timer RD0 interrupt
<b>Header</b>	None
<b>Declaration</b>	void r_tmr_rd0_interrupt(void)
<b>Description</b>	<ul style="list-style-type: none"><li>• Perform timer RD0 interrupt service routine.</li><li>• Clear compare match flag A.</li></ul>
<b>Argument</b>	None
<b>Return Value</b>	None

4.5 Flowcharts

4.5.1 Overall Flowchart

Figure 4.2 shows the Overall Flowchart.

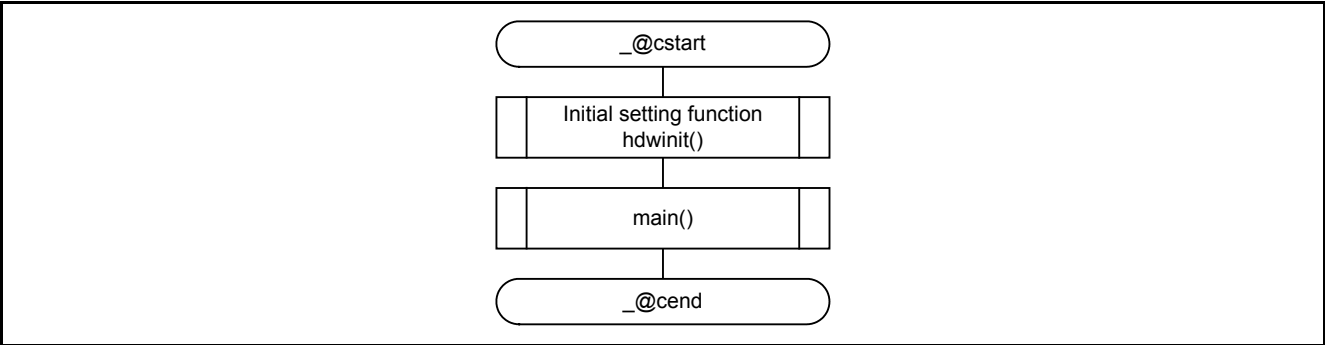


Figure 4.2 Overall Flowchart

4.5.2 Initial Setting

Figure 4.3 shows the Initial Setting.

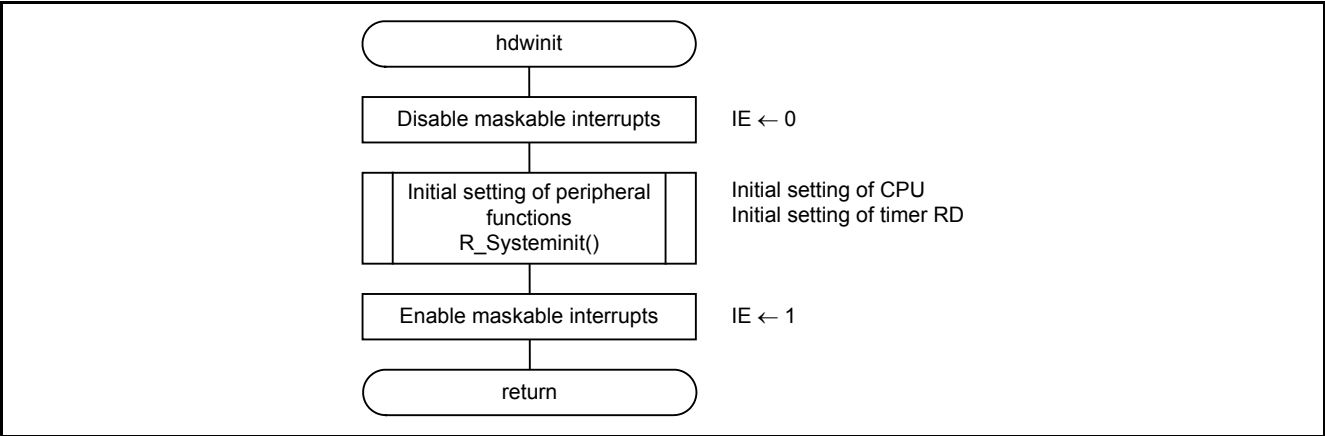
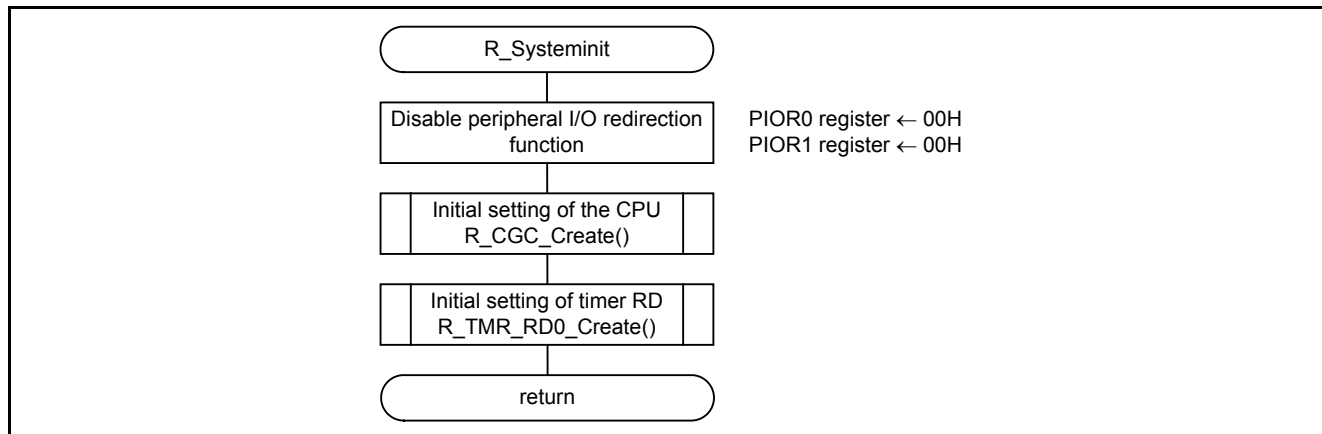


Figure 4.3 Initial Setting

### 4.5.3 Initial Setting of Peripheral Functions

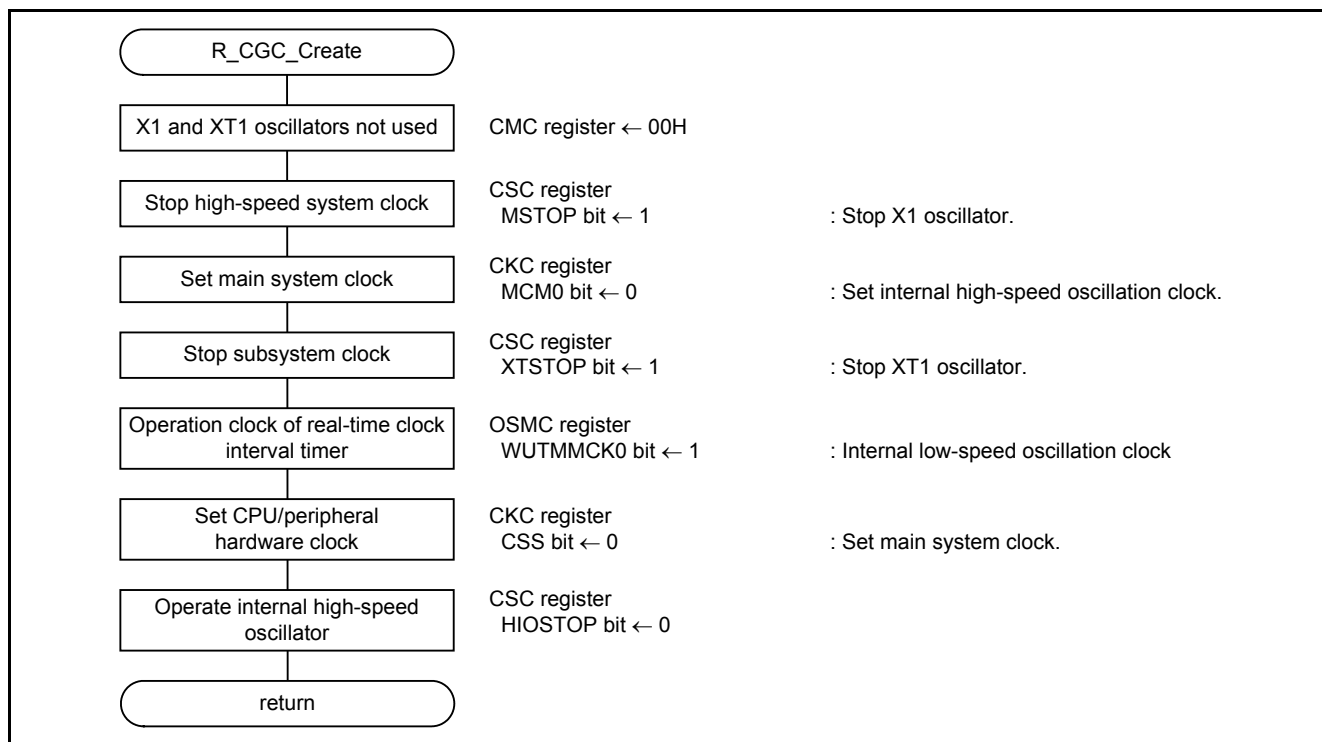
Figure 4.4 shows the Initial Setting of Peripheral Functions.



**Figure 4.4 Initial Setting of Peripheral Functions**

### 4.5.4 Initial Setting of the CPU

Figure 4.5 shows the Initial Setting of the CPU.



**Figure 4.5 Initial Setting of the CPU**

#### 4.5.5 Initial Setting of Timer RD

Figure 4.6 and Figure 4.7 show the Initial Setting of Timer RD.

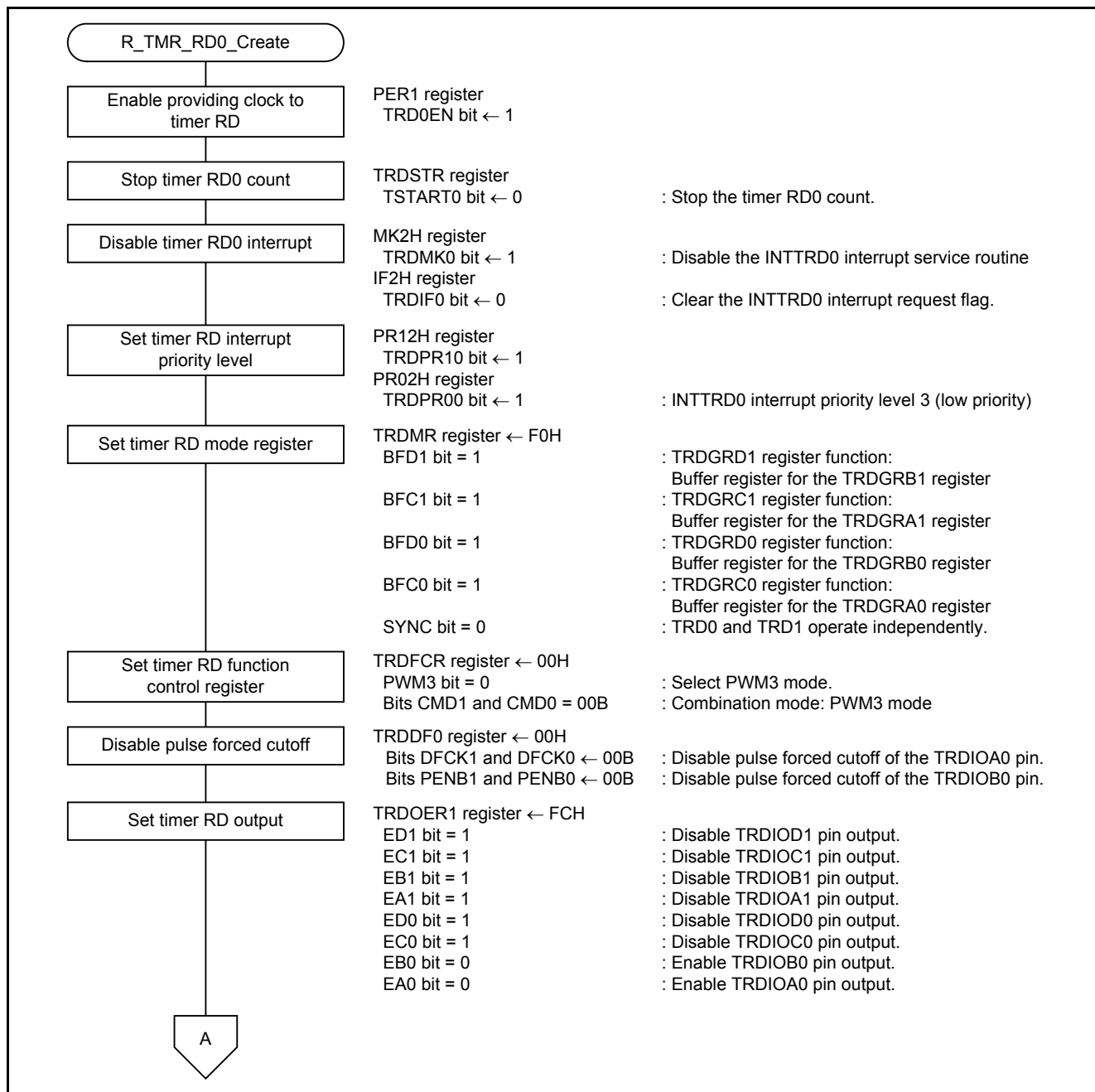


Figure 4.6 Initial Setting of Timer RD (1/2)



Enable providing a clock to timer RD.

- Peripheral Enable Register 1 (PER1)  
Enable providing a clock to timer RD.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	COMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	x	x	1	x	—	—	x

Bit 4

TRD0EN	Control of timer RD input clock supply
0	Stops input clock supply. • SFR used by timer RD cannot be written. • Timer RD is in the reset status.
1	Enables input clock supply. • SFR used by timer RD can be read and written.

Stop the timer RD0 count.

- Timer RD Mode Register (TRDSTR)  
Stop the timer RD0 count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—	x		x	0

Bit 2

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	Count continues after compare match with TRDGRA0 register

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)

Disable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	x	1	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt Request Flag Register (IF2H)

Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD interrupt priority level.

- Priority Specification Flag Registers (PR02H and PR12H)  
Set to level 3 (low priority).

Symbol	7	6	5	4	3	2	1	0
PR02H	FLPR0	IICAPR01	1	SREPR03 TMPR013H	TRGPR0	TRDPR01	TRDPR00	PPR011 CMPPR01
Setting Value	x	x	—	x	x	x	1	x

Symbol	7	6	5	4	3	2	1	0
PR12H	FLPR1	IICAPR11	1	SREPR13 TMPR113H	TRGPR1	TRDPR11	TRDPR10	PPR111 CMPPR11
Setting Value	x	x	—	x	x	x	1	x

TRDPR10	TRDPR00	Priority level selection
0	0	Specify level 0 (high priority level).
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Set the timer RD mode register.

- Timer RD Mode Register (TRDMR)  
Use registers TRDGRC0, TRDGRD0, TRDGRC1, and TRDGRD1 as the buffer registers.

Symbol	7	6	5	4	3	2	1	0
TRDMR	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
Setting Value	1	1	1	1	—	—	—	0

Bit 7

BFD1	TRDGRD1 register function select
0	General register
1	Buffer register for TRDGRB1 register

Bit 6

BFC1	TRDGRC1 register function select
0	General register
1	Buffer register for TRDGRA1 register

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 5

BFD0	TRDGRD0 register function select
0	General register
1	Buffer register for TRDGRB0 register

Bit 4

BFC0	TRDGRC0 register function select
0	General register
1	Buffer register for TRDGRA0 register

Bit 0

SYNC	Timer RD synchronous
0	TRD0 and TRD1 operate independently
1	TRD0 and TRD1 operate synchronously

Set to 0 in PWM3 mode.

Set the timer RD function control register.

- Timer RD Function Control Register (TRDFCR)  
Set PWM3 mode. Set PWM3 mode as a combination mode.

Symbol	7	6	5	4	3	2	1	0
TRDFCR	PWM3	STCLK	0	0	OLS1	OLS0	CMD1	CMD0
Setting Value	0	x	—	—	x	x	0	0

Bit 7

PWM3	PWM3 mode select
<ul style="list-style-type: none"> <li>• In the timer mode, set to 1 (other than PWM3 mode).</li> <li>• In PWM3 mode, set to 0 (PWM3 mode).</li> <li>• Disabled in reset synchronous and complementary PWM modes.</li> </ul>	

Bits 1 and 0

CMD1	CMD0	Combination mode select						
<ul style="list-style-type: none"> <li>• In timer and PWM3 modes, set to 00B (timer mode or PWM3 mode).</li> <li>• In reset synchronous PWM mode, set to 01B (reset synchronous PWM mode).</li> <li>• In complementary PWM mode, CMD1 CMD0               <table> <tr> <td>1</td><td>0:</td><td>Complementary PWM mode (transfer from the buffer register to the general register when TRD1 underflows)</td></tr> <tr> <td>1</td><td>1:</td><td>Complementary PWM mode (transfer from the buffer register to the general register at compare match between registers TRD0 and TRDGRA0)</td></tr> </table> </li> </ul>			1	0:	Complementary PWM mode (transfer from the buffer register to the general register when TRD1 underflows)	1	1:	Complementary PWM mode (transfer from the buffer register to the general register at compare match between registers TRD0 and TRDGRA0)
1	0:	Complementary PWM mode (transfer from the buffer register to the general register when TRD1 underflows)						
1	1:	Complementary PWM mode (transfer from the buffer register to the general register at compare match between registers TRD0 and TRDGRA0)						
Other than the above: Do not set.								

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable pulse forced cut-off.

- Timer RD Digital Filter Function Select Register 0 (TRDDF0)  
Disable pulse forced cut-off of pins TRDIOA0 and TRDIOB0.

Symbol	7	6	5	4	3	2	1	0
TRDDF0	DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
Setting Value	0	0	0	0	x	x	x	x

Bits 7 and 6

DFCK1	DFCK0	TRDIOA0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Bits 5 and 4

PENB1	PENB0	TRDIOB0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Set timer RD output.

- Timer RD Output Master Enable Register 1 (TRDOER1)  
Enable output of pins TRDIOA0 and TRDIOB0, and disable output of pins TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.

Symbol	7	6	5	4	3	2	1	0
TRDOER1	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
Setting Value	1	1	1	1	1	1	0	0

Bit 7

ED1	TRDIOD1 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Set to 1 in PWM3 mode.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 6

EC1	TRDIOC1 output disable
0	Output enabled
1	Output disabled (TRDIOC1 pin functions as an I/O port.)

Set to 1 in PWM3 mode.

Bit 5

EB1	TRDIOB1 output disable
0	Output enabled
1	Output disabled (TRDIOB1 pin functions as an I/O port.)

Set to 1 in PWM3 mode.

Bit 4

EA1	TRDIOA1 output disable
0	Output enabled
1	Output disabled (TRDIOA1 pin functions as an I/O port.)

Set to 1 in PWM3 mode.

Bit 3

ED0	TRDIOD0 output disable
0	Output enabled
1	Output disabled (TRDIOD0 pin functions as an I/O port.)

Set to 1 in PWM3 mode.

Bit 2

EC0	TRDIOC0 output disable
0	Output enabled
1	Output disabled (TRDIOC0 pin functions as an I/O port.)

Set to 1 in PWM3 mode.

Bit 1

EB0	TRDIOB0 output disable
0	Output enabled
1	Output disabled (TRDIOB0 pin functions as an I/O port.)

Bit 0

EA0	TRDIOA0 output disable
0	Output enabled
1	Output disabled (TRDIOA0 pin functions as an I/O port.)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Select output levels.

- Timer RD Output Control Register (TRDOCR)

Set low for initial output of pins TRDIOA0 and TRDIOB0, and high for the active level.

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Setting Value	x	x	x	x	x	x	0	0

Bit 1

TOB0	TRDIOB0 initial output level select
0	Low initial output, high active level, high output at TRDGRB1 compare match, and low output at TRDGRB0 compare match
1	High initial output, low active level, low output at TRDGRB1 compare match, and high output at TRDGRB0 compare match

Bit 0

TOA0	TRDIOA0 initial output level select
0	Low initial output, high active level, high output at TRDGRA1 compare match, and low output at TRDGRA0 compare match
1	High initial output, low active level, low output at TRDGRA1 compare match, and high output at TRDGRA0 compare match

Set timer RD control register 0.

- Timer RD Control Register 0 (TRDCR0)

Set the timing to clear the TRD0 register at the compare match with the TRDGRA0 register. Set fCLK to the count source of timer RD0.

Symbol	7	6	5	4	3	2	1	0
TRDCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
Setting Value	0	0	1	x	x	0	0	0

Bits 7 to 5

CCLR2	CCLR1	CCLR0	TRD0 counter clear select
Set to 001B (TRD0 register is cleared at compare match with TRDGRA0 register).			

Bits 2 to 0

TCK2	TCK1	TCK0	Count source select
0	0	0	fCLK, fHOCO
0	0	1	fCLK/2
0	1	0	fCLK/4
0	1	1	fCLK/8
1	0	0	fCLK/32
1	0	1	Do not set.
1	1	0	Do not set.
1	1	1	Do not set.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the compare match interrupt.

- Timer RD Interrupt Enable Register 0 (TRDIER0)

Set the IMFA bit to enable the interrupt (IMIA).

Symbol	7	6	5	4	3	2	1	0
TRDIER0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
Setting Value	—	—	—	0	0	0	0	1

Bit 4

OVIE	Overflow/underflow interrupt enable
0	Interrupt (OVI) by bits OVF and UDF disabled
1	Interrupt (OVI) by bits OVF and UDF enabled

Bit 3

IMIED	Input capture/compare match interrupt enable D
0	Interrupt (IMID) by the IMFD bit is disabled
1	Interrupt (IMID) by the IMFD bit is enabled

Bit 2

IMIEC	Input capture/compare match interrupt enable C
0	Interrupt (IMIC) by the IMFC bit is disabled
1	Interrupt (IMIC) by the IMFC bit is enabled

Bit 1

IMIEB	Input capture/compare match interrupt enable B
0	Interrupt (IMIB) by the IMFB bit is disabled
1	Interrupt (IMIB) by the IMFB bit is enabled

Bit 0

IMIEA	Input capture/compare match interrupt enable A
0	Interrupt (IMIA) by the IMFA bit is disabled
1	Interrupt (IMIA) by the IMFA bit is enabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the PWM period.

- Timer RD General Register A0 (TRDGRA0)

Set the PWM period to 200  $\mu$ s.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRA0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRA0 register function in PWM3 mode.	0000H to FFFFH

Set the PWM output changing point.

- Timer RD General Register B0 (TRDGRB0)

Set this register after 100  $\mu$ s from the count start to change the output of the TRDIOB0 pin.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRB0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRB0 register function in PWM3 mode.	0000H to FFFFH

- Timer RD General Register A1 (TRDGRA1)

Set this register after 140  $\mu$ s from the count start to change the output of the TRDIOA0 pin.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRA1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRA1 register function in PWM3 mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Timer RD General Register B1 (TRDGRB1)

Set this register after 40  $\mu$ s from the count start to change the output of the TRDIOB0 pin.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRB1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRB1 register function in PWM3 mode.	0000H to FFFFH

### Set the buffer register

- Timer RD General Register C0 (TRDGRC0)

Set C7FH to the buffer register (TRDGRC0) of the TRDGRA0 register.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRC0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRC0 register function in PWM3 mode.	0000H to FFFFH

- Timer RD General Register D0 (TRDGRD0)

Set 63FH to the buffer register (TRDGRD0) of the TRDGRB0 register.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRD0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRD0 register function in PWM3 mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Timer RD General Register C1 (TRDGRC1)

Set 8BFH to the buffer register (TRDGRC1) of the TRDGRA1 register.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRC1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRC1 register function in PWM3 mode.	0000H to FFFFH

- Timer RD General Register D1 (TRDGRD1)

Set 27FH to the buffer register (TRDGRD1) of the TRDGRB1 register.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDGRD1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRD1 register function in PWM3 mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Table 4.3 General Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	—	General register. Set the PWM period. Setting range: $\geq$ Value set in TRDGRA1 register	TRDIOA0
TRDGRA1		General register. Set the changing point (active level timing) of PWM output Setting range: $\leq$ Value set in TRDGRA0 register	
TRDGRB0		General register. Set the changing point (the timing for returning to initial output level) of PWM output. Setting range: $\geq$ Value set in TRDGRB1 register and $\leq$ Value set in TRDGRA0 register	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output Setting range: $\leq$ Value set in TRDGRB0 register	
TRDGRC0	BFC0 = 0	(Not used in PWM3 mode.)	—
TRDGRC1	BFC1 = 0		
TRDGRD0	BFD0 = 0		
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period Setting range: $\geq$ Value set in TRDGRC1 register	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output Setting range: $\leq$ Value set in TRDGRC0 register	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output Setting range: $\geq$ Value set in TRDGRD1 register and $\leq$ Value set in TRDGRC0 register	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output Setting range: $\leq$ Value set in TRDGRD0 register	

Set the port registers.

- Port Register 1 (P1)

Set port register 1.

Symbol	7	6	5	4	3	2	1	0
P1	P17	P16	P15	P14	P13	P12	P11	P10
Setting Value	0	x	0	x	x	x	x	x

Bit 7

P17	Output data control
0	Output 0
1	Output 1

Bit 5

P15	Output data control
0	Output 0
1	Output 1

- Port Mode Register 1 (PM1)

Set pins P17 and P15 to output mode.

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
Setting Value	0	x	0	x	x	x	x	x

Bit 7

PM17	P17 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 5

PM15	P15 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.5.6 Main Processing

Figure 4.8 shows the Main Processing.

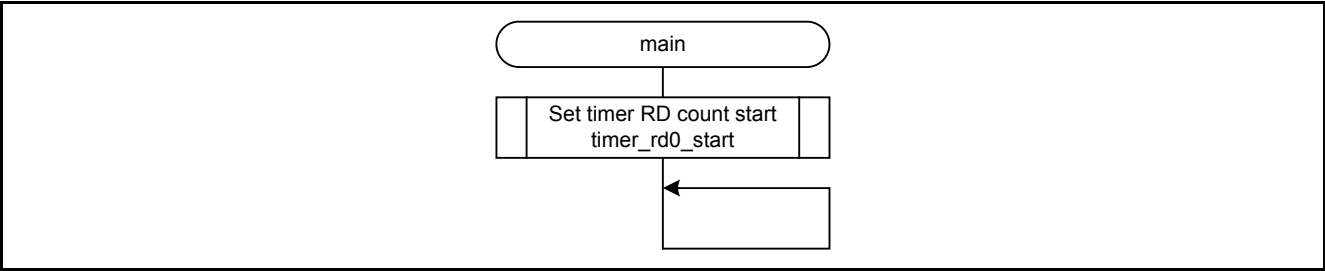


Figure 4.8 Main Processing

4.5.7 Timer RD Count Start Setting

Figure 4.9 shows the Timer RD Count Start Setting.

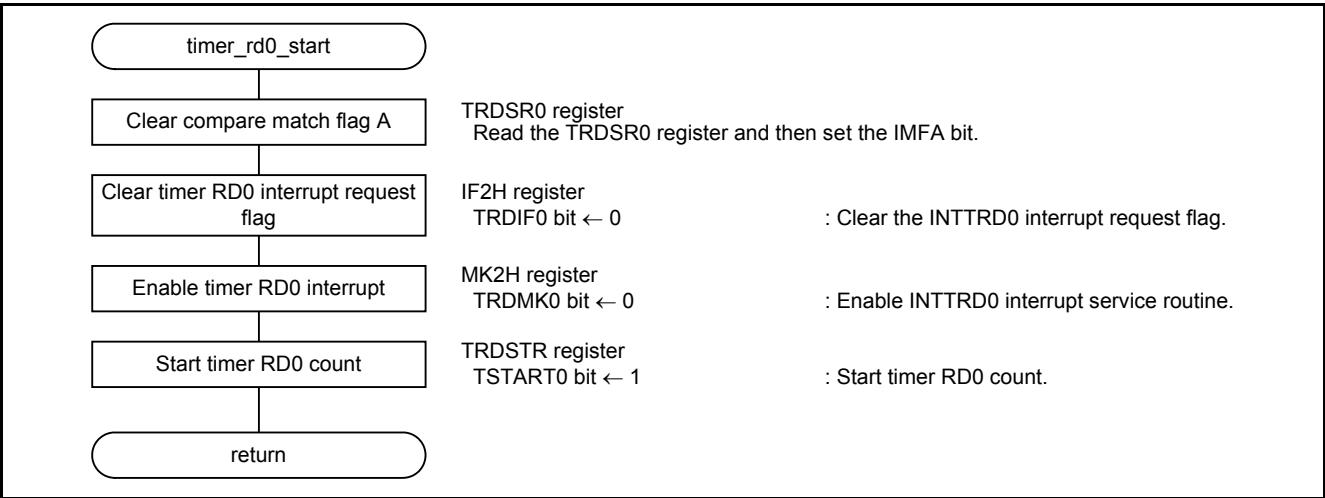


Figure 4.9 Timer RD Count Start Setting

Clear compare match flag A.

- Timer RD Status Register 0 (TRDSR0)

Clear compare match flag A after reading timer RD status register 0.

Symbol	7	6	5	4	3	2	1	0
TRDSR0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA
Setting Value	—	—	—	x	x	x	x	0

Bit 0

IMFA	Input capture/compare match flag A
[Source for setting to 0] Write 0 after reading. [Source for setting to 1] When the values of TRD0 and TRDGRA0 match.	

Clear the timer RD0 interrupt request flag.

- Interrupt Request Flag Register (IF2H)

Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAI1F1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMP1F1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Enable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)

Enable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Start the timer RD0 count.

- Timer RD Mode Register (TRDSTR)  
Start the timer RD0 count.

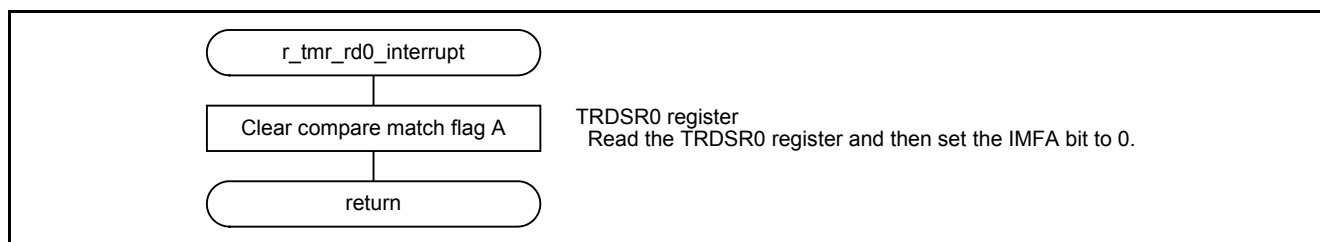
Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—	x		x	1

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

#### 4.5.8 Timer RD0 Interrupt

Figure 4.10 shows the Timer RD0 Interrupt.



**Figure 4.10 Timer RD0 Interrupt**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

## 5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

## 6. Reference Documents

User's Manual: Hardware

RL78/G14 Group User's Manual: Hardware Rev.0.02

RL78 Family User's Manual: Software Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

## Website and Support

Renesas Electronics website

<http://www.renesas.com>

Inquiries

<http://www.renesas.com/contact/>

<b>REVISION HISTORY</b>	RL78/G14 Timer RD in PWM3 Mode
-------------------------	--------------------------------

Rev.	Date	Description	
		Page	Summary
<b>1.00</b>	<b>Jan. 31, 2012</b>	—	First edition issued
<b>1.10</b>	<b>June 1, 2013</b>	<b>4</b>	Fixed typo in Table 2.1
		<b>5</b>	Fixed typo in Figure 3.1

All trademarks and registered trademarks are the property of their respective owners.
---

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
  3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.  
Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
  6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
  11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



### SALES OFFICES

### Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

**Renesas Electronics America Inc.**  
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700, Fax: +44-1628-651-804

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**  
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141