RL78/G14

Sine Waveform Output by Using D/A Converter CC-RL

Introduction

This document describes a method to output sine waveform with analog voltage using the D/A converter in the RL78/G14 Group MCU, DTC (Data Transfer Controller), and ELC (Event Link Controller).

Target Device

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Outputs analog voltage from the ANO0 pin using the D/A converter. Output for the analog voltage starts at 0.0 V. The output level changes every 200 us and the sine waveform of 50 Hz (1 cycle: 20 ms).

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Analog Voltage Output Waveform.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	**Application**
D/A converter 0 (hereinafter referred to as DAC0)	Output the analog voltage
Timer array unit 0 (hereinafter referred to as TAU0)	Generate a period to change the analog voltage
Data Transfer Controller (DTC)	Data transmission from RAM to SFR
Event Link Controller (ELC)	Conversion start trigger of D/A converter

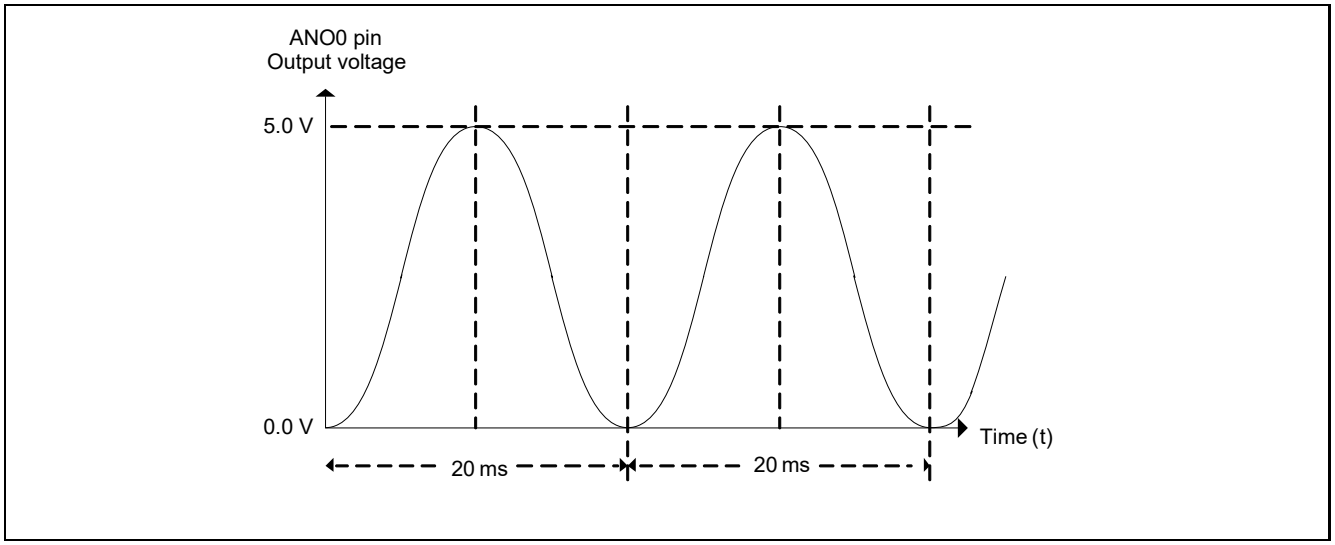

Figure 1.1 Analog Voltage Output Waveform

2. Operation Check Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104PJA)
Operating frequency	• High-speed on-chip oscillator clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run at a voltage range of 2.9 V to 5.5 V.) LVD operation(V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.3.2447 IAR Systems

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.

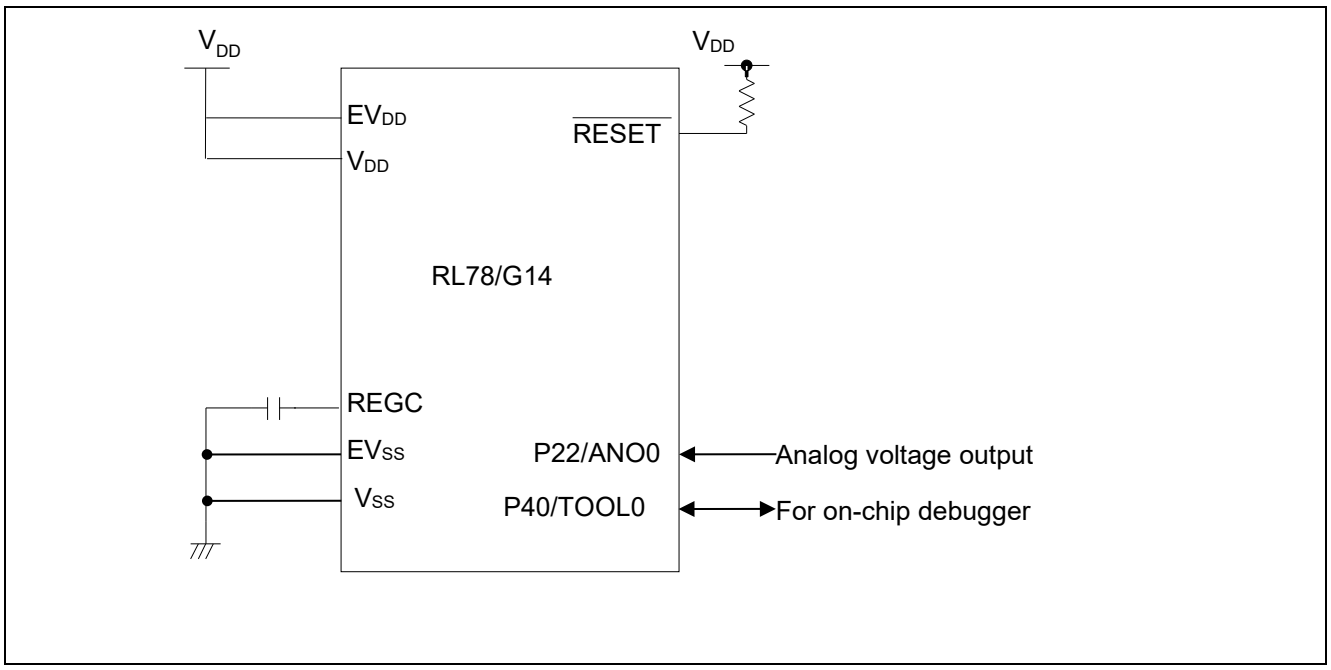

Figure 3.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly.
When designing and implementing an actual circuit, provide proper pin treatment and make sure that the
hardware's electrical specifications are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

3.2 Pin Used

Table 3.1 lists the Pin Used and Its Function.

Table 3.1 Pin Used and Its Function

Pin Name	I/O	Function
P22/ANO0	Output	Output the analog voltage

4. Software

4.1 Operation Overview

Outputs the analog voltage from the ANO0 pin using DAC0. The analog output voltage immediately after DAC0 conversion operation is enabled is 0.0 V. Uses TAU0 channel 0 (TAU00) in interval timer mode and generates interrupts every 200 us. Starts the analog output voltage conversion of DAC0 which uses ELC by TAU00 count end interrupt. Starts DTC at the same time, and transmits the value stored in the D/A conversion value table to the D/A conversion value setting register 0 (DACS0).

The D/A conversion value table:

It is a table that switches values every 200 us from 0.0 V to 5.0 V of the analog output voltage and outputs the sine waveform of 1 cycle: 50 Hz every 100 times when V_{DD} is 5.0 V.

Use the value calculated based on the following calculating formula for the D/A conversion value.

Analog output voltage of the D/A converter (DACS0) = $A \times \sin(2\pi f t + (270/360) \times 2\pi) + B$

$= (255/2) \times \sin(2\pi f t + 1.5\pi) + ((255+1)/2)$

$= 127 \times \sin(2\pi f t + 1.5\pi) + 128$

A: amplitude, B: center output voltage, ω: angular velocity, t: time, f: frequency = 50 Hz

Setups of using peripherals are shown below.

DAC0 settings:
- Uses real-time output mode for the operation mode.
- Uses the ANO0 pin.

TAU00 settings:
- Uses interval timer mode for the operation mode.
- Sets 200 us for the interrupt period.
- Uses the TAU00 count completion interrupt.
- Uses f_{CLK} (32 MHz) for the count source.

DTC settings:
- Sets FDH (FFD00H) as DTC base address register (DTCBAR).
- Sets normal mode as the transfer mode.
- Set the data length to 8 bits.
- Sets FE000 H as the transfer source address.
- Sets incremented as the transfer source address control.
- Sets FFF34 H as the transfer destination address.
- Sets fixed as the transfer destination address.
- Sets 1 byte (01H) as the data block size transferred.
- Sets 100 times (63H) as the number of DTC data transfers.

ELC settings:

- Sets TAU channel 00 count end as the event generation source.
- Sets DA0 real-time output as the event output destination.

When an ELC program is automatically generated using Applilet3, a build error occurs when declaring variables in the R_ELC_Stop function. Please add __no_bit_access to the variable declaration to prevent build errors.

```
void R_ELC_Stop(uint32_t  event)
{
        Volatile uint32_t w_count;
        Volatile uint8_t __no_bit_access * sfr_addr;

        sfr_addr = &ELSELR00;
```

addition

Figure 4.1 shows the Timing Diagram.

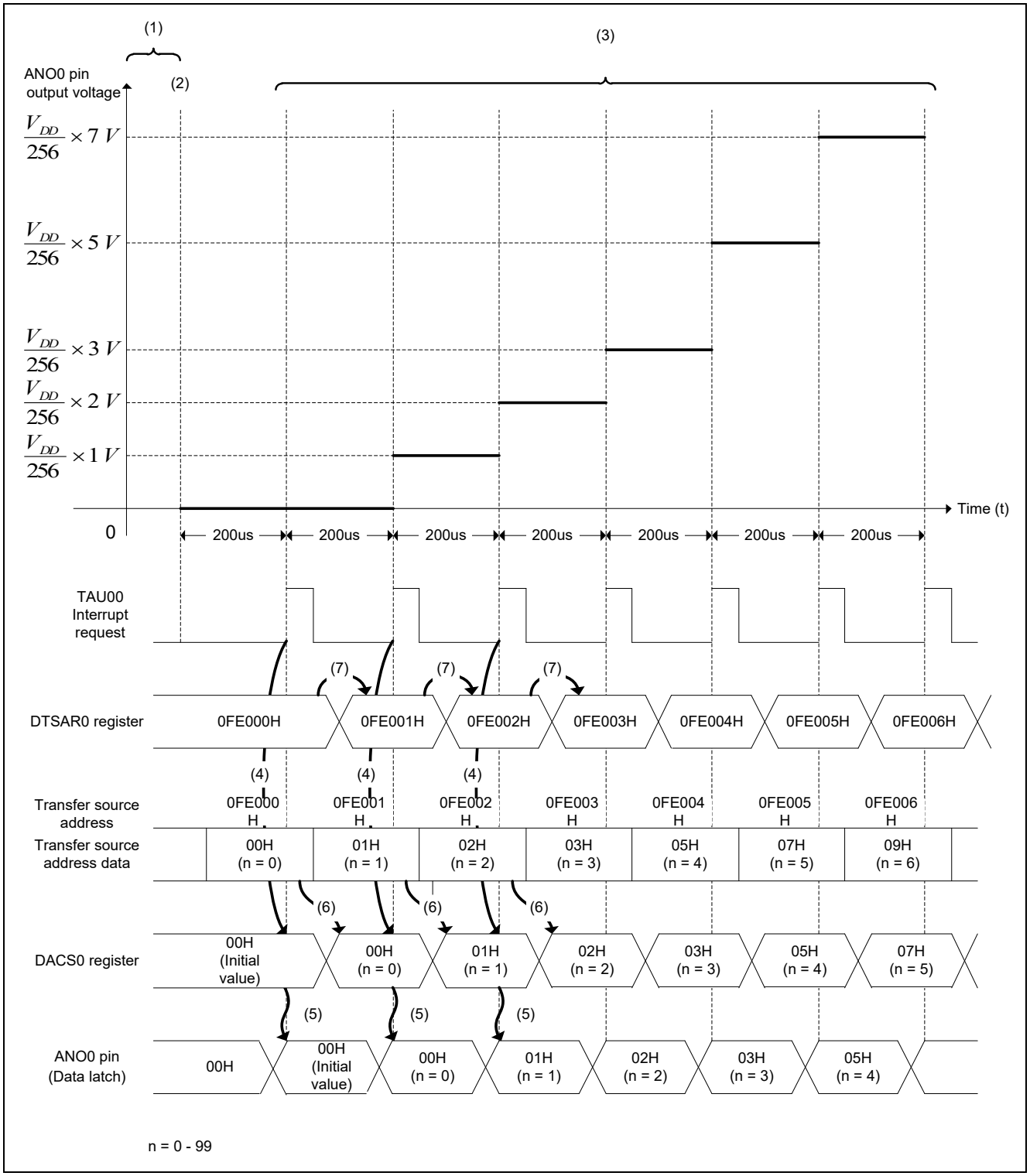

Figure 4.1 Timing Diagram

(1) Initial settings

Performs initial settings of DAC0 and TAU00. Sets the D/A conversion value to the DACS0 register to output 0.0 V from the ANO0 pin.

(2) Starts the TAU00 count.

Starts counting 200 us.

(3) TAU00 count completion

The interrupt request of TAU00 occurs.

ELC connects TAU00 interrupt request signal (Event signal) to DAC0 (Event destination).

(4) Starts D/A conversion

DAC0 performs D/A conversion of the analog voltage value of DACS0register by receiving TAU00 interrupt request signal (Event signal).

(5) Analog voltage output

After the settling time elapses, the analog voltage set in DACS0 register is output from the ANO0 pin.

(6) DTC transfer-1

DTC is activated by TAU00 interrupt request signal.

DTC reads the transfer source address data from DTSAR0 register and transfers it to DACS0 register.

(7) DTC transfer-2

DTC completes the transfer by adding the transfer source address of DTSAR0 register at the end of transfer.

4.2 Option Byte Settings

Table 4.1 lists the Option Byte Settings. When necessary, set a value suited to the user system.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	01101110B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101000B	Internal high-speed oscillation HS mode: 32 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Variables

Table 4.2 lists the Global Variables.

Table 4.2 Global Variables

Type	Variable Name	Contents	Functions Used
uint8_t	g_dac_datatable[]	D/A conversion value table	R_MAIN_UserInit

4.4 Functions

Table 4.3 lists the Functions.

Table 4.3 Functions

Function Name	Outline
R_DTCD0_Start	DTC operation start setting
R_DAC0_Start	DAC0 conversion start setting
R_TAU0_Channel0_Start	TAU00 operation enable setting

4.5 Function Specifications

The following tables list the sample code function specifications.

R_DTCD0_Start	
Outline	DTC operation start setting
Header	r_cg_dtc.h
Declaration	void R_DTCD0_Start(void)
Description	Starts DTC operation.
Argument	None
Return Value	None

R_DAC0_Start	
Outline	DAC0 conversion start setting
Header	r_cg_dac.h
Declaration	void R_DAC0_Start(void)
Description	Starts D/A conversion.
Argument	None
Return Value	None

R_TAU0_Channel0_Start	
Outline	TAU00 operation enable setting
Header	r_cg_timer.h
Declaration	void R_TAU0_Channel0_Start(void)
Description	Starts TAU00 count.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Overall Flowchart

Figure 4.2 shows the Overall Flowchart.

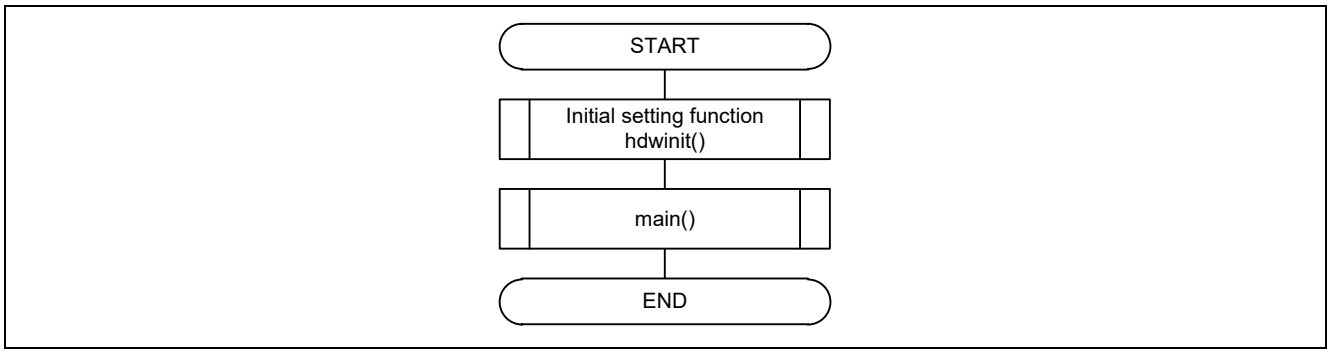

Figure 4.2 Overall Flowchart

4.6.2 Initial Setting

Figure 4.3 shows the Initial Setting.

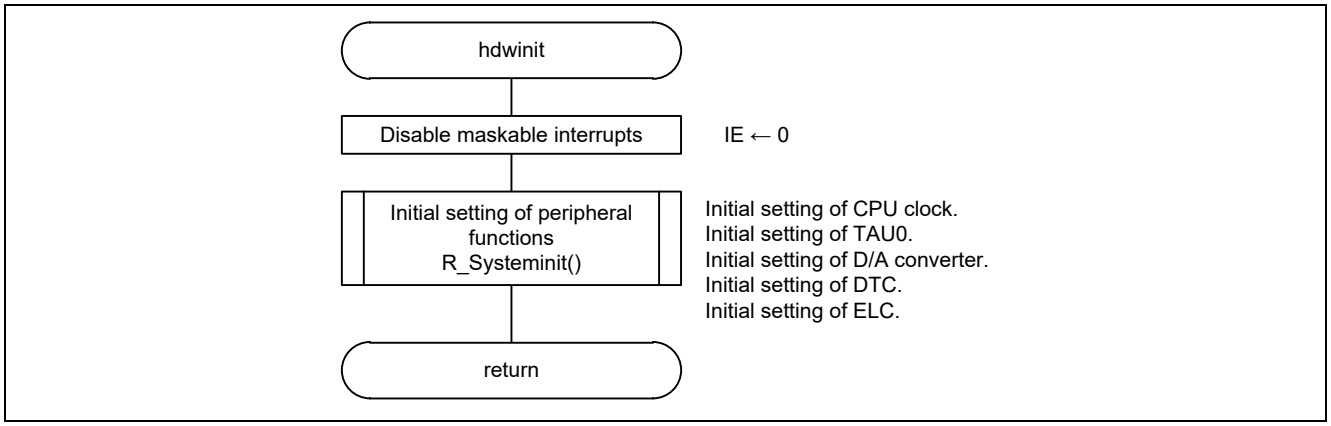

Figure 4.3 Initial Setting

4.6.3 Initial Setting of Peripheral Functions

Figure 4.4 shows the Initial Setting of Peripheral Functions.

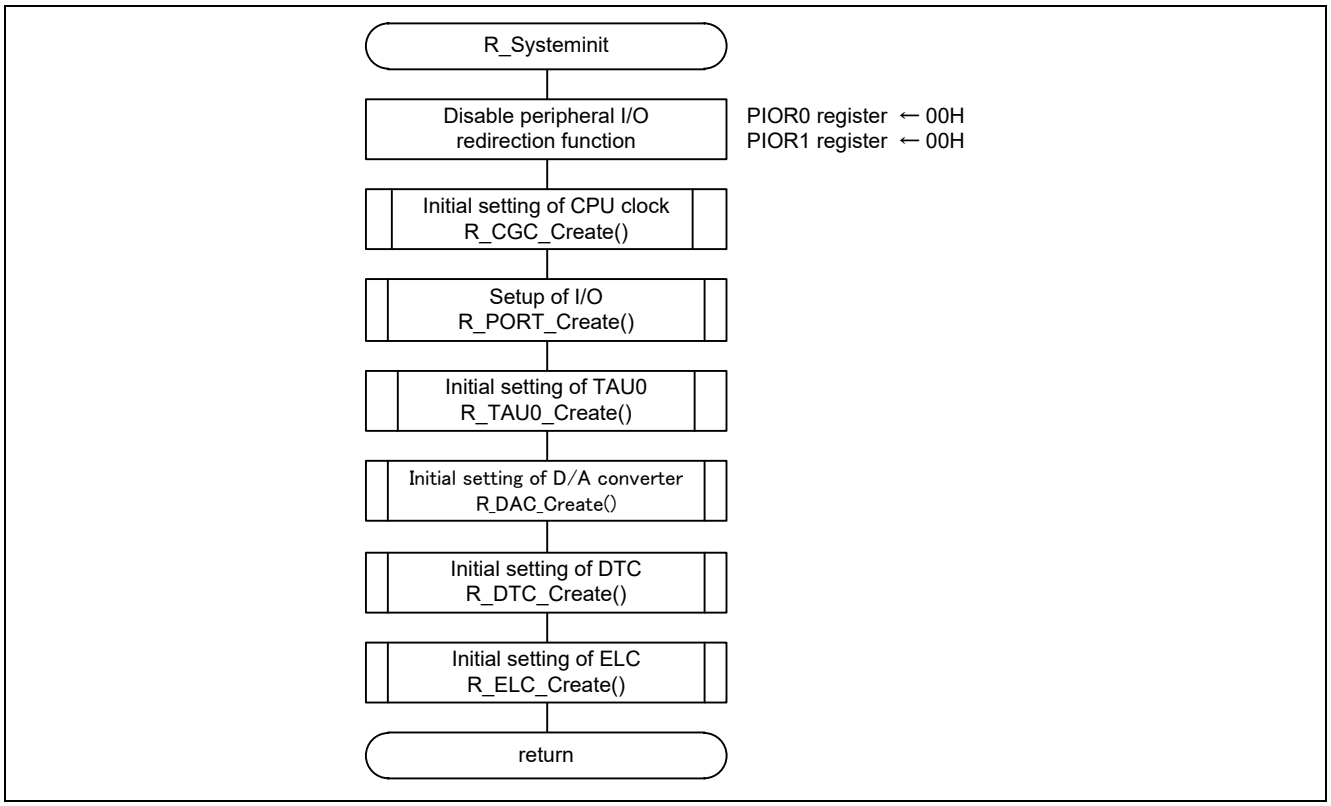

Figure 4.4 Initial Setting of Peripheral Functions

4.6.4 Initial Setting of the CPU Clock

Figure 4.5 shows the Initial Setting of the CPU Clock.

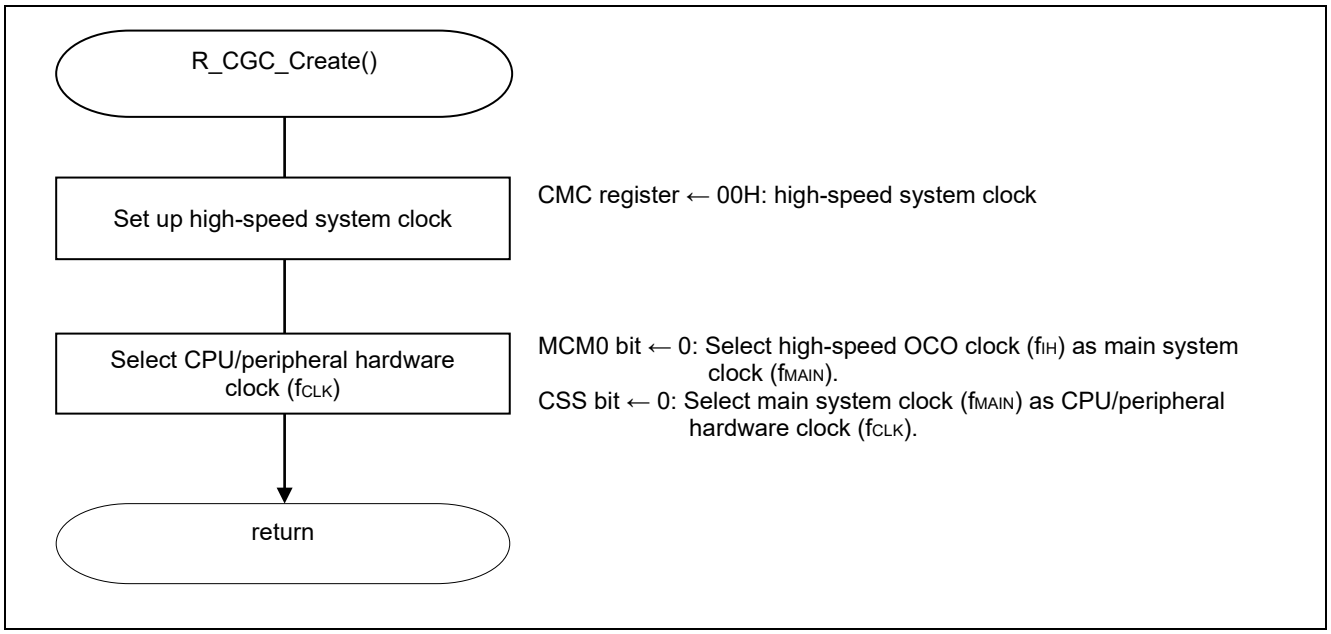

Figure 4.5 Initial Setting of the CPU Clock

Note: Refer to RL78/G13 Initialization (R01AN2575E) Application Note “Flowchart” for CPU Clock Setup (R_CGC_Create()).

4.6.5 Initial Setting of TAU0

Figure 4.6 shows the Initial Setting of TAU0.

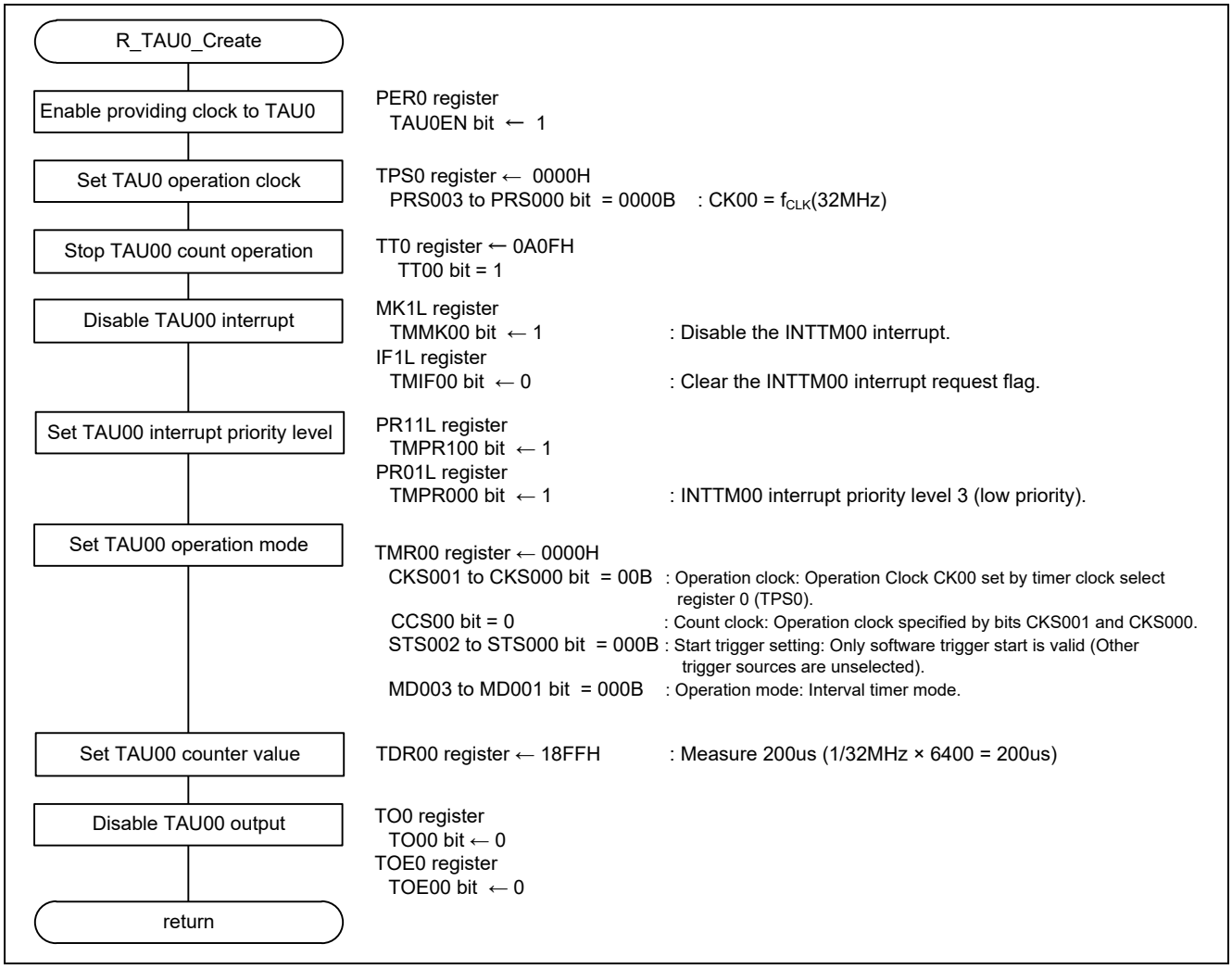

Figure 4.6 Initial Setting of TAU0

Enable providing a clock to TAU0.

- Peripheral Enable Register 0 (PER0)

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
×	×	**1**	×	×	×	×	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer array unit 0 can be read and written.**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set an operation clock of TAU0.

- Timer Clock Select Register 0 (TPS0)

Set 32 MHz for the operation clock.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
—	—	×	×	—	—	×	×	×	×	×	×	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Stop the TAU00 count operation.

- Timer Channel Stop Register 0 (TT0)
  Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
—	—	—	—	×	—	×	—	—	—	—	—	×	×	×	**1**

Bit 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).** **This bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in the 8-bit timer mode.**

Disable the TAU00 interrupt.

- Interrupt Mask Flag Register (MK1L)
  Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
×	×	×	**1**	×	×	×	×

Bit 4

TMMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Clear the TAU00 interrupt request flag.

- Interrupt Request Flag Register (IF1L)

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
×	×	×	**0**	×	×	×	×

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Set the TAU00 interrupt priority level.

- Priority Specification Flag Register (PR11L, PR01L)

Symbol: PR11L

7	6	5	4	3	2	1	0
TMPR103	TMPR102	TMPR101	TMPR100	IICAPR10	SREPR11 TMPR103H	SRPR11 CSIPR111 IICPR111	STPR11 CSIPR110 IICPR110
×	×	×	**1**	×	×	×	×

Symbol: PR01L

7	6	5	4	3	2	1	0
TMPR003	TMPR002	TMPR001	TMPR000	IICAPR00	SREPR01 TMPR003H	SRPR01 CSIPR011 IICPR011	STPR01 CSIPR010 IICPR010
×	×	×	**1**	×	×	×	×

Bit 4

TMPR100	TMPR000	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set TAU00 operation mode.

- Timer Mode Register (TMR00)
  Operation clock (f_{MCK}): CK00
  Count clock (f_{TCLK}): f_{MCK}
  Start trigger: Only software trigger start is valid.
  Operation mode: Interval timer mode (A timer interrupt is not generated when counting is started.)
  Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	—	**0**	—	**0**	**0**	**0**	×	×	—	—	**0**	**0**	**0**	**0**

Bit 15 and 14

CKS 001	CKS 000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCS00 bit. The operation clocks CK02 and CK03 can only be selected for channels 1 and 3.		

Bit 12

CCS 00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of input signal input from the TI00 pin
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Bit 10 - 8

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bit 3 - 1

MD 003	MD 002	MD 001	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	**Interval timer mode**	**Interval timer** / Square wave output / Divider function / PWM output (master)	**Counting down**
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting up
Other than above			Setting prohibited		
The operation of the MD000 bit varies depending on each operation mode (see table below).					

Bit 0

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD 000	Setting of starting counting and interrupt
· **Interval timer mode (0, 0, 0)** · Capture mode (0, 1, 0)	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
· Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
· One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
· Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set the TAU00 count value.

- Timer Data Register (TDR00)

Set 18FFH to the counter and measure 200us.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Disable the TAU00 output.

- Timer Output Register (TO0)

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
—	—	—	—	—	—	—	—	—	—	—	—	×	×	×	**0**

Bit 0

TO00	Timer output of channel 0
0	**Timer output value is “0”.**
1	Timer output value is “1”.

- Timer Output Enable Register (TOE0)

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE 03	TOE 02	TOE 01	TOE 00
—	—	—	—	—	—	—	—	—	—	—	—	×	×	×	**0**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

Note: Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

4.6.6 Initial Setting of the D/A Converter

Figure 4.7 shows the Initial Setting of the D/A Converter.

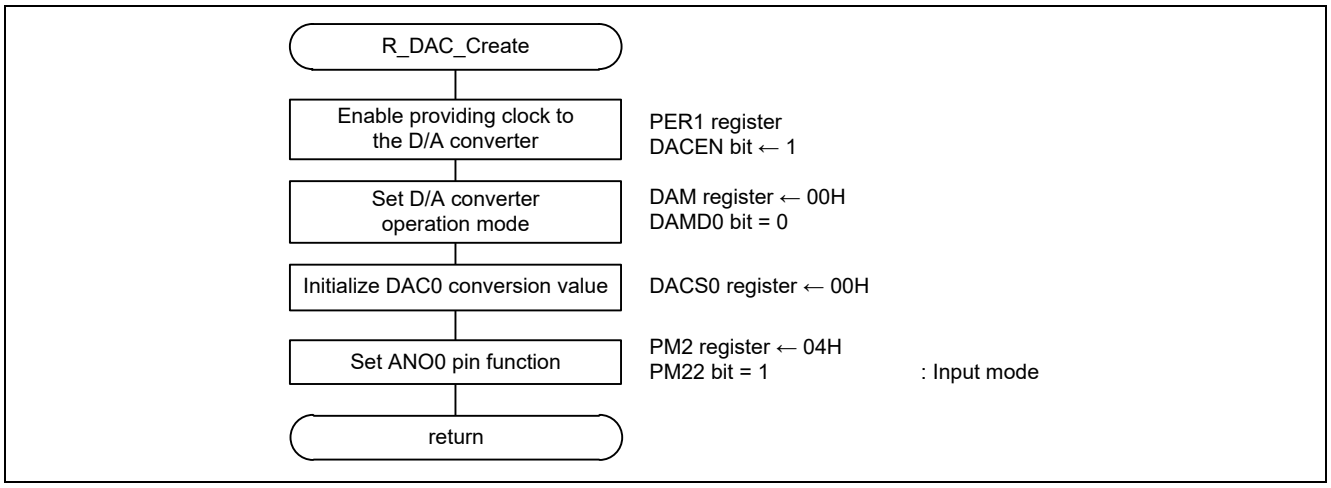

Figure 4.7 Initial Setting of the D/A Converter

Enable providing a clock to the D/A converter.

- Peripheral Enable Register 1 (PER1)

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
1	×	×	×	×	—	—	×

Bit 7

DACEN	Control of D/A converter input clock
0	Stops input clock supply. • SFR used by the D/A converter cannot be written. • The D/A converter is in the reset status.
1	**Supplies input clock.** **• SFR used by the D/A converter can be read/written.**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set the D/A converter to normal mode.

- D/A Converter Mode Register (DAM)

Symbol: DAM

7	6	5	4	3	2	1	0
0	0	DACE1	DACE0	0	0	DAMD1	DAMD0
—	—	×		—	—	×	**0**

Bit 0

DAMD0	D/A converter operation mode selection
0	**Normal mode**
1	Real-time output mode

Initialize the DAC0 conversion value.

- D/A Conversion Value Setting Register 0 (DACS0)
  Set 00H to the D/A conversion value.

Symbol: DACS0

7	6	5	4	3	2	1	0
DACS07	DACS06	DACS05	DACS04	DACS03	DACS02	DACS01	DACS00
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

—	Function
Bits 7 to 0	**The relation between the resolution and analog output voltage (VANO0) of the D/A converter are as follows. VANO0 = Reference voltage for D/A converter × (DACS0) / 256**

Set the ANO0 pin function.

- Port Mode Register 2 (PM2)

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
×	×	×	×	×	**1**	×	×

Bit 2

PM22	P22 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

4.6.7 Initial Setting of DTC

Figure 4.8 shows the Initial Setting of the DTC.

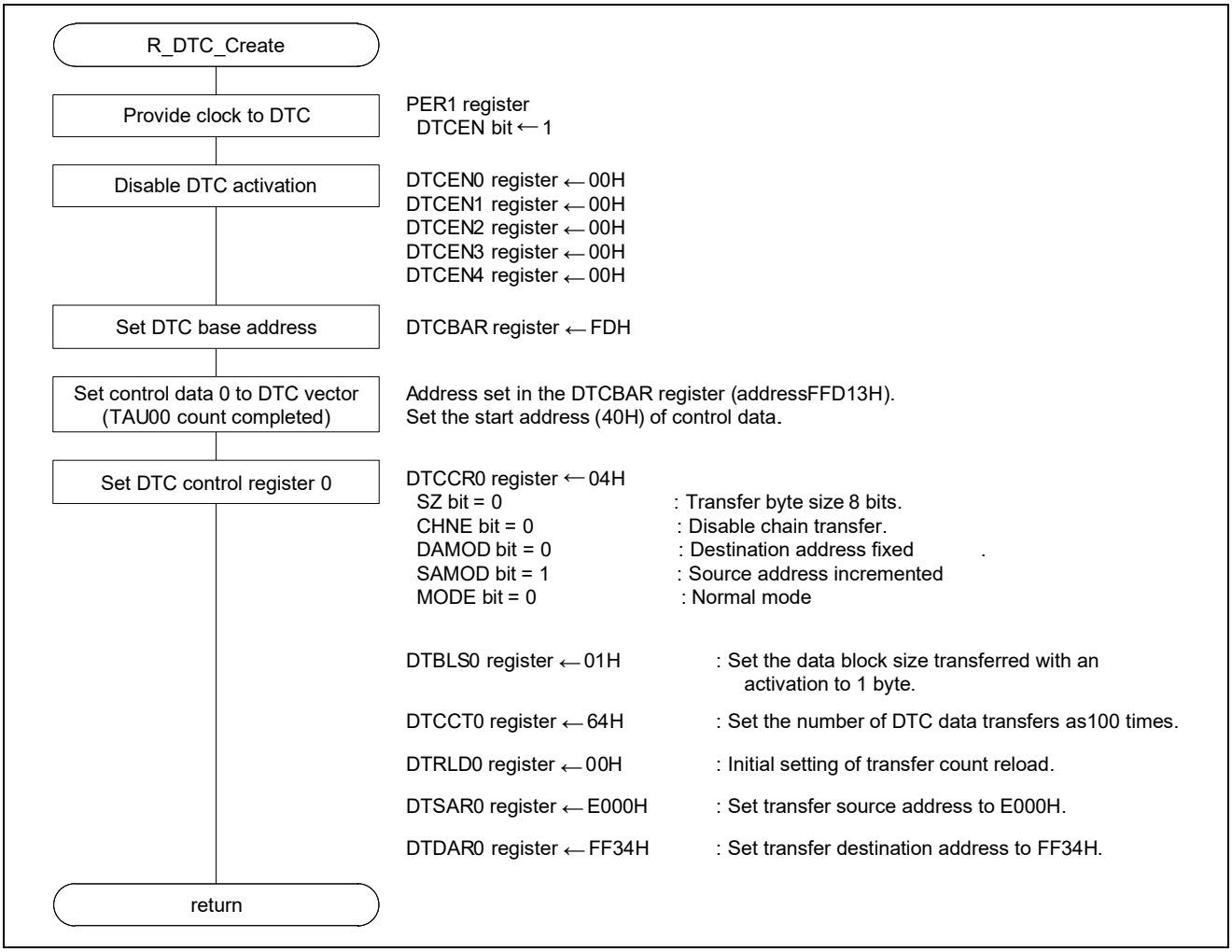

Figure 4.8 Initial Setting of the DTC

Start providing a clock to the DTC.

- Peripheral Enable Register 1 (PER1)
  Provide a clock to the DTC.
  Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
×	×	×	×	**1**	—	—	×

Bit 3

DTCEN	Control of DTC input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Disable DTC activation.

- DTC Activation Enable Register i (DTCENi) (i = 0 to 4)
  Disable DTC activation.
  Symbol: DTCENi

7	6	5	4	3	2	1	0
DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7

DTCENi7	DTC activation enable i7
0	**Activation disabled**
1	Activation enabled
The DTCENi7 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 6

DTCENi6	DTC activation enable i6
0	**Activation disabled**
1	Activation enabled
The DTCENi6 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 5

DTCENi5	DTC activation enable i5
0	**Activation disabled**
1	Activation enabled
The DTCENi5 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 4

DTCENi4	DTC activation enable i4
0	**Activation disabled**
1	Activation enabled
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 3

DTCENi3	DTC activation enable i3
0	**Activation disabled**
1	Activation enabled
The DTCENi3 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Bit 2

DTCENi2	DTC activation enable i2
0	**Activation disabled**
1	Activation enabled
The DTCENi2 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 1

DTCENi1	DTC activation enable i1
0	**Activation disabled**
1	Activation enabled
The DTCENi1 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 0

DTCENi0	DTC activation enable i0
0	**Activation disabled**
1	Activation enabled
The DTCENi0 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Set the DTC base address.

- DTC Base Address Register (DTCBAR)
  Set FDH to the DTC base address.

Symbol: DTCBAR

7	6	5	4	3	2	1	0
DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0
1	**1**	**1**	**1**	**1**	**1**	0	**1**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set the DTC control register.

- DTC Control Register 0 (DTCCR0)
  Set DTC control register 0.

Symbol: DTCCR0

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
—	**0**	**0**	**0**	**0**	**1**	**0**	**0**

Bit 6

SZ	Data size selection
0	**8 bits**
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	**Interrupt generation disabled**
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Bit 2

SAMOD	Transfer source address control
0	Fixed
1	**Incremented**
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

RPTSEL	Repeat area selection
0	**Transfer destination is the repeat area**
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	**Normal mode**
1	Repeat mode

Set DTC block size register 0.

- DTC Block Size Register 0 (DTBLS0)
  Set 01H (1 byte) to DTC block size register 0.
  Symbol: DTBLS0

7	6	5	4	3	2	1	0
DTBLS07	DTBLS06	DTBLS05	DTBLS04	DTBLS03	DTBLS02	DTBLS01	DTBLS00
0	0	0	0	0	0	0	**1**

DTBLS0	Transfer Block Size	
	8-bit transfer	16-bit transfer
00H	256 bytes	512 bytes
01H	**1 byte**	**2 bytes**
.	.	.
.	.	.
.	.	.
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set DTC transfer count register 0.

- DTC Transfer Count Register (DTCCT0)

  Set 64H (100 bytes) to the DTC transfer count register.

Symbol: DTCCT0

7	6	5	4	3	2	1	0
DTCCT07	DTCCT06	DTCCT05	DTCCT04	DTCCT03	DTCCT02	DTCCT01	DTCCT00
0	0	0	0	0	0	0	**1**

DTCCT0	Number of Transfers
00H	256 times
01H	Once
. .	. .
64H	**100 times**
. .	. .
FEH	254 times
FFH	255 times

Set DTC transfer count re load register 0.

- DTC Transfer Count Reload Register 0 (DTRLD0)

  Set 00H (0 byte) to DTC transfer count re load register 0.

Symbol: DTRLD0

7	6	5	4	3	2	1	0
DTRLD07	DTRLD06	DTRLD05	DTRLD04	DTRLD03	DTRLD02	DTRLD01	DTRLD00
0	0	0	0	0	0	0	0

Set DTC source address register 0.

- DTC Source Address Register 0 (DTSAR0)

  Set E000H to DTC source transfer source address 0.

  Symbol: DTSAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTS AR015	DTS AR014	DTS AR013	DTS AR012	DTS AR011	DTS AR010	DTS AR09	DTS AR08	DTS AR07	DTS AR06	DTS AR05	DTS AR04	DTS AR03	DTS AR02	DTS AR01	DTS AR00
1	**1**	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set DTC destination address register 0.

- DTC Destination Address Register 0 (DTDAR0)

  Set FF34H to DTC destination address register 0.

  Symbol: DTDAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR015	DTDAR014	DTDAR013	DTDAR012	DTDAR011	DTDAR010	DTDAR09	DTDAR08	DTDAR07	DTDAR06	DTDAR05	DTDAR04	DTDAR03	DTDAR02	DTDAR01	DTDAR00
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	0	0	**1**	**1**	0	**1**	0	0

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

4.6.8 Initial Setting of ELC

Figure 4.9 shows the Initial Setting of the ELC.

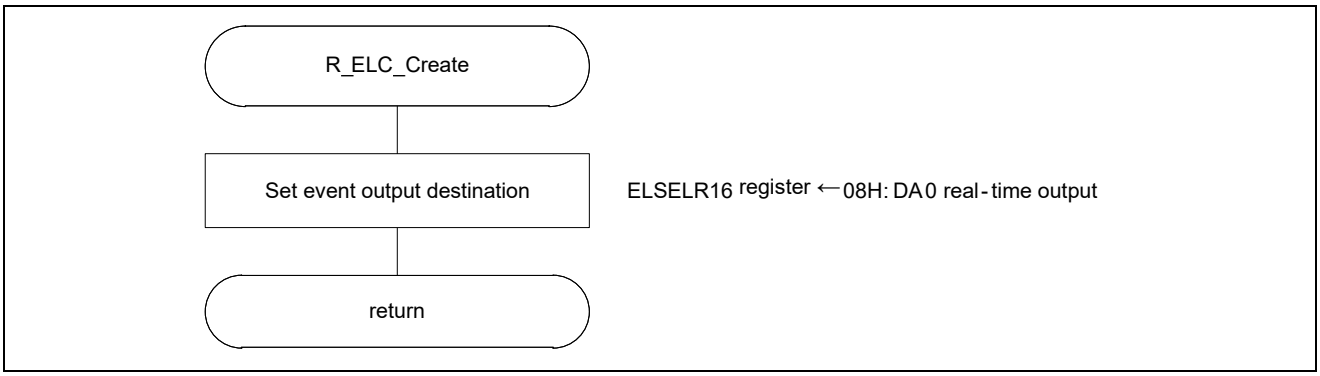

Figure 4.9 Initial Setting of ELC

Set event output destination.

- Event output destination select register 16 (ELSELR16)

Register Name	Event source (0utput source of event input 16)	Event Description
ELSELR16	**TAU channel 00 count end/capture end**	**INTTM00**

Symbol: ELSELR16

7	6	5	4	3	2	1	0
0	0	0	0	ELSELR163	ELSELR162	ELSELR161	ELSELR160
—	—	—	—	**1**	0	0	0

Bit 3-0

ELSELR163	ELSELR162	ELSELR161	ELSELR160	Event Link Selection
0	0	0	0	Event link disabled
0	0	0	1	Select operation of peripheral function 1 to link.
0	0	1	0	Select operation of peripheral function 2 to link.
0	0	1	1	Select operation of peripheral function 3 to link.
0	1	0	0	Select operation of peripheral function 4 to link.
0	1	0	1	Select operation of peripheral function 5 to link.
0	1	1	0	Select operation of peripheral function 6 to link.
0	1	1	1	Select operation of peripheral function 7 to link.
1	**0**	**0**	**0**	**Link Destination Peripheral Function: DA0 Operation When Receiving Event: Real-time output (96 KB or more code flash memory products only.)**
1	0	0	1	Select operation of peripheral function 9 to link.

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

4.6.9 Main Processing

Figure 4.10 shows the Main Processing.

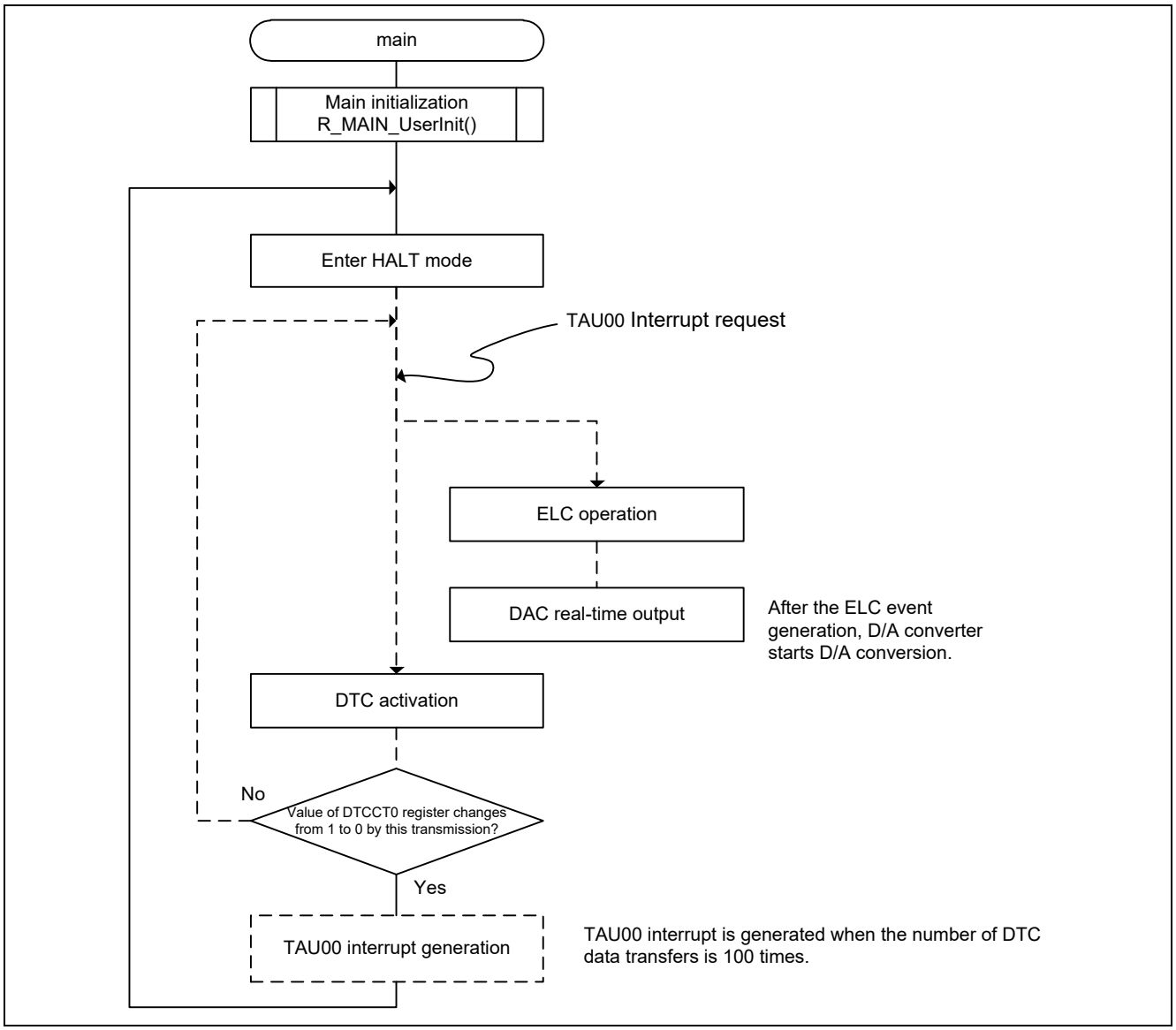

Figure 4.10 Main Processing

4.6.10 Main Initialization

Figure 4.11 shows the main initialization.

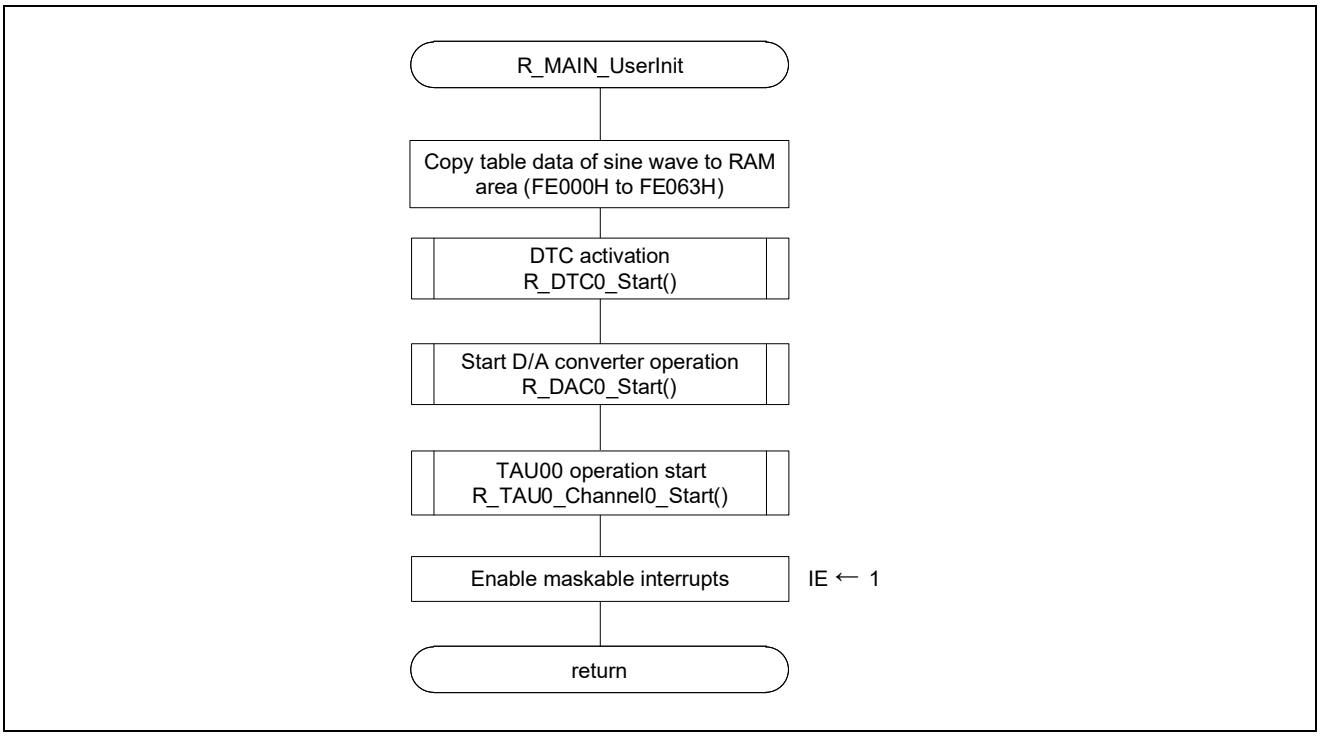

Figure 4.11 Main Initialization

4.6.11 DTC Activation

Figure 4.12 shows the DTC activation.

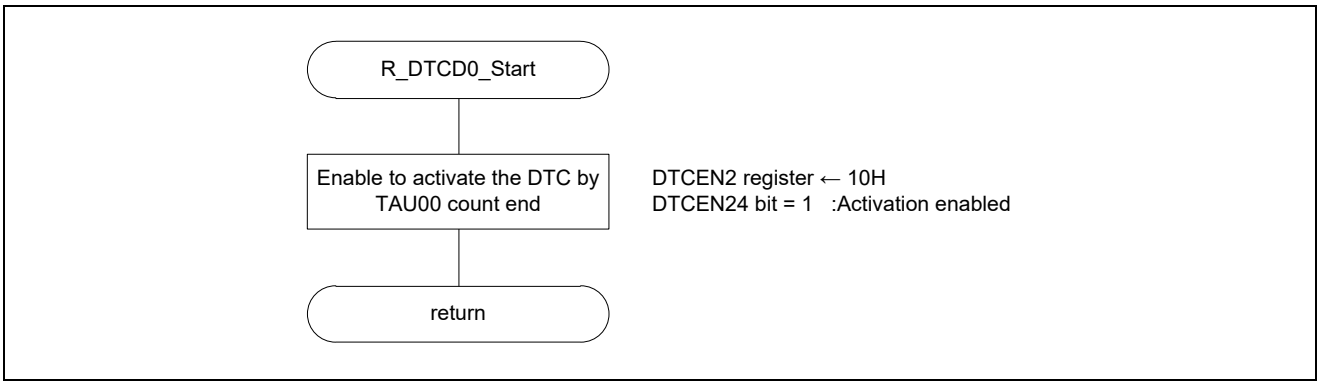

Figure 4.12 DTC Activation

Enabling to activate the DTC

- DTC activation enable register 2 (DTCEN2)
  Enable DTC to activate.
  Symbol: DTCEN2

7	6	5	4	3	2	1	0
DTCEN27	DTCEN26	DTCEN25	DTCEN24	DTCEN23	DTCEN22	DTCEN21	DTCEN20
0	0	0	**1**	0	0	0	0

Bit 4

DTCEN24	DTC activation enable 24
0	Activation disabled
1	**Activation enabled**
0 (disable to activate) is set to DTCENi4 bit on the conditions which the transfer end interrupt is generated.	

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

4.6.12 DAC0 Conversion Start Setting

Figure 4.13 shows the DAC0 Conversion Start Setting.

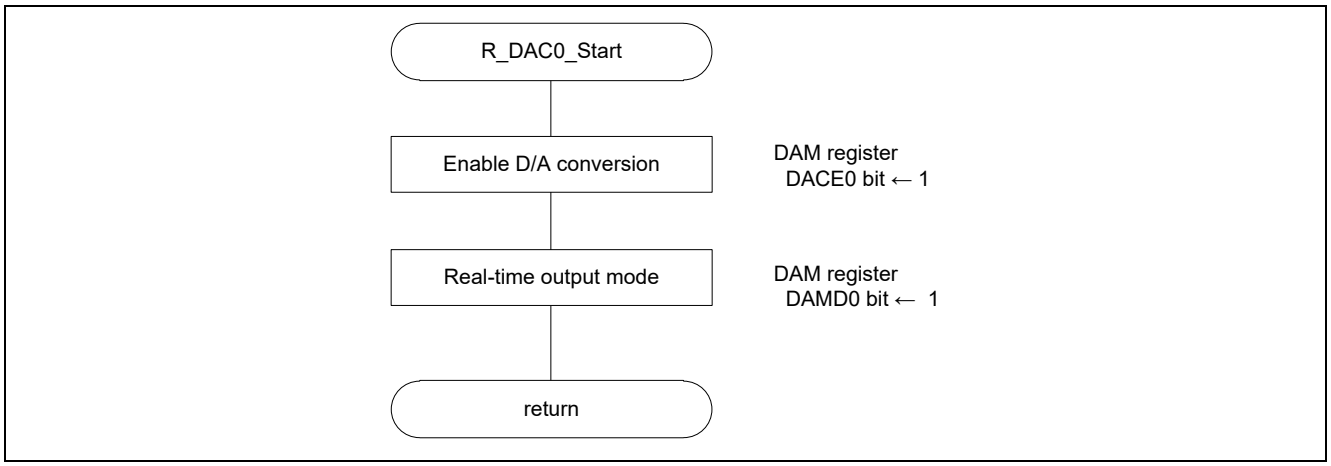

Figure 4.13 DAC0 Conversion Start Setting

Enable D/A conversion.

- D/A Converter Mode Register (DAM)
  Symbol: DAM

7	6	5	4	3	2	1	0
—	—	DACE1	DACE0	—	—	DAMD1	DAMD0
—	—	×	**1**	—	—	×	×

Bit 4

DACE0	D/A conversion operation control
0	Stops D/A conversion operation
1	**Enables D/A conversion operation**

Real-time output mode

- D/A Converter Mode Register (DAM)
  Symbol: DAM

7	6	5	4	3	2	1	0
—	—	DACE1	DACE0	—	—	DAMD1	DAMD0
—	—	×		—	—	×	**1**

Bit 0

DAMD0	D/A converter operation mode selection
0	Normal mode
1	**Real-time output mode**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

4.6.13 TAU00 Operation Enable Setting

Figure 4.14 shows the TAU00 Operation Enable Setting.

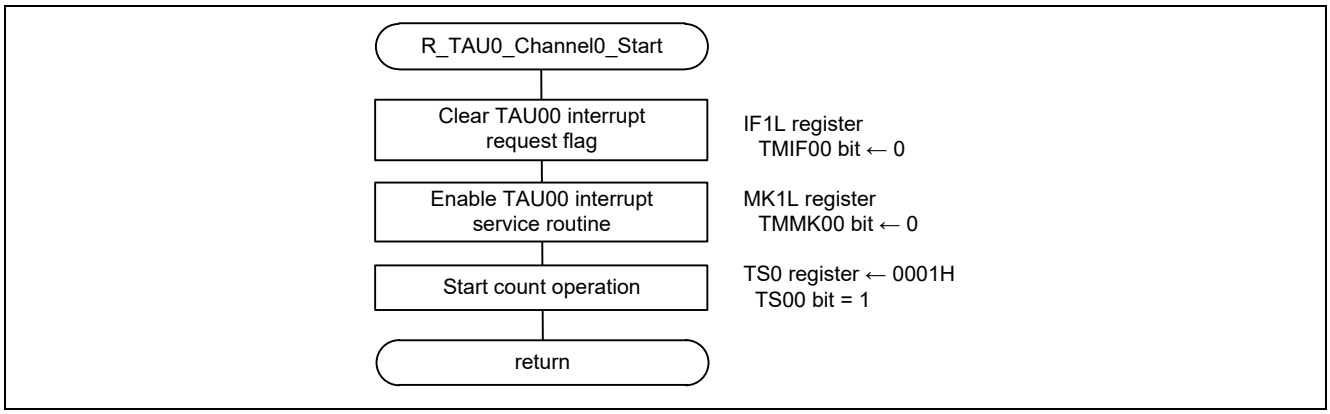

Figure 4.14 TAU00 Operation Enable Setting

Clear the TAU00 interrupt request flag.

- Interrupt Request Flag Register (IF1L)
  Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
×	×	×	**0**	×	×	×	×

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Enable the TAU00 interrupt service routine.

- Interrupt Mask Flag Register (MK1L)

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
×	×	×	**0**	×	×	×	×

Bit 4

TMMK00	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Start count operation.

- Timer Channel Start Register (TS0)

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH 03	0	TSH 01	0	0	0	0	0	TS 03	TS 02	TS 01	TS 00
—	—	—	—	×	—	×	—	—	—	—	—	×	×	×	**1**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.** **The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.**

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

4.6.14 TAU00 Interrupt

Figure 4.15 shows TAU00 interrupt.

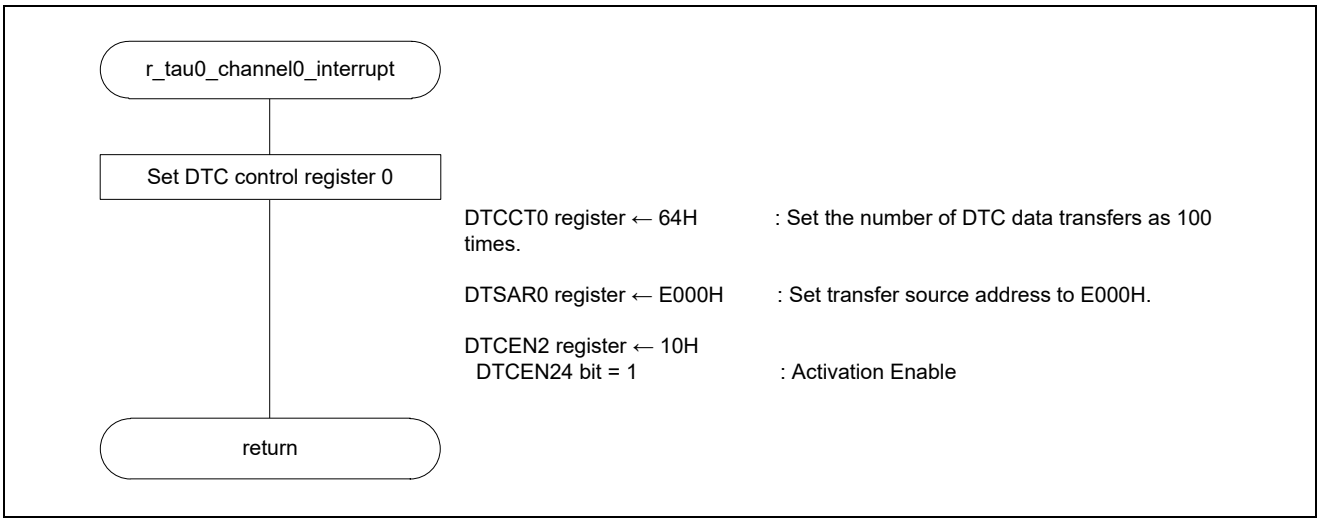

Figure 4.15 TAU00 Interrupt

Set DTC transfer count register 0.

- DTC Transfer Count Register (DTCCT0)

  Set 64H (100 bytes) to the DTC transfer count register.

  Symbol: DTCCT0

7	6	5	4	3	2	1	0
DTCCT07	DTCCT06	DTCCT05	DTCCT04	DTCCT03	DTCCT02	DTCCT01	DTCCT00
0	0	0	0	0	0	0	**1**

Bit 0

DTCCT0	Number of Transfers
00H	256 times
01H	Once
. .	. .
64H	**100 times**
. .	. .
FEH	254 times
FFH	255 times

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Set DTC source address register 0.

- DTC Source Address Register 0 (DTSAR0)

  Set E000H to DTC source transfer source address 0.

  Symbol: DTSAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTS AR015	DTS AR014	DTS AR013	DTS AR012	DTS AR011	DTS AR010	DTS AR09	DTS AR08	DTS AR07	DTS AR06	DTS AR05	DTS AR04	DTS AR03	DTS AR02	DTS AR01	DTS AR00
1	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Enable DTC activation.

- DTC Activation Enable Register 2 (DTCEN2)

  Enable DTC activation.

  Symbol: DTCEN2

7	6	5	4	3	2	1	0
DTCEN27	DTCEN26	DTCEN25	DTCEN24	DTCEN23	DTCEN22	DTCEN21	DTCEN20
0	0	0	**1**	0	0	0	0

Bit 4

DTCEN24	DTC activation enable 24
0	Activation disabled
1	**Activation enabled**
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G14 User's Manual: Hardware (R01UH0186E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Oct. 01, 2015	—	First edition issued.
1.10	May. 11, 2022	4	Updated operation check conditions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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