RL78/G14

How to Use the DTC for the RL78/G14

R01AN0861EJ0100
Rev. 1.00
Oct. 4, 2011

Abstract

This document describes an overview of the data transfer controller (DTC), a setting method for the RL78/G14, and differences with the direct memory access controller (DMA controller). Activation sources differ depending on the product. Refer to each hardware user's manual for details.

Product

RL78/G14

Contents

1. DTC

The DTC is activated using a peripheral function interrupt and transfers data between memories without going through the CPU.

Figure 1.1 shows a Comparison between Not Using and Using the DTC.

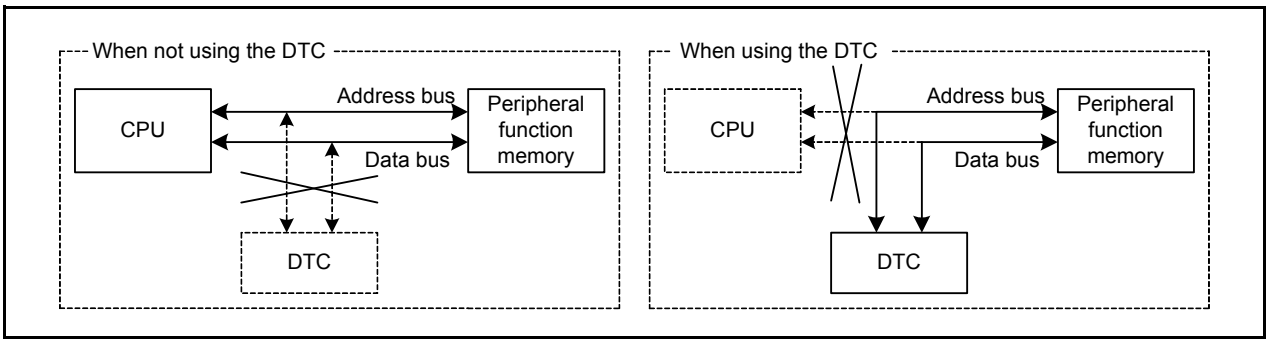


Figure 1.1 Comparison between Not Using and Using the DTC

The DTC is activated using a peripheral function interrupt. There is a maximum of 39 peripheral function interrupts that can be used as an activation source. A maximum of 24 data sets can be sent successively. Set the control data to specify a transfer source address, transfer destination address, and the number of transfer bytes. Given data transfer can be performed in a short time without going through the CPU when the interrupt request of individual peripheral function is generated.

Figure 1.2 shows an Overview of DTC Operation.

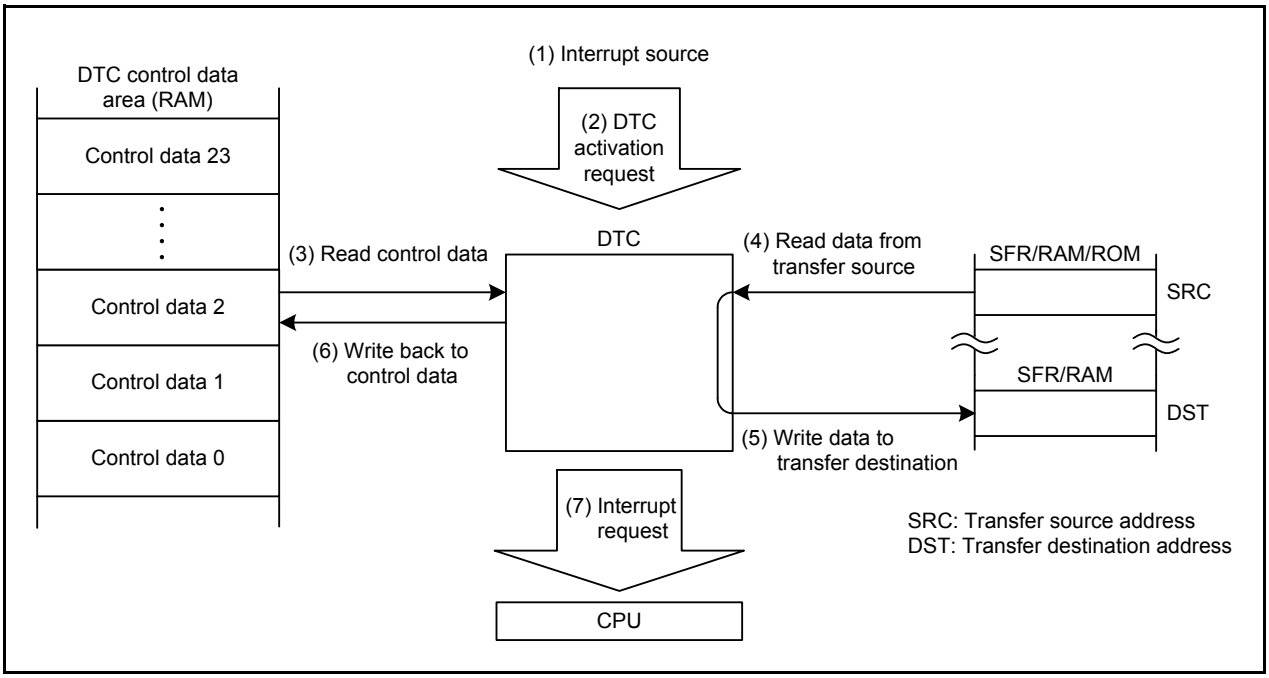


Figure 1.2 Overview of DTC Operation

2. Advantages of the DTC

This chapter explains the differences in processing between data transfer being performed during interrupt handling, and data transfer being performed by the DTC. In the former, data transfer is performed in the interrupt handling by a program after an interrupt source is generated. In the latter, after an interrupt source is generated, the DTC is used to transfer data between memories directly without going through the CPU. As interrupt transition time and program processing time are not necessary, using the DTC shortens the amount of processing time.

Figure 2.1 shows Processing Comparison of Data Transfer between Using the CPU and Using the DTC.

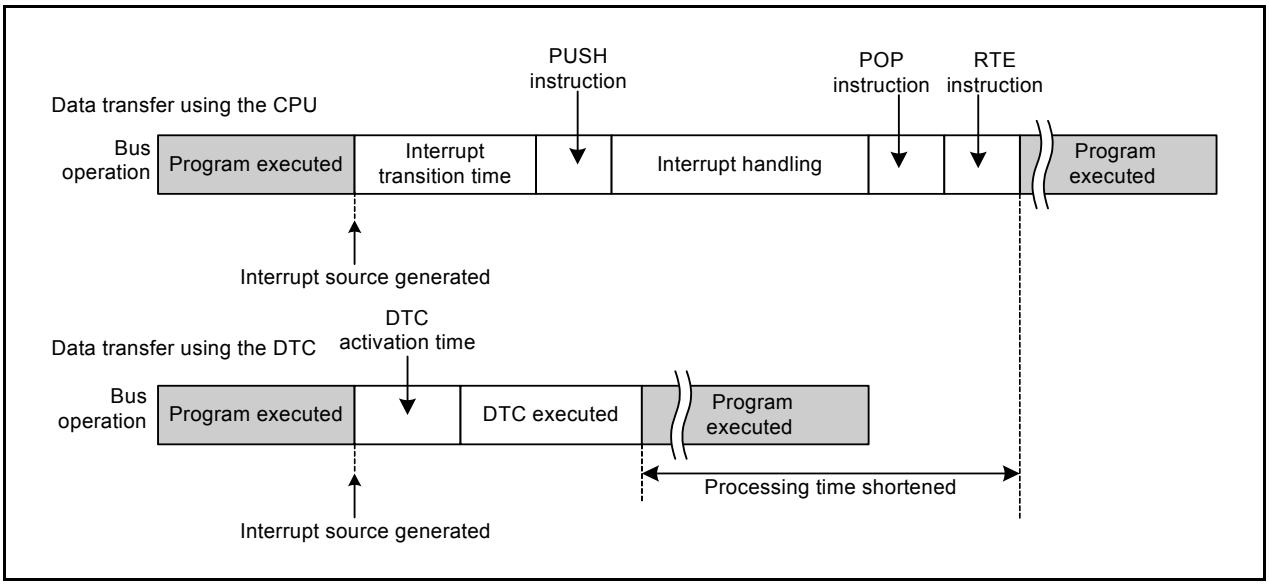


Figure 2.1 Processing Comparison of Data Transfer between Using the CPU and Using the DTC

3. Available Activation Sources

The DTC is activated by an interrupt source. Priorities are set each activation source. When multiple activation sources are generated simultaneously, the DTC activates in accordance with the priority set to the DTC activation source.

Tables 3.1 and 3.2 list Activation Sources of the RL78/G14.

Table 3.1 Activation Sources of the RL78/G14 (1/2)

DTC Activation Sources	Source Number	Priority
Reserved	0	High
INTP0	1	↑
INTP1	2	
INTP2	3	
INTP3	4	
INTP4	5	
INTP5	6	
INTP6	7	
INTP7	8	
Key input	9	
A/D conversion	10	
UART0 reception transfer end/CSI01 transfer end or buffer empty/IIC01 transfer end	11	
UART0 transmission transfer end/CSI00 transfer end or buffer empty/IIC00 transfer end	12	
UART1 reception transfer end/CSI11 transfer end or buffer empty/IIC11 transfer end	13	
UART1 transmission transfer end/CSI10 transfer end or buffer empty/IIC10 transfer end	14	
UART2 reception transfer end/CSI21 transfer end or buffer empty/IIC21 transfer end	15	
UART2 transmission transfer end/CSI20 transfer end or buffer empty/IIC20 transfer end	16	
UART3 reception transfer end/CSI31 transfer end or buffer empty/IIC31 transfer end (1)	17	
UART3 transmission transfer end/CSI30 transfer end or buffer empty/IIC30 transfer end (1)	18	
End of channel 0 of timer array unit 0 count or capture	19	
End of channel 1 of timer array unit 0 count or capture	20	
End of channel 2 of timer array unit 0 count or capture	21	
End of channel 3 of timer array unit 0 count or capture	22	
End of channel 0 of timer array unit 1 count or capture (1)	23	
End of channel 1 of timer array unit 1 count or capture (1)	24	
End of channel 2 of timer array unit 1 count or capture (1)	25	
End of channel 3 of timer array unit 1 count or capture (1)	26	

Note:

1. Only for 80-pin and 100-pin packages

Table 3.2 Activation Sources of the RL78/G14 (2/2)

DTC Activation Sources	Source Number	Priority
Timer RD compare match A0	27	
Timer RD compare match B0	28	
Timer RD compare match C0	29	
Timer RD compare match D0	30	
Timer RD compare match A1	31	
Timer RD compare match B1	32	
Timer RD compare match C1	33	
Timer RD compare match D1	34	
Timer RG compare match A	35	
Timer RG compare match B	36	
Timer RJ0 underflow	37	
Comparator detection 0 (1)	38	
Comparator detection 1 (1)	39	Low

Note:
1. Only for products with a code flash memory size of 96 KB or more.

4. DTC Control Data and DTC Vector Table

In order to transfer data using the DTC, it is necessary to set the DTC control data which controls data transfer, and setting the DTC vector address which shows the control data to be used.

4.1 Allocation of DTC Control Data Area and DTC Vector Table Area

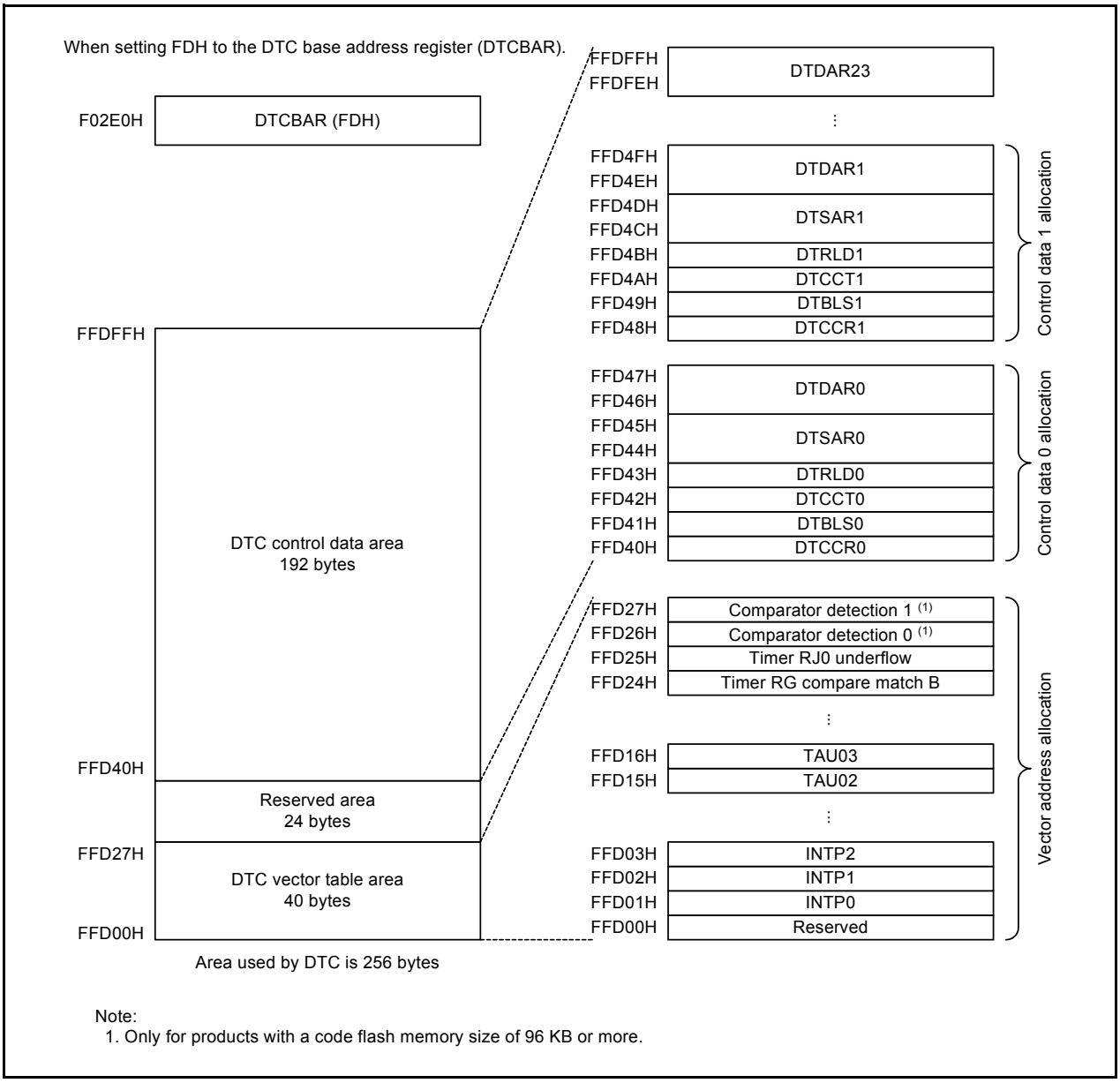
The DTC control data area and DTC vector table area are allocated on internal RAM using the DTC base address register (DTCBAR). The DTC control data area and DTC vector table area can be allocated to given addresses using the DTCBAR register.

DTCBAR register:
Set the higher 8 bits of the DTC vector table area and DTC control data area.

DTC Control Data Area:
The upper 8 bits are the value of the DTCBAR register; the value of the lower 8 bits is 40H, which is the starting address of the DTC control data area. There are 24 sets (0 to 23) of 8-byte control data for a total of 192 bytes.

DTC Vector Table Area:
The upper 8 bits are the value of the DTCBAR register; the value of the lower 8 bits is 00H, which is the starting address of the DTC vector table area. The DTC vector table area has a total of 40 bytes.

Figure 4.1 shows an Allocation Example of DTC Control Data Area and DTC Vector Table Area.



Note:
1. Only for products with a code flash memory size of 96 KB or more.

Figure 4.1 Allocation Example of DTC Control Data Area and DTC Vector Table Area

4.2 DTC Control Data

The control data controls the DTC data transfer. The DTC reads the control data specified from the control data area when the DTC activates, and performs data transfer according to the read data contents. The DTC updates the control data and writes back to the DTC control data area when data transfer is completed. The DTC control data is allocated from the starting address in order of registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). 24 sets of control data can be set to the DTC control data area and 24 types of data transfer can be performed.

Table 4.1 lists the Control Data Settings.

Table 4.1 Control Data Settings

Setting Register	Item	Contents
DTC control register j (DTCCRj)	Select data size	Select 8 bits or 16 bits
	Enable or disable repeat mode interrupts	Select interrupt generation disabled or enabled
	Enable or disable chain transfer	Select chain transfer disabled or enabled
	Control transfer destination address	Select fixed or incremented
	Control transfer source address	Select fixed or incremented
	Select repeat area	Select transfer destination address or transfer source address
	Select transfer mode	Select normal mode or repeat mode
DTC block size register j (DTBLSj)	The number of bytes in transfer block	The number of bytes in a block transferred by an activation • 8 bits: 1 byte (01H) to 256 bytes (00H) • 16 bits: 2 bytes (01H) to 512 bytes (00H)
DTC transfer count register j (DTCCTj)	The number of DTC data transfers	Normal mode: 1 time (01H) to 256 times (00H) Repeat mode: 1 time (01H) to 255 times (FFH)
DTC transfer count reload register j (DTRLDj)	Initial value of transfer count register in repeat mode	1 time (01H) to 255 times (FFH)
DTC source address register j (DTSARj)	Transfer source address when data transfer is performed	Refer to Address space which can be transferred in Table 5.1 DTC Specifications
DTC destination address register j (DTDARj)	Transfer destination address when data transfer is performed	

j = 0 to 23

4.3 DTC Vector Table

The DTC vector address is set in the DTC vector table area and includes 1 byte for each activation source. The address where the source number of activation sources was added to the starting address of the DTC vector table is the corresponding DTC vector address to each source. Set the lower 8 bits of the starting address of the control data to be used to each DTC vector address for activation. The DTC decides the control data based on the corresponding DTC vector address value and DTCBAR register value when an activation source is generated.

Figure 4.2 shows the Relationship Between the Control Data and Vector Table.

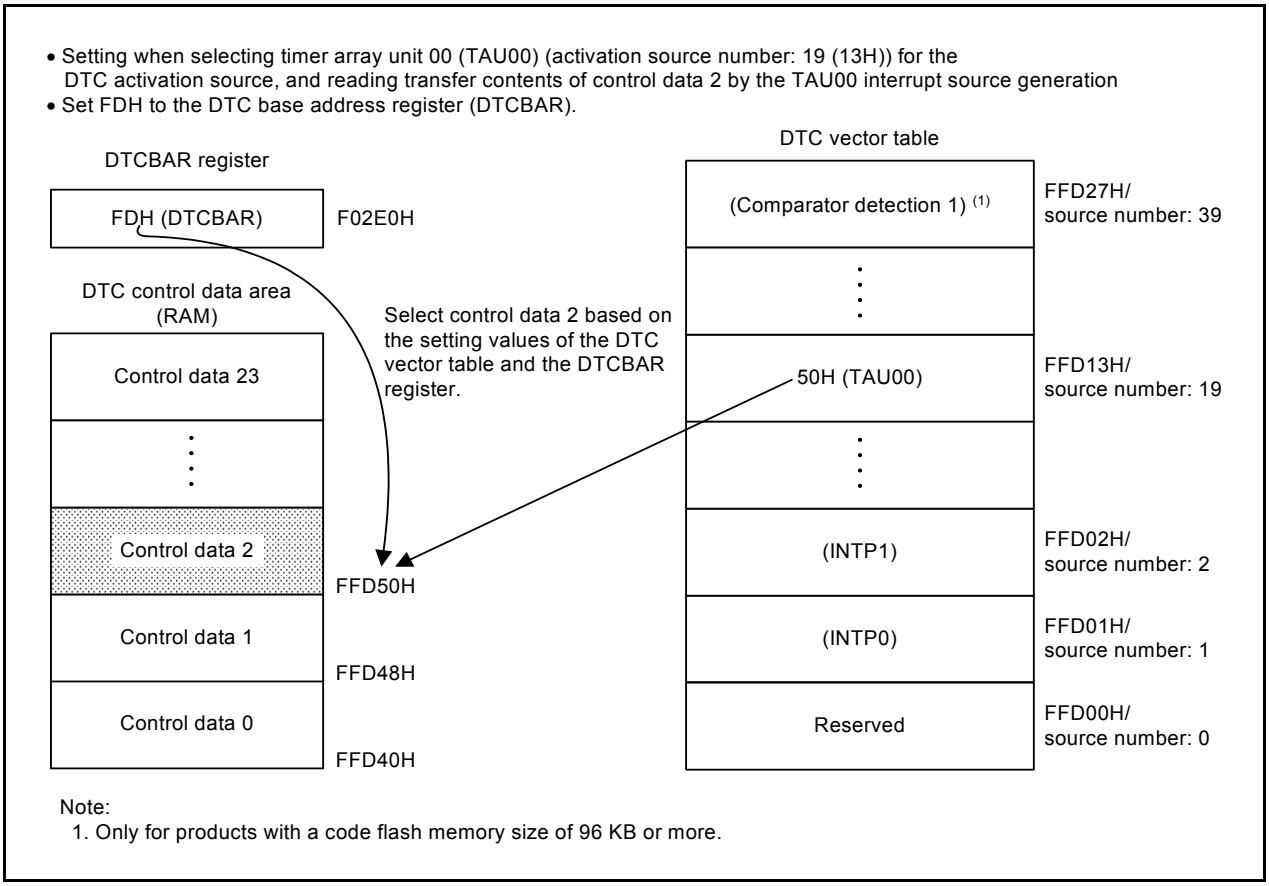


Figure 4.2 Relationship Between the Control Data and Vector Table

4.4 DTC Activation Enable Register i

Set this register to enable or disable DTC activation using each interrupt source, and there is a total of 5 bytes. Each activation source is assigned 1 bit.

Table 4.2 lists the Relationship Between Interrupt Sources of RL78/G14 and Bits DTCENi0 to DTCEN7.

Table 4.2 Relationship Between Interrupt Sources of RL78/G14 and Bits DTCENi0 to DTCEN7

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	Reserved	INTP0	INTP1	INTP2	INTP3	INTP4	INTP5	INTP6
DTCEN1	INTP7	Key input	A/D conversion	UART0 reception transfer end/CSI01 transfer end or buffer empty/IIC01 transfer end	UART0 transmission transfer end/CSI00 transfer end or buffer empty/IIC00 transfer end	UART1 reception transfer end/CSI11 transfer end or buffer empty/IIC11 transfer end	UART1 transmission transfer end/CSI10 transfer end or buffer empty/IIC10 transfer end	UART2 reception transfer end/CSI21 transfer end or buffer empty/IIC21 transfer end
DTCEN2	UART2 transmission transfer end/CSI20 transfer end or buffer empty/IIC20 transfer end	UART3 reception transfer end/CSI31 transfer end or buffer empty/IIC31 transfer end (1)	UART3 transmission transfer end/CSI30 transfer end or buffer empty/IIC30 transfer end (1)	End of channel 0 of timer array unit 0 count or capture	End of channel 1 of timer array unit 0 count or capture	End of channel 2 of timer array unit 0 count or capture	End of channel 3 of timer array unit 0 count or capture	End of channel 0 of timer array unit 1 count or capture (1)
DTCEN3	End of channel 1 of timer array unit 1 count or capture (1)	End of channel 2 of timer array unit 1 count or capture (1)	End of channel 3 of timer array unit 1 count or capture (1)	Timer RD compare match A0	Timer RD compare match B0	Timer RD compare match C0	Timer RD compare match D0	Timer RD compare match A1
DTCEN4	Timer RD compare match B1	Timer RD compare match C1	Timer RD compare match D1	Timer RG compare match A	Timer RG compare match B	Timer RJ0 underflow	Comparator detection 0 (2)	Comparator detection 1 (2)

i = 0 to 4

Notes:

1. Only for 80-pin and 100-pin packages.
2. Only for products with a code flash memory size of 96 KB or more.

5. Transfer Modes

Transfer modes include normal mode and repeat mode, and data transfer is performed in 8-bit or 16-bit units.In normal mode, one block consists of a specific number of bytes. One block is transferred for each activation, and the number of blocks equals the number of transfers set. When either the transfer source address or destination address is specified as the repeat area, and transfer of the number of blocks set is completed, the address specified as the repeat area is initialized, and transfer is repeated. Several control data are read for an activation source and transfer is sequentially performed as a chain transfer.

Table 5.1 lists DTC Specifications.

Table 5.1 DTC Specifications

Item		Normal Mode	Repeat Mode
Activation sources		Maximum 39 sources	
Allocatable control data		24 types	
Address space which can be transferred	Address space	64 Kbytes (F0000H to FFFFFH), excluding general-purpose registers	
	Transfer source address	1st SFR area, RAM area (excluding general-purpose registers), mirror area (1), data flash memory area (1), 2nd SFR area	
	Transfer destination address	1st SFR area, RAM area (excluding general-purpose registers), 2nd SFR area	
Maximum number of transfers		256 times	255 times
Maximum size of block to be transferred		• 256 bytes (8-bit transfer) • 512 bytes (16-bit transfer)	255 bytes
Unit of transfers		8 bits/16 bits	
Transfer mode		Transfers end on completion of the transfer causing the DTCCTj register value to change from 01H to 00H.	On completion of the transfer causing the DTCCTj register value to change from 01H to 00H, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control		Fixed or incremented	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		Refer to Tables 3.1 and 3.2 Activation Sources of RL78/G14	
Interrupt request		When data transfer causing the DTCCTj register value to change from 01H to 00H is performed, an activation source interrupt request is generated, and interrupt handling is performed on completion of data transfer.	When data transfer causing the DTCCTj register value to change from 01H to 00H is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an activation source interrupt request is generated, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.	
Transfer stop		• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When data transfer causing the DTCCTj register value to change from 01H to 00H is completed.	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When data transfer causing the DTCCTj register value to change from 01H to 00H is completed while the RPTINT bit is 1 (interrupt generation enabled).
Operation in standby mode	HALT	DTC operates	
	SNOOZE	DTC operates	
	STOP	DTC stops	

i = 0 to 4, j = 0 to 23

Note:

1. In SNOOZE mode, these areas cannot be set as the sources for DTC transfer since the flash memory is stopped.

5.1 Normal Mode

In normal mode, for each DTC activation, either 1 to 256 bytes of 8-bit data can be transferred, or 2 to 512 bytes of 16-bit data can be transferred.The number of transfers can be set from 1 to 256. Fixed or incremented for the number of byes in each block can be selected for the transfer source address and destination address to update the control data when data transfer is completed. When selecting incremented, the number of bytes in each block is incremented.
When data transfer for the number of transfers is completed, the DTC generates an interrupt request corresponding to the activation source and automatically sets bits DTCENi0 to DTCENi7 corresponding to the DTCENi register to 0 (activation disabled) (i = 0 to 4). When activating the DTC again, enable DTC activation.

Figure 5.1 shows an Example of Address Control (Transfer Source Address: Fixed; Transfer Destination Address: Incremented), and Figure 5.2 shows an Example of Address Control (Transfer Source Address: Incremented; Transfer Destination Address: Incremented).

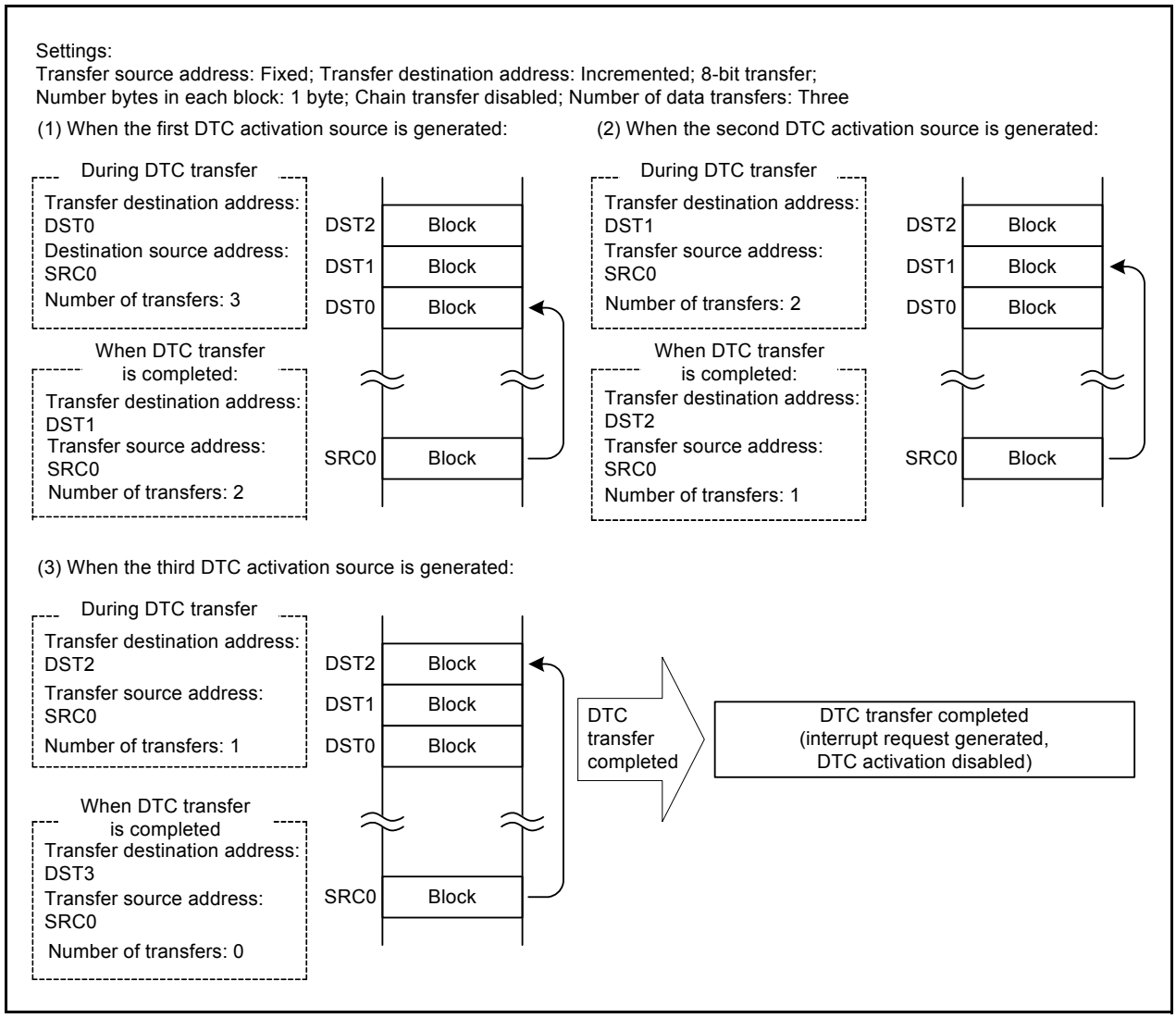


Figure 5.1 Example of Address Control (Transfer Source Address: Fixed; Transfer Destination Address: Incremented)

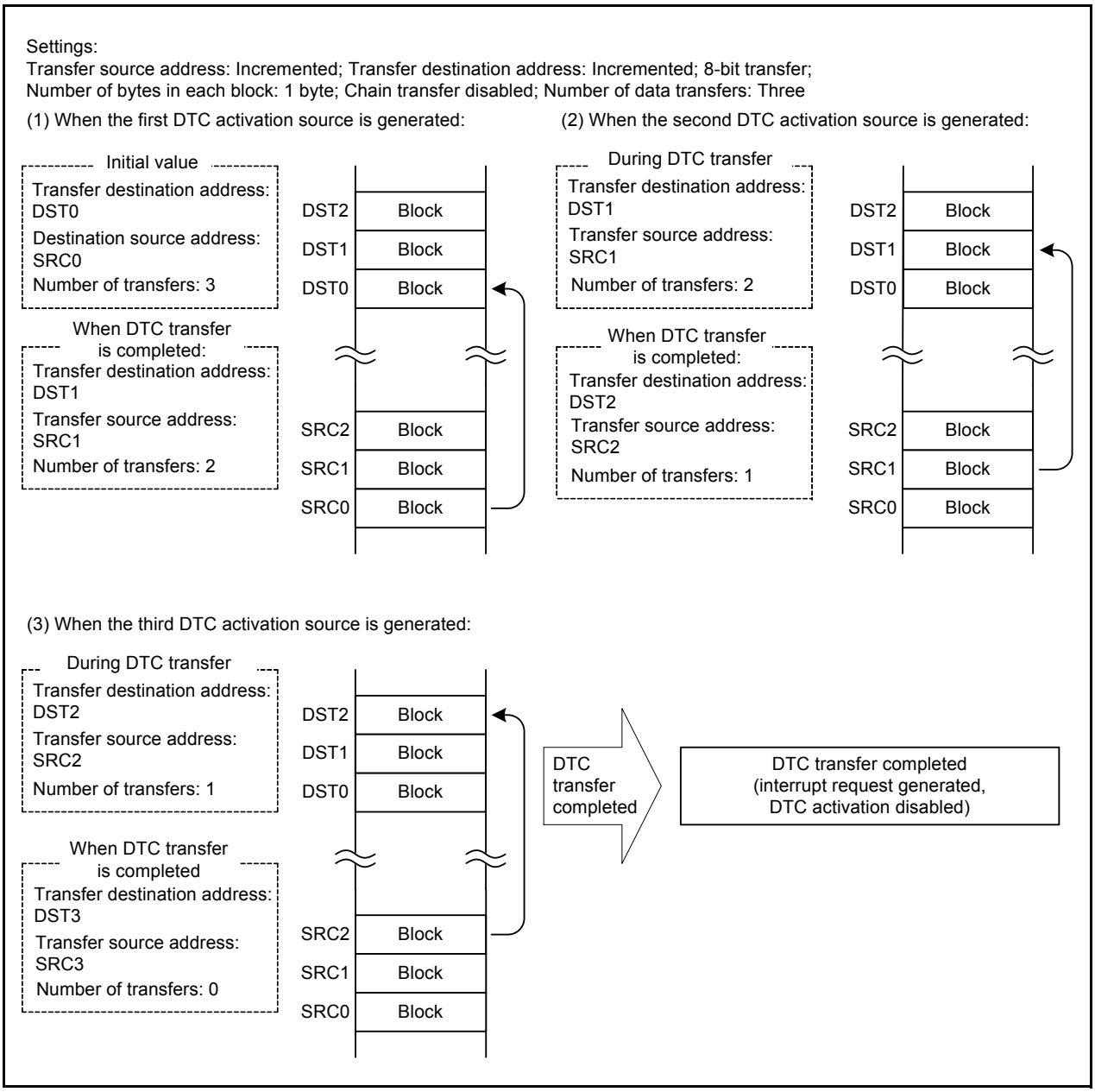


Figure 5.2 Example of Address Control (Transfer Source Address: Incremented; Transfer Destination Address: Incremented)

5.2 Repeat Mode

1 to 255 bytes of data can be transferred by a DTC activation in repeat mode. The number of transfers can be set from 1 to 255. However, the total number of bytes cannot exceed 255 bytes until the number of transfers is completed. Repeat mode is different from normal mode in that either the transfer source address or destination address can be specified as the repeat area. Set the lower 8 bits of the repeat area address to 00H. The number of bytes in each block is incremented for the address specified as the repeat area. Either fixed or incremented can be selected for the address which is not specified as the repeat area. When selecting incremented, the number of bytes in each block is incremented. When data transfer of the number of set transfers is completed, write back the initial value to the address specified as the repeat area and write back the value in the DTRLD register to the DTCCT register. Repeat mode interrupts can be enabled or disabled in repeat mode. When repeat mode interrupts are disabled and data transfer for the number of transfers is completed, DTC activation is not disabled and the DTC successively activates by generated activation sources.

Figure 5.3 shows an Example of Address Control (Transfer Source Address: Fixed; Repeat Area: Transfer Destination Address). Figure 5.4 shows an Example of Address Control (Transfer Source Address: Incremented; Repeat Area: Transfer Destination Address).

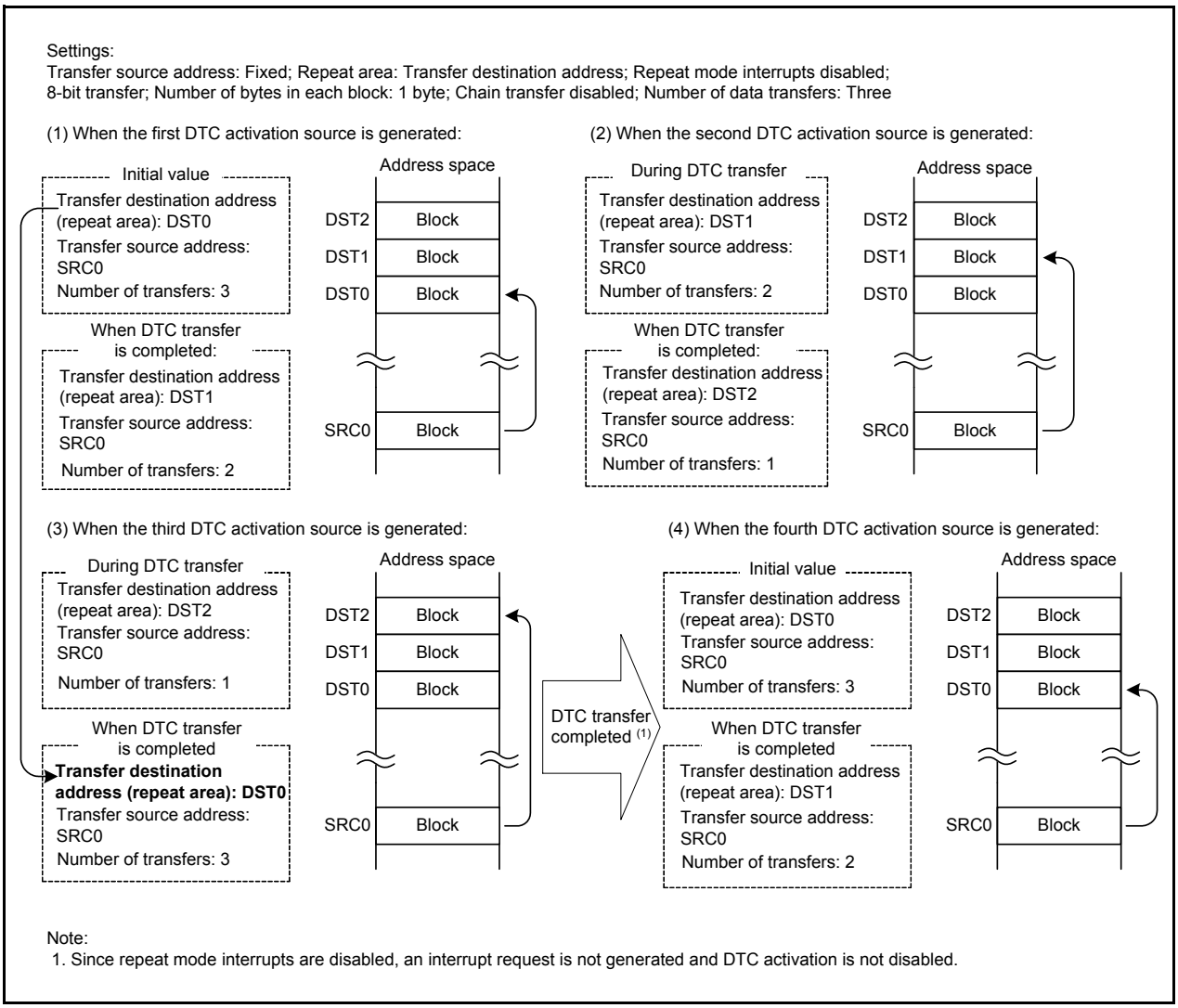


Figure 5.3 Example of Address Control (Transfer Source Address: Fixed; Repeat Area: Transfer Destination Address)

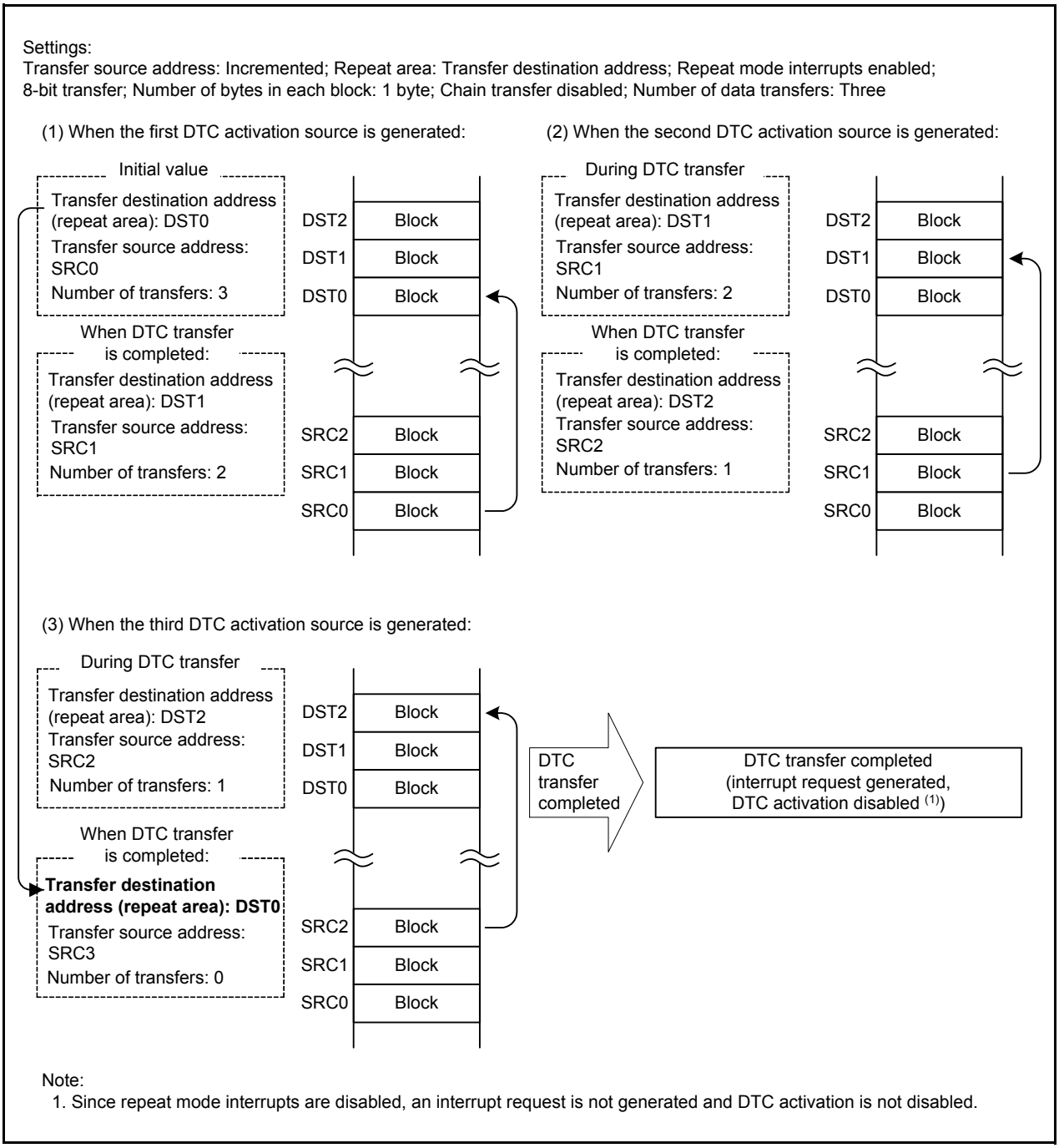


Figure 5.4 Example of Address Control (Transfer Source Address: Incremented; Repeat Area: Transfer Destination Address)

5.3 Chain Transfer

In a chain transfer, multiple data transfers are successively performed by an activation source. When a chain transfer is enabled for the control data during operation, after data transfer is completed, DTC operation is not completed. The next control data of the data which has been successively allocated is read, and data transfer continues. This is repeated until transfer based on the control data for which chain transfer is disabled is completed. However, disable chain transfer for control data 23 allocated at the end in DTC control data area.

When transfer sets the DTCCT register of the control data corresponding to the activation source from 01H to 00H, an interrupt request is generated and DTC activation is disabled. Interrupt requests are retained until transfer based on the control data for which chain transfer is disabled is completed. An interrupt request and DTC activation enable bit are not changed for transfer based on the control data read by chain transfer.

Figure 5.5 shows an Example of Chain Transfer Operation.

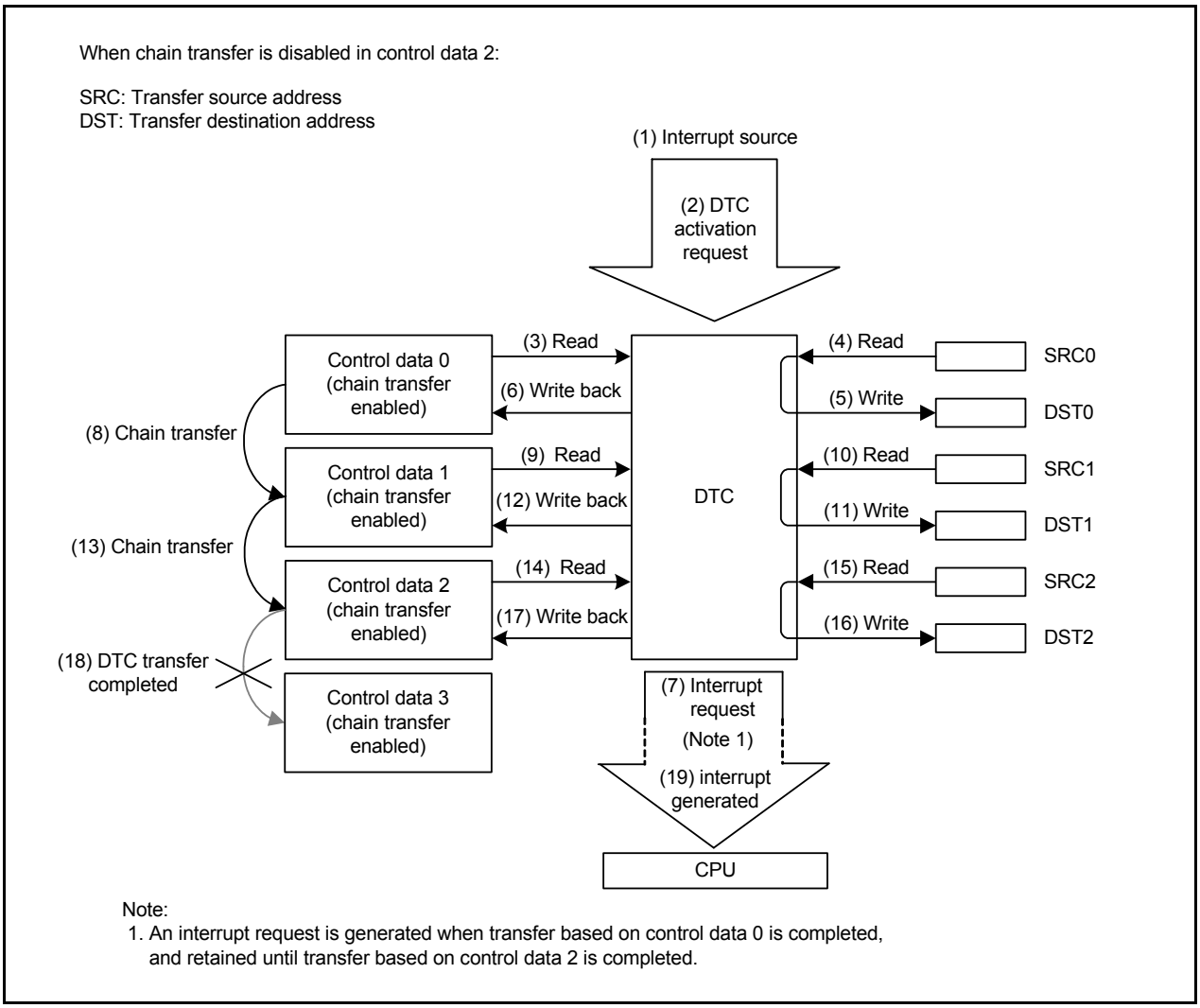


Figure 5.5 Example of Chain Transfer Operation

6. DTC Setting Example

6.1 Setting

This section describes the settings necessary to activate the DTC. The DTC control data area and DTC vector table area are allocated to given addresses (excluding general-purpose registers) on the internal RAM. Store the lower 8 bits of the starting address in the control data to be used (setting value of the DTCBAR register for the higher 8 bits) to the DTC vector address corresponding to the activation source. Then set registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, DTDARj (j = 0 to 23). Set the DTCENi register (i = 0 to 4) to enable or disable DTC activation by an individual interrupt source. When an enabled activation source is generated, the DTC activates.

Figure 6.1 shows the Setting.

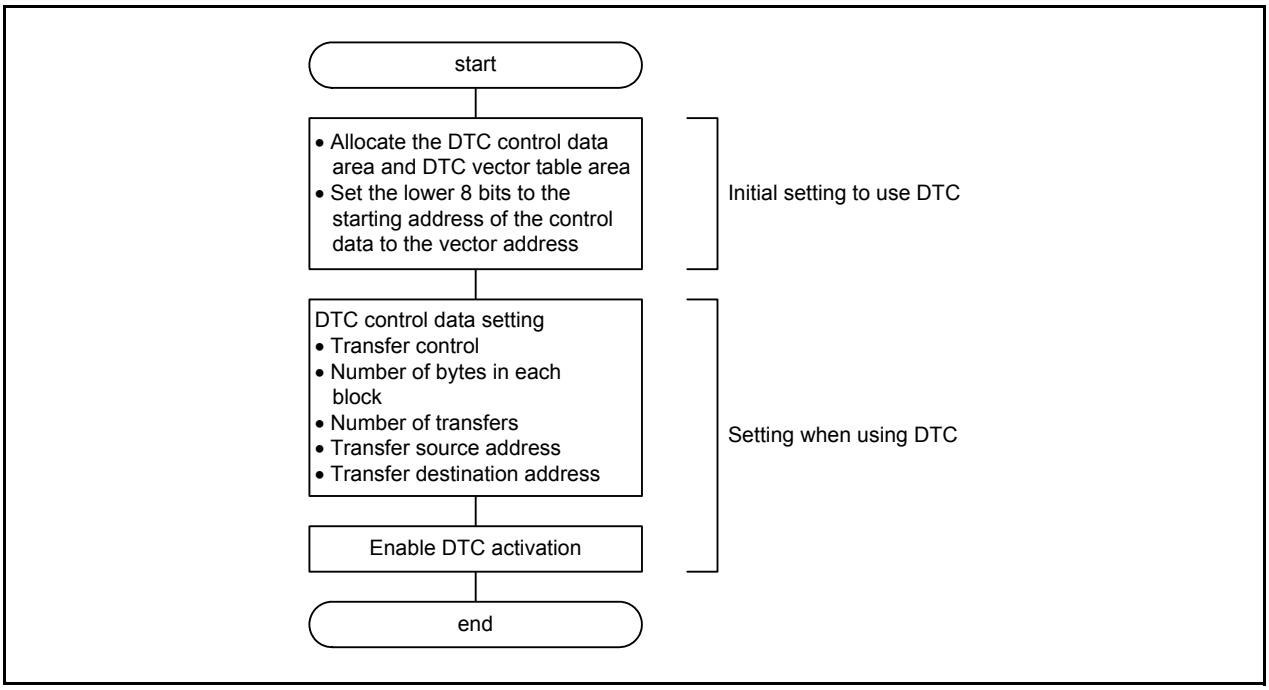


Figure 6.1 Setting

6.1.1 Example of Using DTC

This section describes how to use the DTC and serial array unit (SAU) in conjunction. Data reception by the DTC is performed using UART mode. Every time 1 byte is received, the DTC activates and stores the received data to the variable. A total of 5-byte data is received and DTC transfer is completed. The transfer end interrupt of UART reception is assumed as the DTC activation source.

Table 6.1 lists the Control Data Setting.

Table 6.1 Control Data Setting

Setting Item	Setting Value
	Control data 0
Transfer mode	Normal mode
Transfer source address control	Fixed
Transfer destination address control	Incremented
Chain transfer	Disabled
Number of bytes in transfer block	1 byte
Number of DTC transfers	5
Transfer source address	Serial data register (FFF12H, FFF13H)
Transfer destination address	Receive data storing array (RAM)

(1) Perform an initial setting for the DTC and SAU.
(2) Start receiving data.
(3) After 1-byte reception is completed, DTC transfer starts by the transfer end interrupt request.
(4) Read control data 0. Transfer the serial data register value of the transfer source address to the internal RAM of the transfer destination address. After the transfer, write back control data 0 in which the transfer destination address is updated.
(5) When DTC transfer of which the DTC transfer count register value becomes 00H from 01H, the transfer end interrupt of the DTC activation source is generated.

Figure 6.2 shows a SAU and DTC Used in Conjunction.

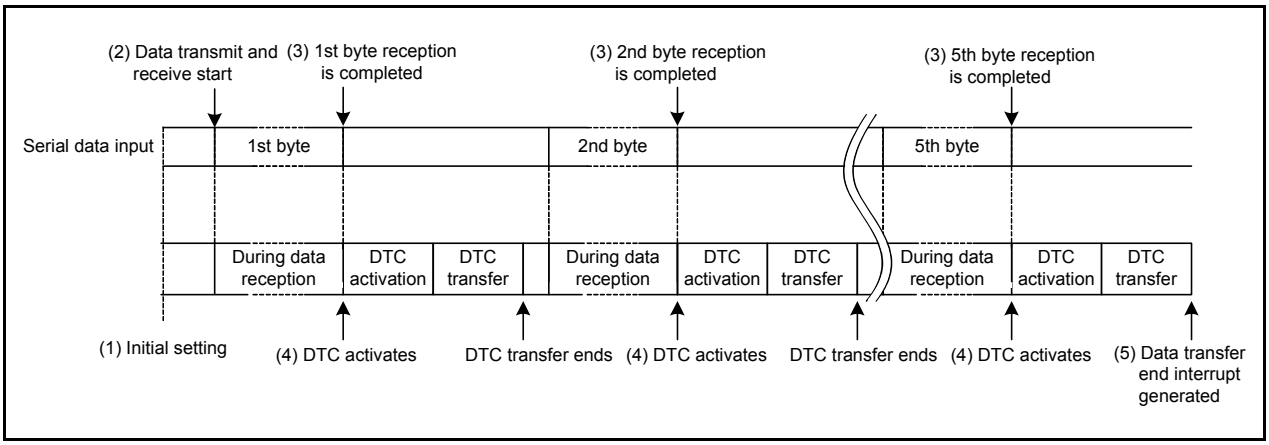


Figure 6.2 SAU and DTC Used in Conjunction

7. Differences with the RL78/G13 DMA Controller

Like the RL78/G14 DTC, the RL78/G13 DMA controller can be activated by a set activation sources and automatically performs data transfer between memories without going through the CPU. Since the DMA controller exclusively includes registers which set transfer addresses and modes for each channel, transfer can be performed at high speed. However, it is limited to transfer between SFRs and internal RAM.
The DTC stores information such as transfer addresses and modes on memories as control data and reads given control data for each activation source to transfer data. Since it takes more time to read and write back control data, DTC transfer time is longer than the DMA controller transfer time, but transfer between given memories can be performed. The DTC includes many channels and activation sources. Multiple transfers can be performed by repeat mode which successively repeats data transfer and chain transfer which in turn performs multiple data transfers by an activation source.

Figure 7.1 shows the Comparison of Data Transfer Processing. Table 7.1 lists Differences between the RL78/G14 DTC and RL78/G13 DMA Controller.

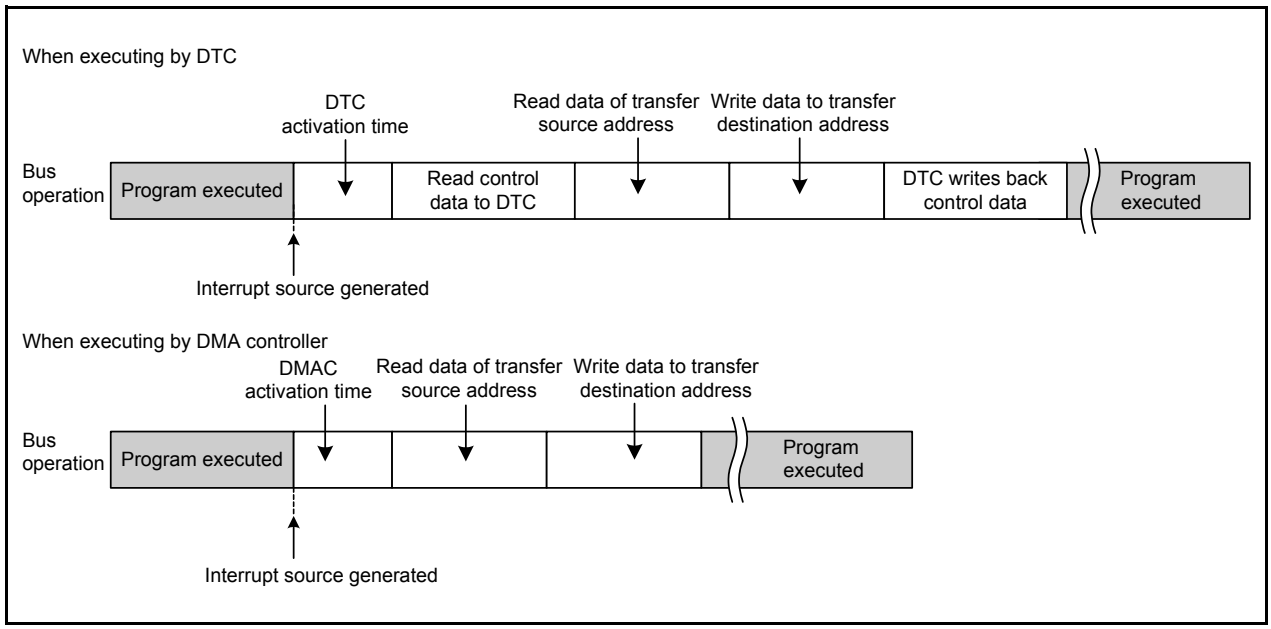


Figure 7.1 Comparison of Data Transfer Processing

Table 7.1 Differences

Item	DTC (RL78/G14)	DMA Controller (RL78/G13)
Number of channels	24 channels	2 channels (20, 24, 25, 30, 32, 36, 40, 44, 48, 52, and 64 pins) 4 channels (80, 100, and 128 pins)
Setting of transfer information	Store to internal RAM and read at each activation	Dedicated registers
The number of bytes in a block per transfer	8 bits: 1 to 256 bytes 16 bits: 2 to 512 bytes	8 bits: 1 byte 16 bits: 2 bytes
Maximum number of transfers	256	1024
Transfer modes	• Normal mode • Repeat mode • Chain transfer	Single transfer mode
Target for transfer	Transfer source address: 1st SFR area, RAM area (excluding general-purpose registers), mirror area (1), data flash memory area (1), 2nd SFR area Transfer destination address: 1st SFR area, RAM area (excluding general-purpose registers), 2nd SFR area	Between SFR and internal RAM
Activation sources	Peripheral function interrupts: Maximum 39 sources	• Activation by software • Peripheral function interrupts: Maximum 18 sources
Transfer pending function by software	None	Included
Standby function	• HALT mode: Operate • SNOOZE mode: Operate • STOP mode: Stop	• HALT mode: Operate • SNOOZE mode: Stop • STOP mode: Stop

Note:

1. In SNOOZE mode, these areas cannot be set as the sources for DTC transfer since the flash memory is stopped.

8. Reference Documents

RL78/G14 User's Manual: Hardware Rev.0.02
RL78/G13 User's Manual: Hardware Rev.0.03
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	RL78/G14 How to Use the DTC for the RL78/G14

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 4, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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