RL78/G12

Voltage Detector (Reset Mode)

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Introduction

This application note describes the reset mode of the voltage detector (LVD) on the RL78/G12. When the supply voltage (V_{DD}) becomes lower than the LVD detection voltage (V_{LVI}), the voltage detector generates an internal reset. Using LEDs, the internal reset can be distinguished from a power-on reset (POR).

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes the operation (reset mode) of the voltage detector.

When the supply voltage (V_{DD}) becomes lower than the LVD detection voltage (V_{LVI}), the voltage detector generates an internal reset. The three LEDs permit a visual distinction between this internal reset and a power-on reset. The indications provided by these LEDs are changed according to the switch input count.

When V_{DD} becomes lower than V_{LVI}, the voltage detector generates an internal reset. Later, when V_{DD} becomes equal to or higher than V_{LVI}, this reset is ended. At this time, the system restarts from the state it was in when the LEDs provided the last indications.

When V_{DD} becomes lower than V_{PDR} (POR power-supply falling-edge voltage), an internal reset occurs due to a power-on reset. Later, when V_{DD} becomes equal to or higher than V_{LVI}, this internal reset is ended and the system restarts while all the LEDs are off.

Table 1 lists the peripheral functions to be used and their uses. Figure 1.1 shows the outline of the operation (reset mode) of the voltage detector.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
LVD	Supply voltage (V_{DD}) monitoring
P137/INTP0	Switch input
P12 to P14	LED lighting control (for LED0 to LED2)

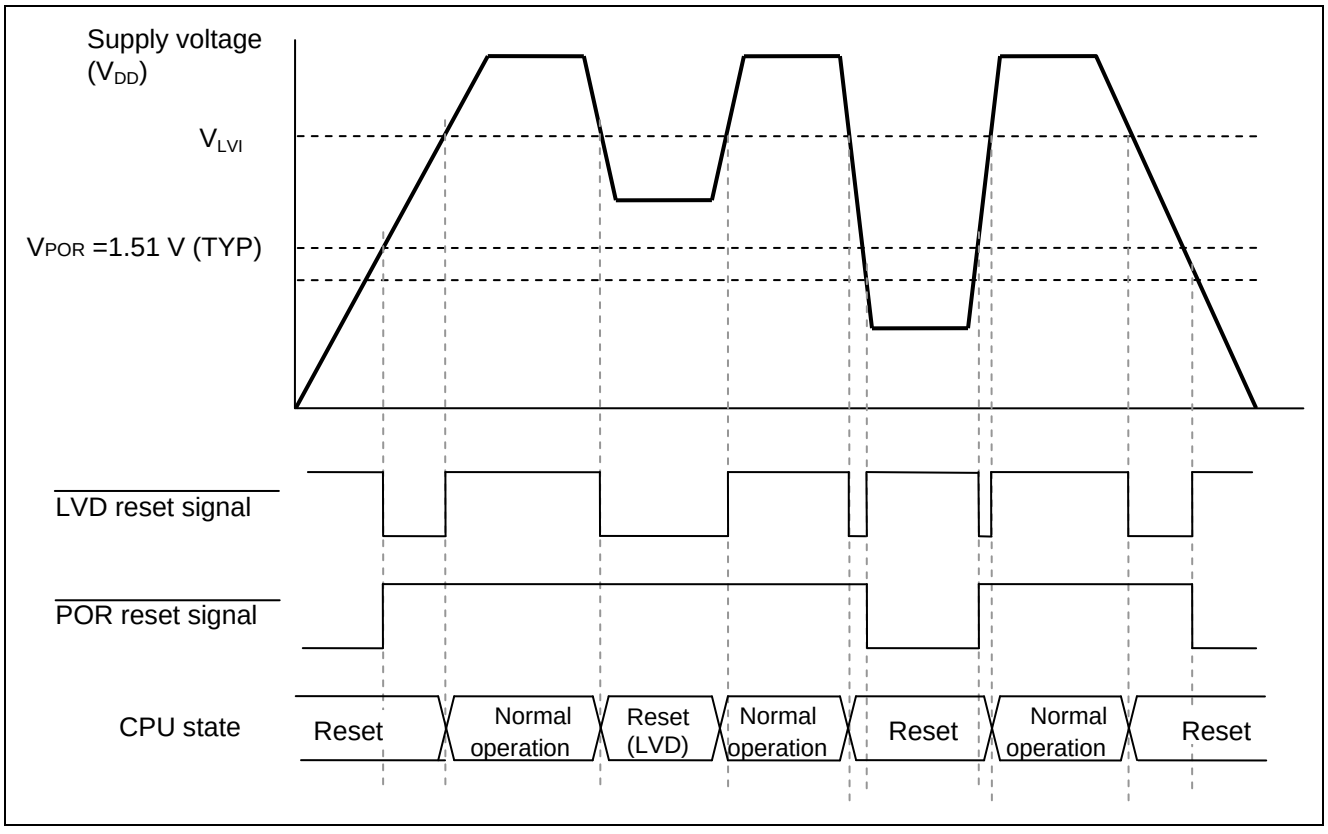


Figure 1.1 Overview of LVD Operation (Reset Mode)

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 to 5.5 V.) LVD operation (V_{LVI}): Reset mode • Rising-edge voltage: 2.81 V (2.76 to 2.87 V) • Falling-edge voltage: 2.75 V (2.70 to 2.81V)
Integrated development environment	CubeSuite+ V1.01.01 from Renesas Electronics Corp.
Assembler	RA78K0R V1.50 from Renesas Electronics Corp.
Board to be used	RL78/G12 target board (QB-R5F1026A-TB) +LED

3. Related Application Notes

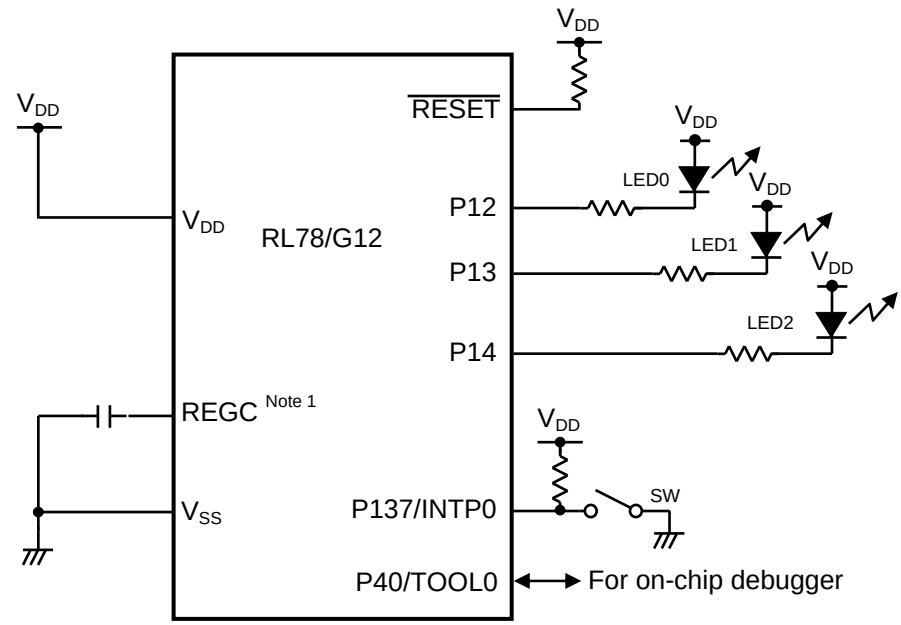
The application note related to this application note is listed below for reference.

RL78/G12 Initialization (R01AN1030E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.



Note 1. Only for 30-pin products.

Figure 4.1 Hardware Configuration

Caution The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P12	Output	LED on (LED0) control port
P13	Output	LED on (LED1) control port
P14	Output	LED on (LED2) control port
P137/INTP0	Input	Switch input port

5. Description of the Software

5.1 Operation Outline

The sample program described in this application note monitors the supply voltage using the voltage detector (reset mode).

When V_{DD} becomes lower than V_{LVI}, the voltage detector generates an internal reset. At this time, various registers are initialized. However, when V_{DD} is higher than V_{PDR}, the on-chip RAM retains the state in which it was before the reset generation. Because the on-chip RAM holds the switch input count which was obtained before the reset generation, the system can restart from the state it was in when the LED indications were provided before the reset generation.

Note that the switch input count is initialized when a reset other than the LVD reset occurs.

(1) Initializing the voltage detector

<Conditions for setting>

- When the power is turned on or after the reset is ended, the option byte should be referenced automatically and the voltage detector should be set to reset mode.
- The rising-edge detection voltage should be set to 2.81 V. The falling-edge detection voltage should be set to 2.75 V.

Caution: When reset mode is selected, writing to the voltage detection level register (LVIS) is prohibited. The initial value for the LVIS register is set to 81H (low-voltage detection level: V_{LVI} for reset mode) automatically.

(2) Setting the input and output ports

LED lighting control (for LED0 to LED2): Set P12, P13 and P14 to the output ports.
Switch input: Set P137/INTP0 for detecting INTP0 falling edges (via an external pull-up resistor)

(3) LED indications depending on the switch input count

Interrupt processing is started upon detection of a P137/INTP0 falling edge. Chattering is detected and, if the on state of the input lasts about 10 ms, it is recognized as a switch input and the LED indications are changed. When VDD becomes lower than VLVI, an LVD reset is generated; however the on-chip RAM's state remains unchanged since before the reset generation (see note 1.).

(4) When V_{DD} becomes lower than V_{PDR}, a POR internal reset occurs and the LED indication data is deleted.

Note 1. This program reads values in RAM after an LVB reset is ended. In order to prevent a reset by the RAM parity error detection function at this time, disable this function.

Caution: For information about the precautions in using the device, refer to RL78/G12 User's Manual: Hardware.

Figure 5.1 shows the outline of the sample code operation.

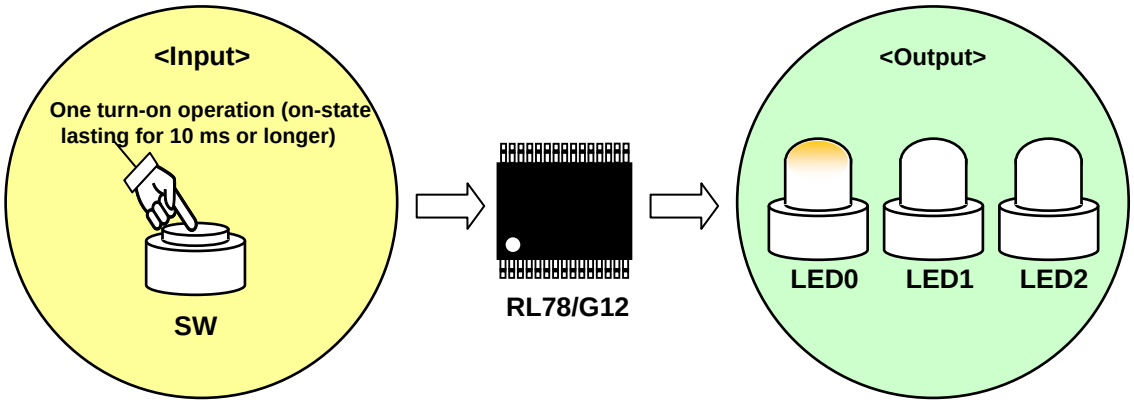


Figure 5.1 Overview of Sample Code Operation

Switch (SW) input count Note 1	LED indications		
	LED0	LED1	LED2
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON

Note 1: For the eighth and subsequent operations, the above LED indications are repeated.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	01111111B	LVD reset mode Rising-edge voltage: 2.81 V (2.76 V to 2.87 V) Falling-edge voltage: 2.75 V (2.70 V to 2.81 V)
000C2H	11100000B	HS mode HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Variables

Table 5.2 lists the global variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
8 bits	RSWCNT	SW depress count (complement)	main IINTP0

5.4 List of Functions (Subroutines)

Table 5.3 lists the functions (subroutines).

Table 5.3 List of Functions (Subroutines)

Function Name	Outline
RESET_START	Initializes the CPU (port clock external interrupt) and starts the main processing.
SINIPORT	Initializes the input and output ports.
SINICLK	Sets the clock generation circuit setting.
SINIINTP0	Initializes the external interrupt settings.

5.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] SINIPORT

Synopsis	Initializes the input and output ports.
Explanation	LED lighting control (for LED 0 to LED2): This function sets P12, P13 and P14 to the output ports.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIINTP0

Synopsis	Initializes the external interrupt settings.
Explanation	This function initializes the external interrupt settings. This function clears the interrupt request.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINICLK

Synopsis	Sets the clock generation circuit.
Explanation	This function sets the operation clock to HOCO 24 MHz.
Arguments	None
Return value	None
Remarks	None

5.6 Flowcharts

Figure 5.2 shows the overall flow of the sample program described in this application note.

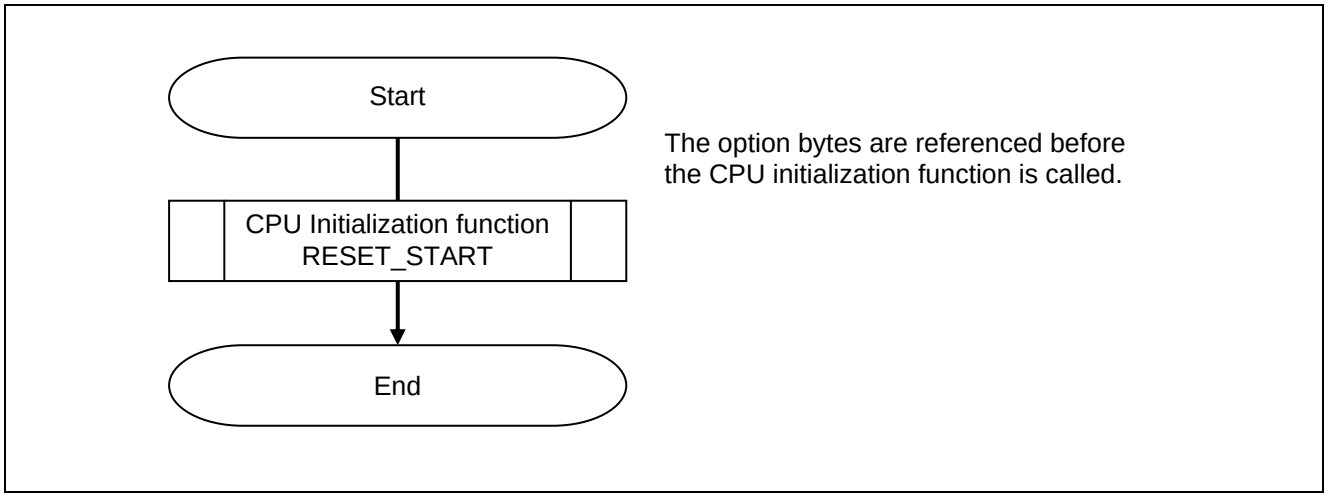


Figure 5.2 Overall Flow

5.6.1 CPU Initialization Function

Figure 5.3 shows the flowchart for the CPU initialization function.

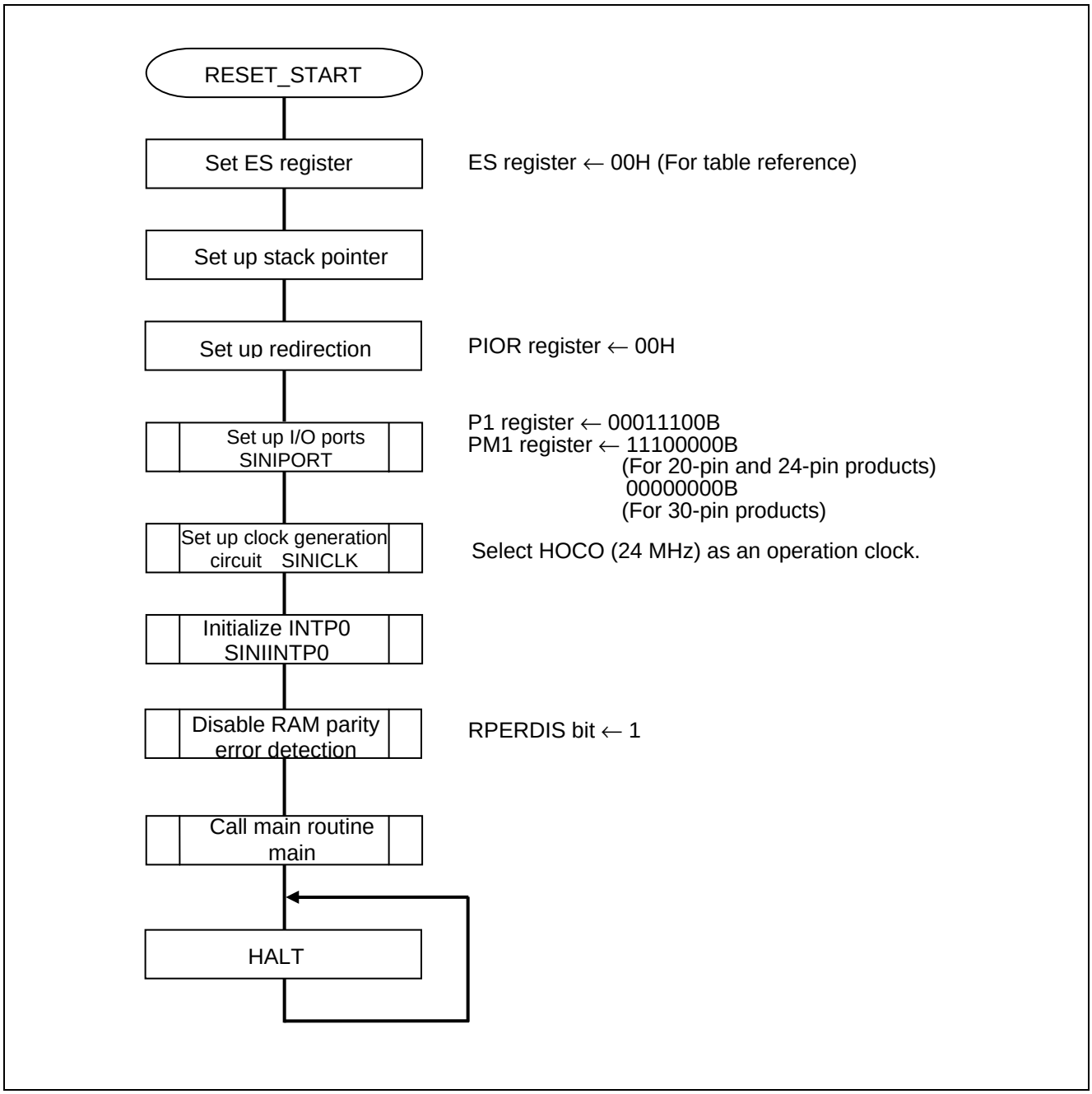


Figure 5.3 CPU Initialization Function

5.6.2 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

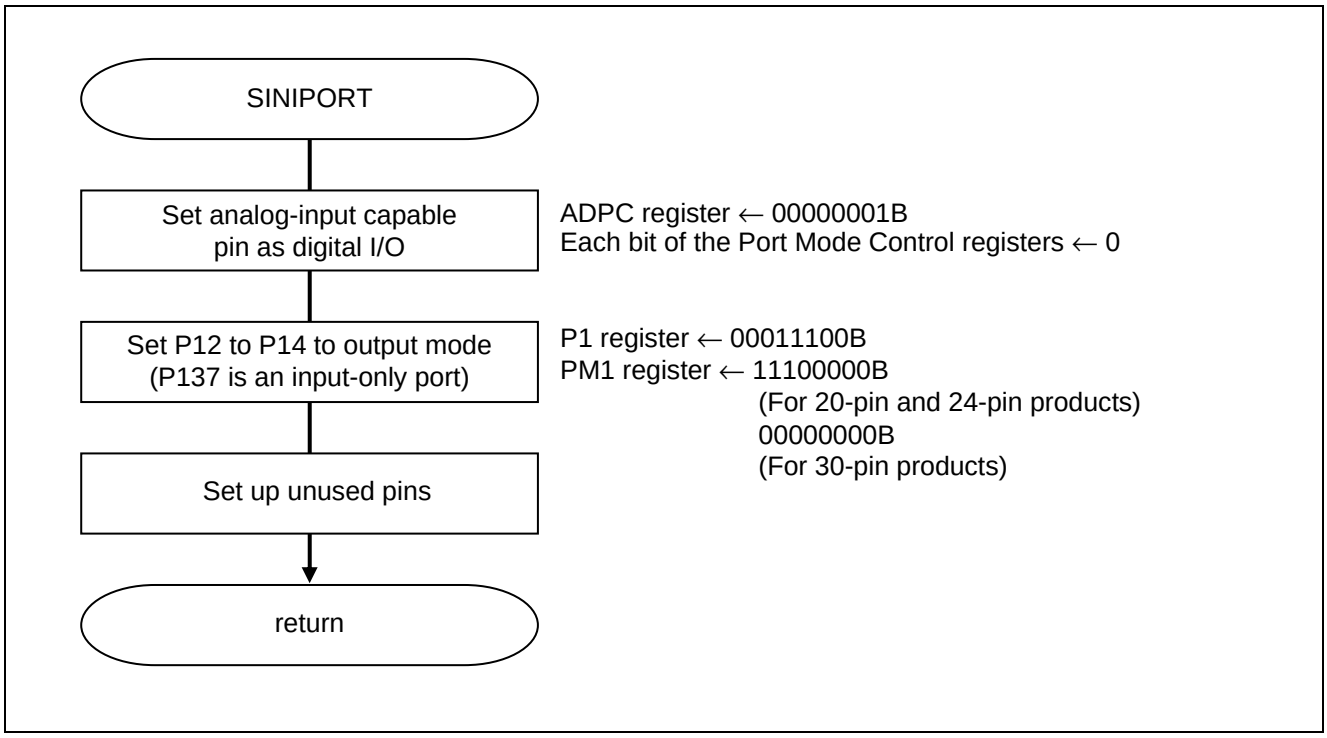


Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.6.3 Clock Generation Circuit Setup

Figure 5.5 shows the flowchart for clock generation circuit setup.

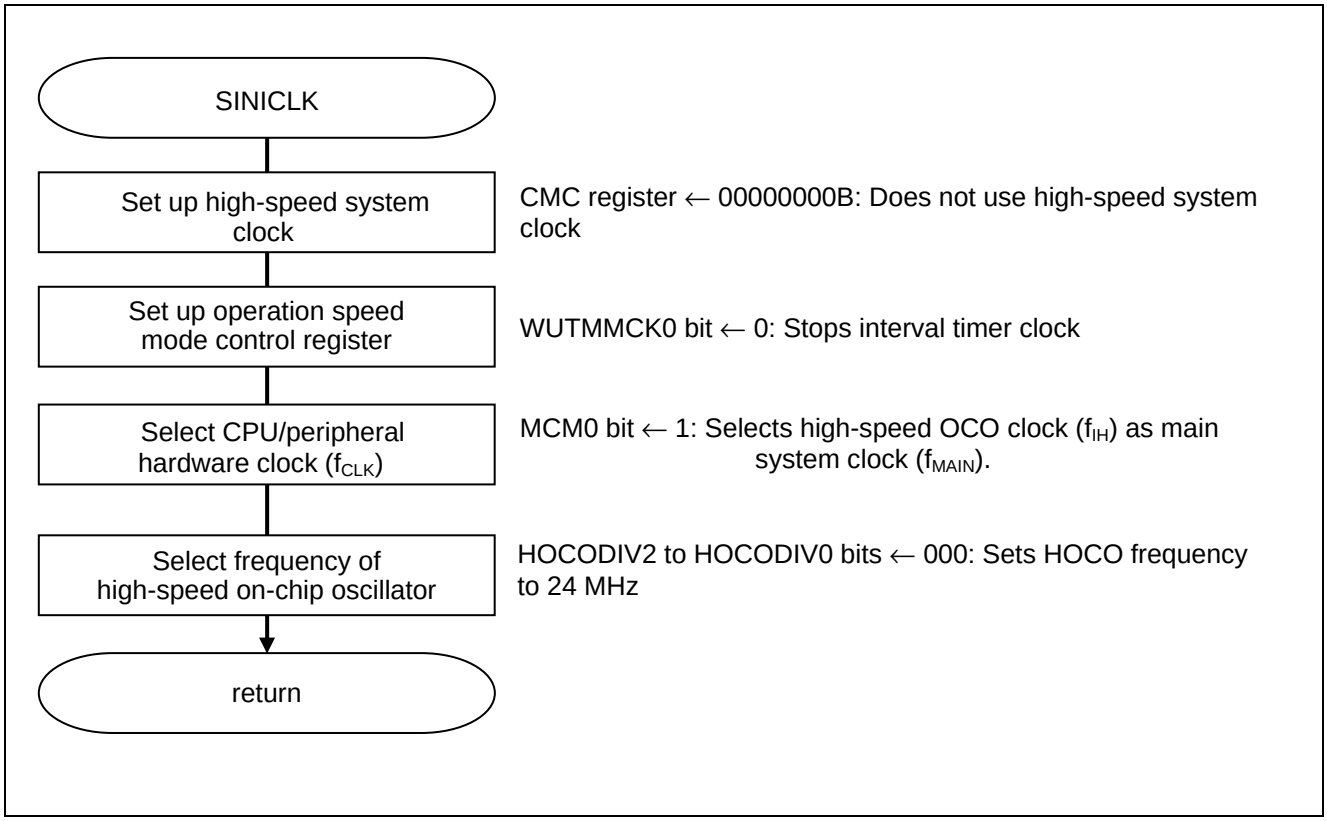


Figure 5.5 Clock Generation Circuit Setup

Caution: For details on the procedure for setting up the clock generation circuit (SINICLK), refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E).

5.6.4 INTP0 Initialization

Figure 5.6 shows the flowchart for INTP0 initialization.

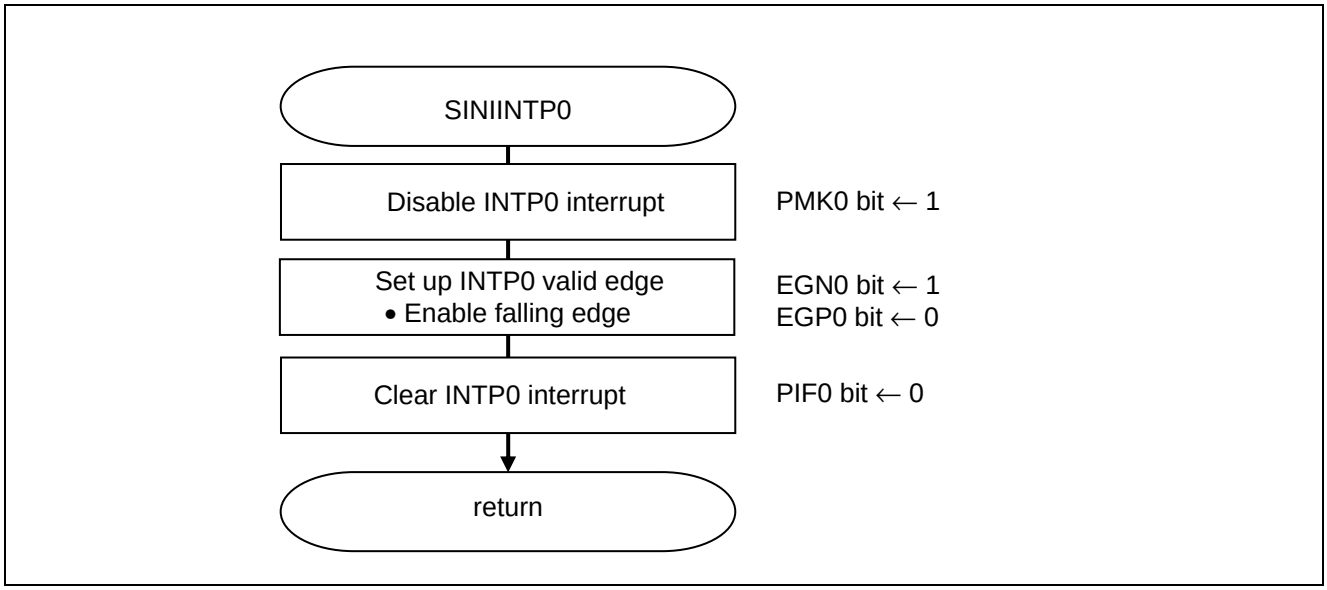


Figure 5.6 INTP0 Initialization

(1) Setup for INTP0 pin edge detection

- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)

Select a valid edge for INTP0 to INTP11

Symbol: EGP0

7	6	5	4	3	2	1	0
0	0	0 Note 1	0 Note 1	EGP3	EGP2	EGP1	EGP0
0	0	0	0	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
0	0	0 Note 1	0 Note 1	EGN3	EGN2	EGN1	EGN0
0	0	0	0	x	x	x	**1**

Note 1. For 20-pin and 24-pin products.

Bit 0

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.6.5 Main Processing

Figure 5.7 shows the flowchart for main processing.

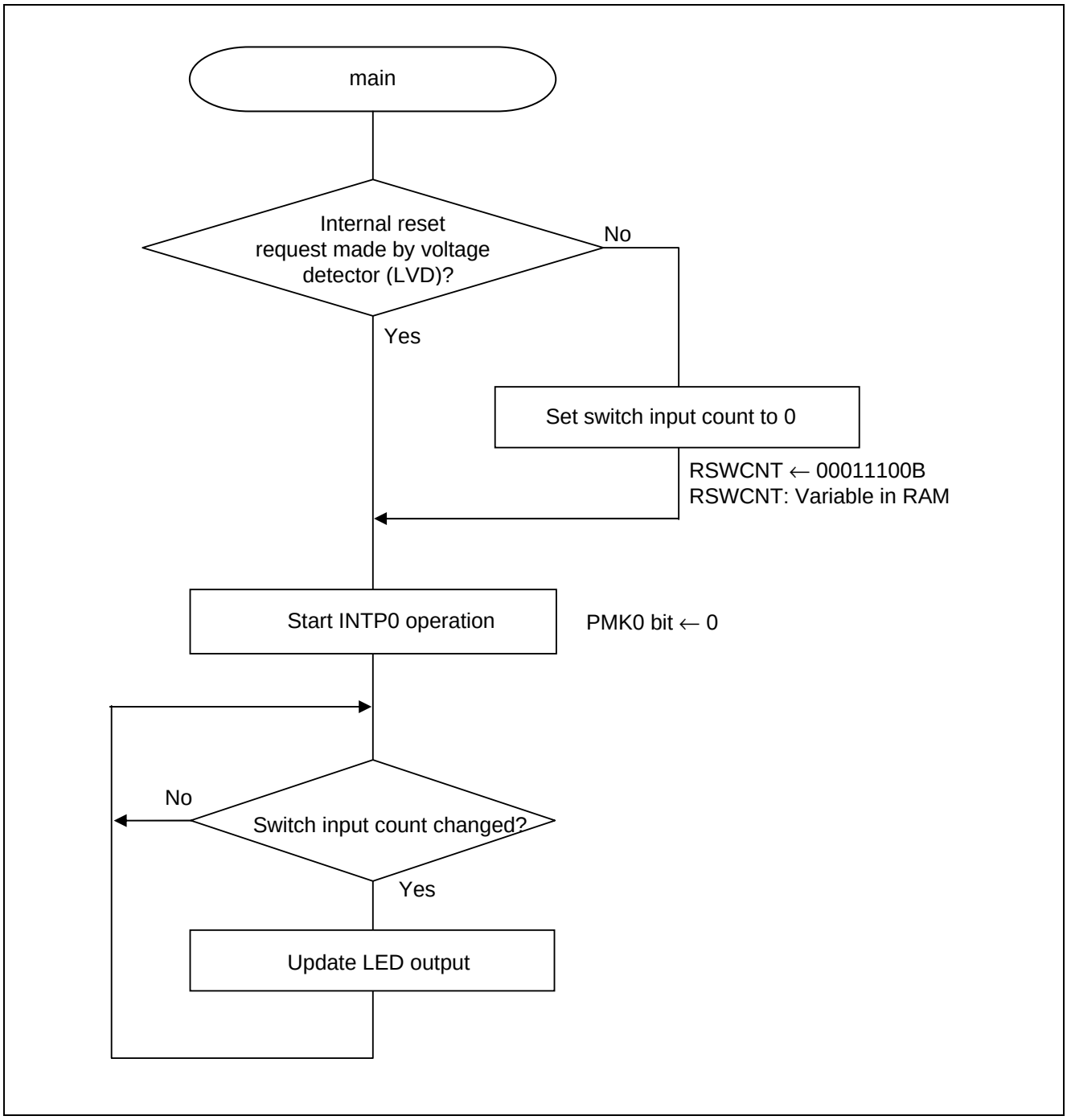


Figure 5.7 Main Processing

5.6.6 INTP0 Interrupt Processing

Figure 5. shows the flowchart for INTP0 interrupt processing.

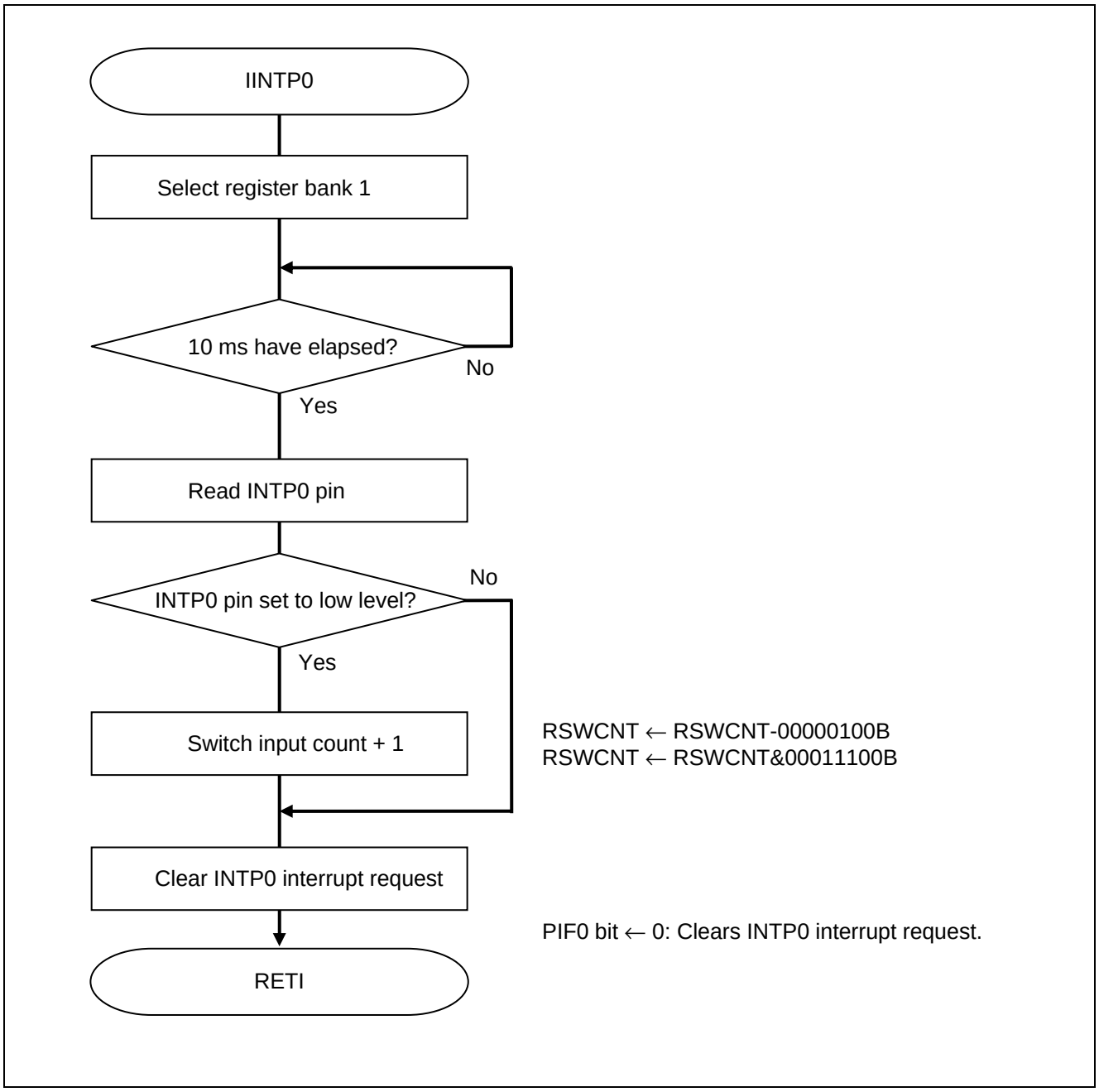


Figure 5.8 INTP0 Interrupt Processing

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G12 User's Manual: Hardware (R01UH0200E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record	RL78/G12 Voltage Detector (Reset Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 1. 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
  - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
  - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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