

RL78/G12

R01AN1373EJ0100

Rev. 1.00

Timer Array Unit (PWM Output)

Mar.01, 2013

Introduction

This application note describes the PWM output function of the timer array unit (TAU). This unit changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

This application note describes the PWM output function which is realized using channel 0 as the master and channel 1 as the slave in simultaneous channel operation mode. The brightness of the LEDs is controlled by connecting the PWM output to LED2 (for PWM output). Timing signals with fixed cycle time (500 ms) are created by counting the number of timer interrupts (INTTM00) generated by channel 0. Using these timing signals, the duty ratio of the PWM output is changed and the output of LED1 (for updating) is inverted.

Table 1.1 shows the required peripheral function and its use. Figure 1.1 presents an overview of the PWM output operation. Table 1.2 shows the relation between PWM output duty ratios and LED brightnesses. Figure 1.2 is a simplified timing chart which summarizes the PWM output operation.

Table 1.1 Required Peripheral Function and Its Use

Peripheral function	Use
Timer array unit 0	This unit is used to realize the PWM function by operating channel 0 and channel 1 together and deliver a PWM output from the TO01 pin.

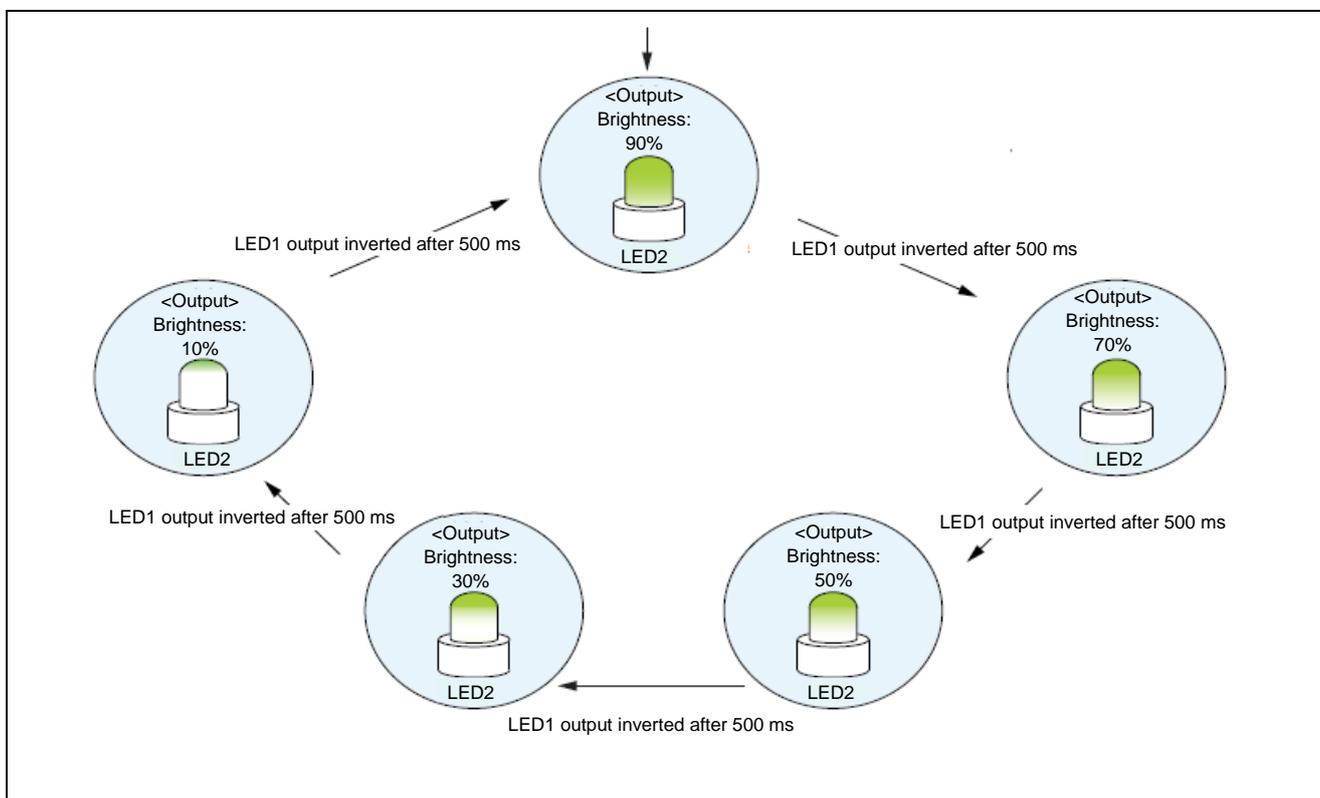


Figure 1.1 Overview of PWM Output Operation

Table 1.2 Relation between PWM Output Duty Ratios and LED Brightnesses

Duty ratio	LED2 brightness
10%	90%
30%	70%
50%	50%
70%	30%
90%	10%

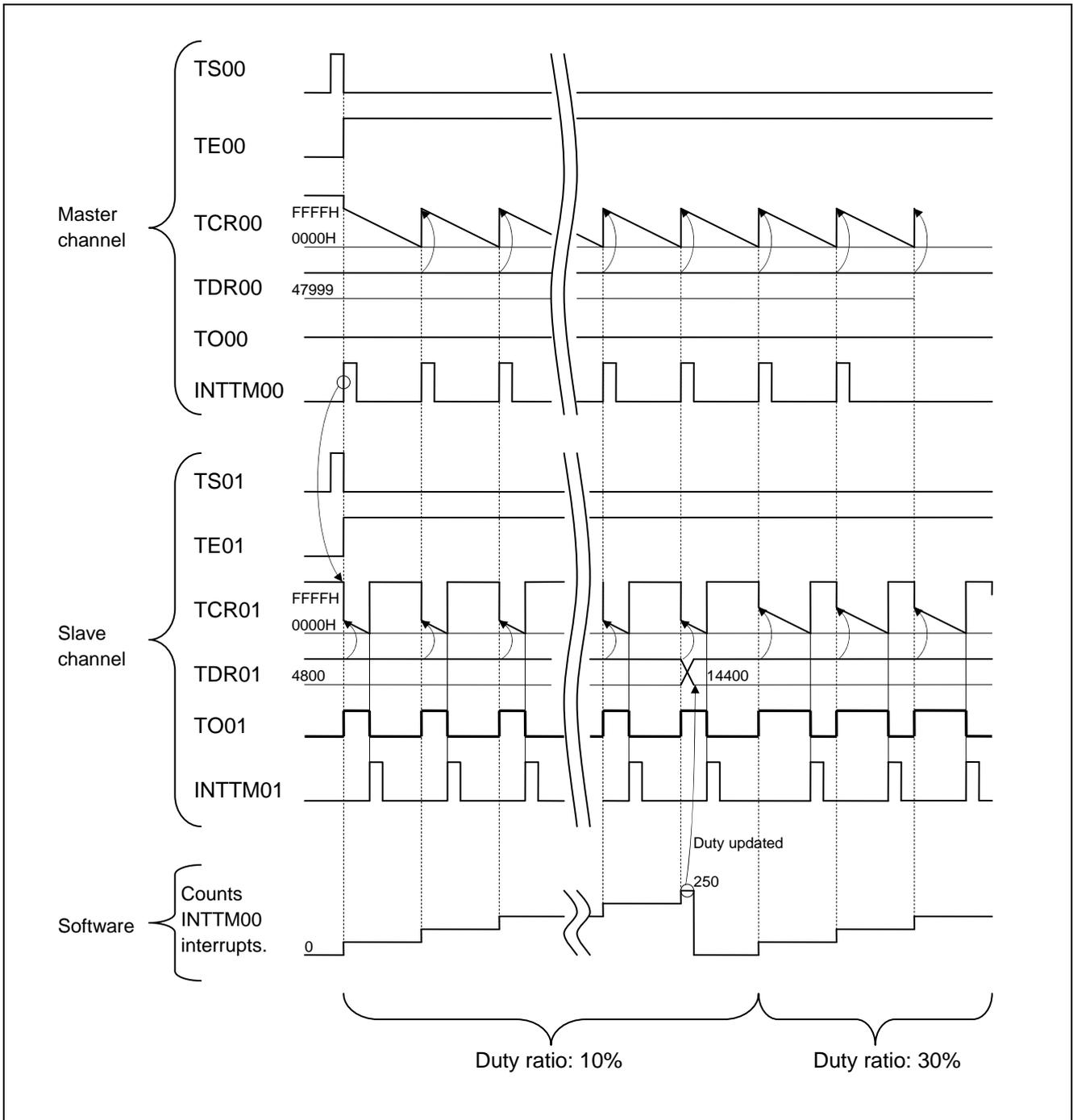


Figure 1.2 Simplified Timing Chart for PWM Output Operation

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	<ul style="list-style-type: none"> • High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVI}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment	CubeSuite+ V1.01.00 from Renesas Electronics Corp.
Assembler	RA78K0R V1.50 from Renesas Electronics Corp.
Board to be used	RL78/G12 target board (QB-R5F1026A-TB)

3. Related Application Note

The application notes that are related to this application note are listed below for reference.

RL78/G12 Initialization (R01AN1030E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

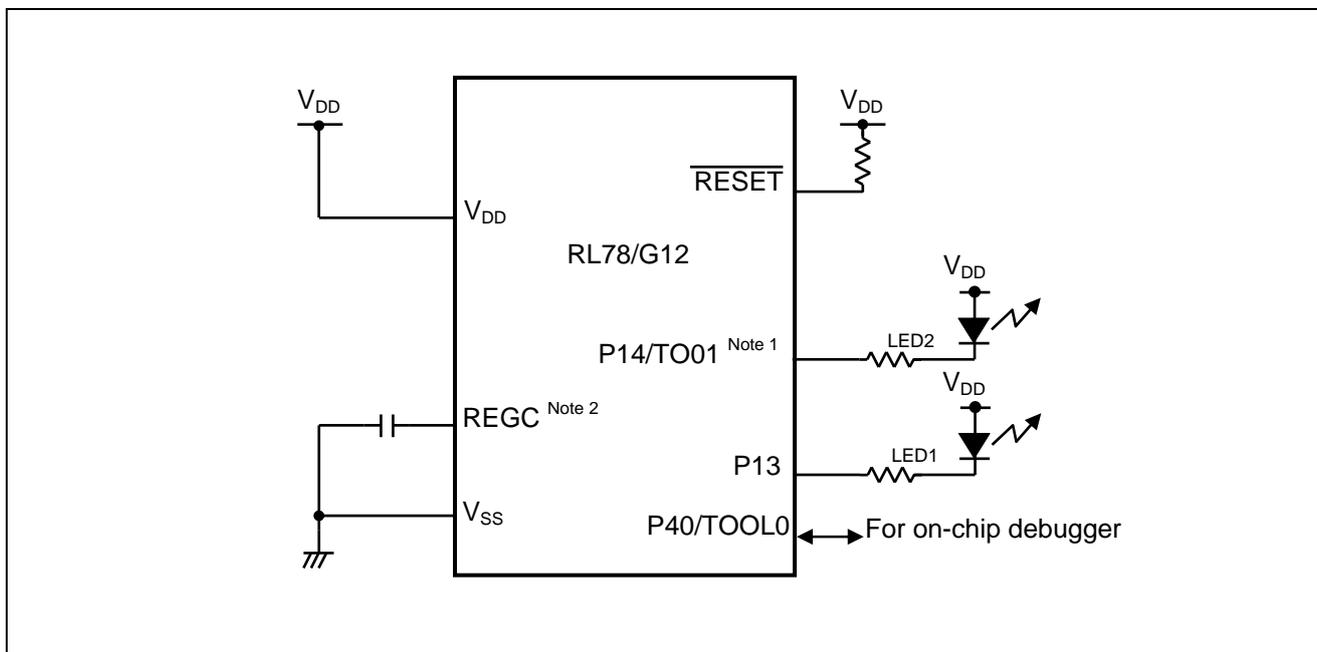


Figure 4.1 Hardware Configuration

Notes: 1. For 20-pin and 24-pin products. P16/TO01 for 30-pin products.

2. Only for 30-pin products.

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P14/TO01 ^{Note}	Output	PWM output (LED2) port
P13	Output	Output port for LED1 indications

Note: For 20-pin and 24-pin products. P16/TO01 for 30-pin products.

Caution: The products to be exemplified hereafter are 20-pin products, unless it is explicitly stated otherwise.

5. Description of the Software

5.1 Operation Outline

The sample program covered in this application note implements PWM by operating channel 0 and channel 1 together, and delivers a PWM output from P14/TO01.

Also, this program detects 250 timer interrupts (INTTM00) with 2-ms cycle time which are generated by channel 0. Then, it changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

(1) Initialize the TAU.

<Conditions for setting>

- Set the P14/TO01 pin to a PWM output.
- Set TAU0 channel 0 to 2-ms cycle interval timer mode. ^{Note 1}
- Set TAU0 channel 1 to one-count mode.
- Initialize the duty ratio of the PWM output to 10%. ^{Note 2}
- Use timer interrupts (INTTM00) from timer channel 0.

(2) Operation starts when both the operation enable trigger bits for TAU0 channel 0 and channel 1 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

(3) After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at 2 ms intervals.

(4) When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, the sample program starts counting the number of INTTM00 interrupts generated. After channel 0 has generated 250 timer interrupts (i.e., after 500 ms), the sample program updates the channel 1 count value and changes the duty ratio. This duty ratio is increased from 10% to 90% (10% → 30% → 50% → 70% → 90%). It is incremented by 20% each time the number of channel 0 timer interrupts (INTTM00) generated reaches 250 ^{Note 3}. (Thus, it is incremented at 500 ms intervals) It is reset to 10% after the duty ratio to be set next exceeds 100%. ^{Note 2}

(5) After processing timer interrupts (INTTM00) from channel 0, the sample program executes another HALT instruction and waits for the next timer interrupt (INTTM00) from channel 0.

Notes. 1: Constant INTERVAL is defined as 2 (ms) at initial setting (r_init.asm).

2. Constant INITIAL is defined as 10 (%) at initial setting (r_init.asm).

3. Constant INCREMENT is defined as 20 (%) at initial setting (r_init.asm).

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	01111111B	LVD reset mode, 2.81 V (2.76 to 2.87 V)
000C2H	11100000B	HS mode, HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constant

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constant for the Sample Program

Constant	Setting	Description
INTERVAL	2	Cycle of PWM output in units of ms
INITIAL	10	Duty ratio of PWM in units of percent
INCREMENT	20	Increment in duty ratio of PWM in units of percent
PERIOD	$24000 * \text{INTERVAL}$	Number of clocks corresponding to duty ratio of PWM
INCDATA	$(\text{PERIOD} / 100) * \text{INCREMENT}$	Number of clocks corresponding to increment in duty ratio of PWM
INITDATA	$(\text{PERIOD} / 100) * \text{INITIAL}$	TDR01 setting for a 10% duty ratio

5.4 List of Variables

Table 5.3 lists the variables that are used in this sample program.

Table 5.3 Variables for the Sample Program

Variable Name	Outline
RTMCNT	Used to detect an elapse of 500 ms by counting occurrence of INTTM00 at an interval of 2 ms

5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines) that are used in this sample program.

Table 5.4 Functions (Subroutines)

Function	Outline
SSTARTPWM	Timer array unit start processing
INTTM00	TAU0 channel 0 timer interrupt processing

5.6 Function (Subroutine) Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] SSTARTPWM

Synopsis	TAU0 channel 0 start processing
Explanation	This function starts count operation of channels 0 and 1 and unmask TAU0 channel 0 interrupts.
Arguments	None
Return value	None
Remarks	None

[Function Name] INTTM00

Synopsis	Channel 0 timer interrupt processing
Explanation	This function counts the number of INTTM00 interrupts generated. Each time the count reaches 250, it updates the duty ratio of a PWM output. (Thus, it updates the duty ratio at 500-ms intervals)
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

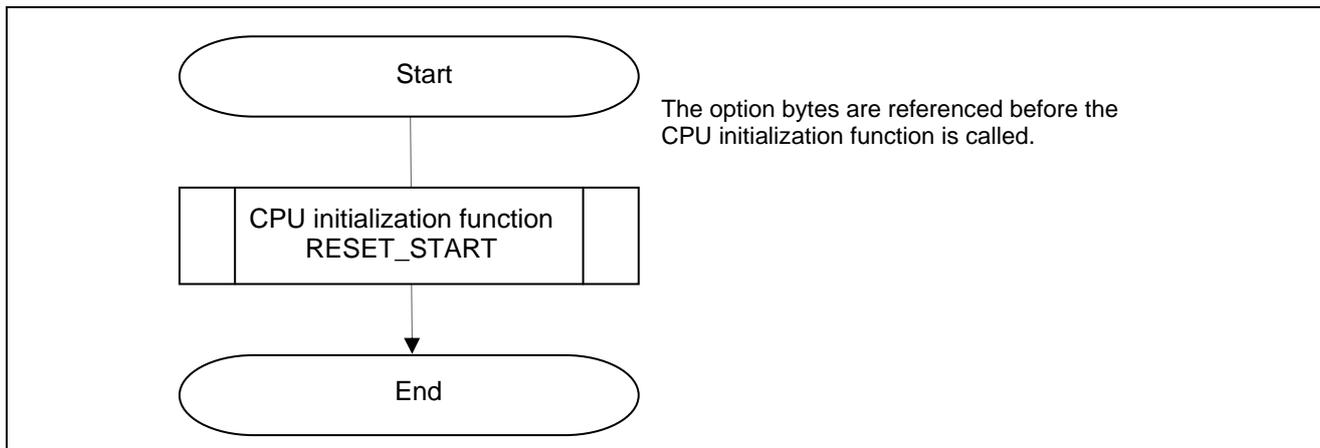


Figure 5.1 Overall Flow

5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

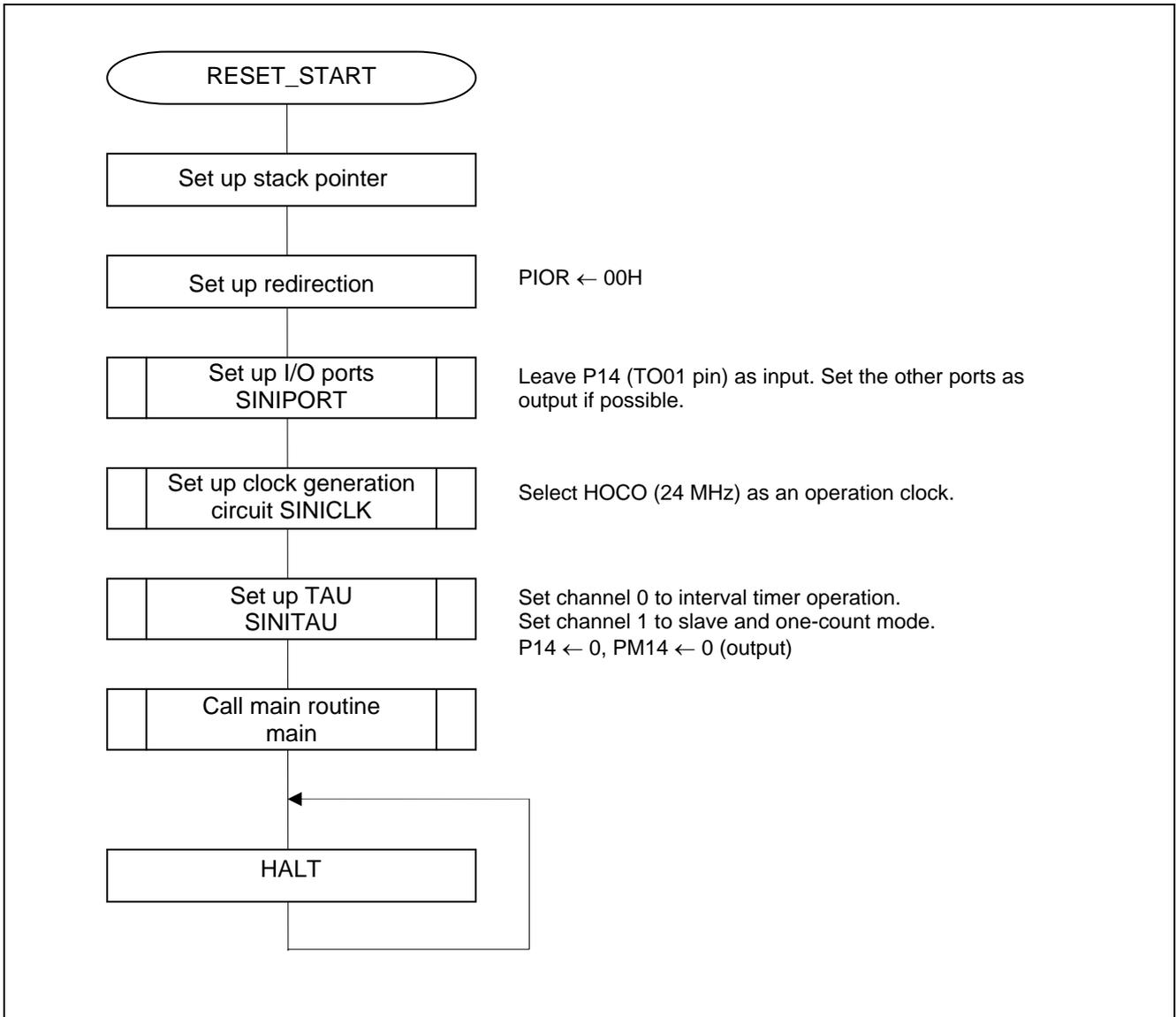


Figure 5.2 CPU Initialization Function

5.7.2 I/O Port Setup

Figure 5.3 shows the flowchart for setting up the I/O ports.

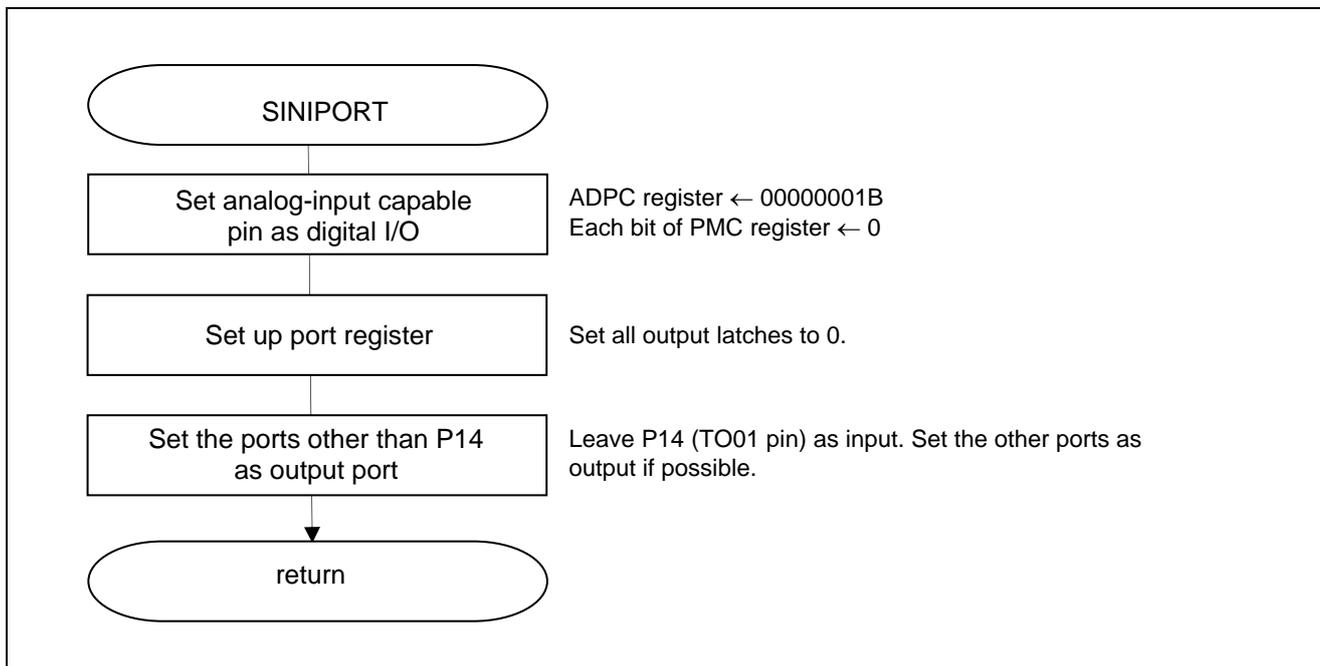


Figure 5.3 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED pin to indicate updating of the duty ratio

- Port mode register (PM1)
Select I/O mode for PM10.

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	x	x	0

Bit 0

PM10	PM10 I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.

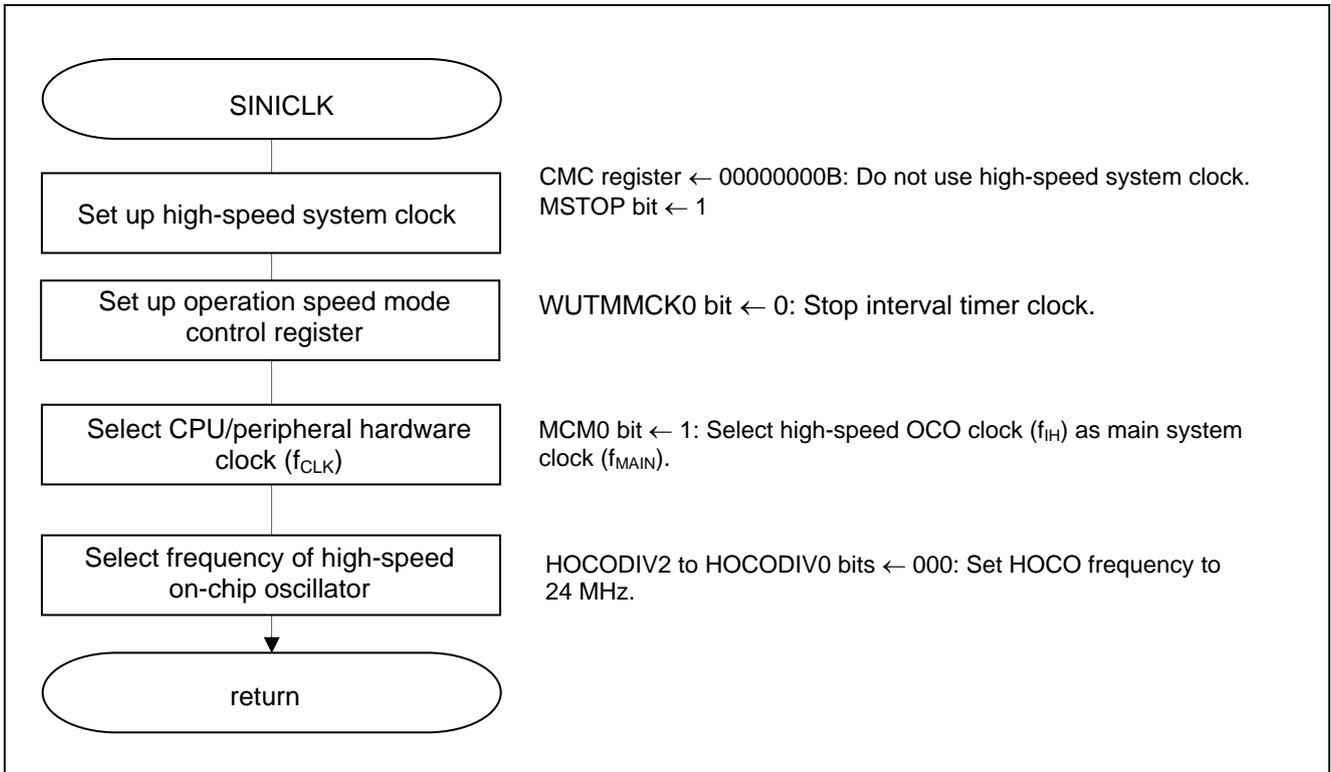


Figure 5.4 Clock Generation Circuit Setup

Caution: For details on the procedure for setting up the clock generation circuit (SINICKL), refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN1030E).

5.7.4 Timer Array Unit Setup

Figure 5.5 shows the flowcharts for setting up the timer array unit.

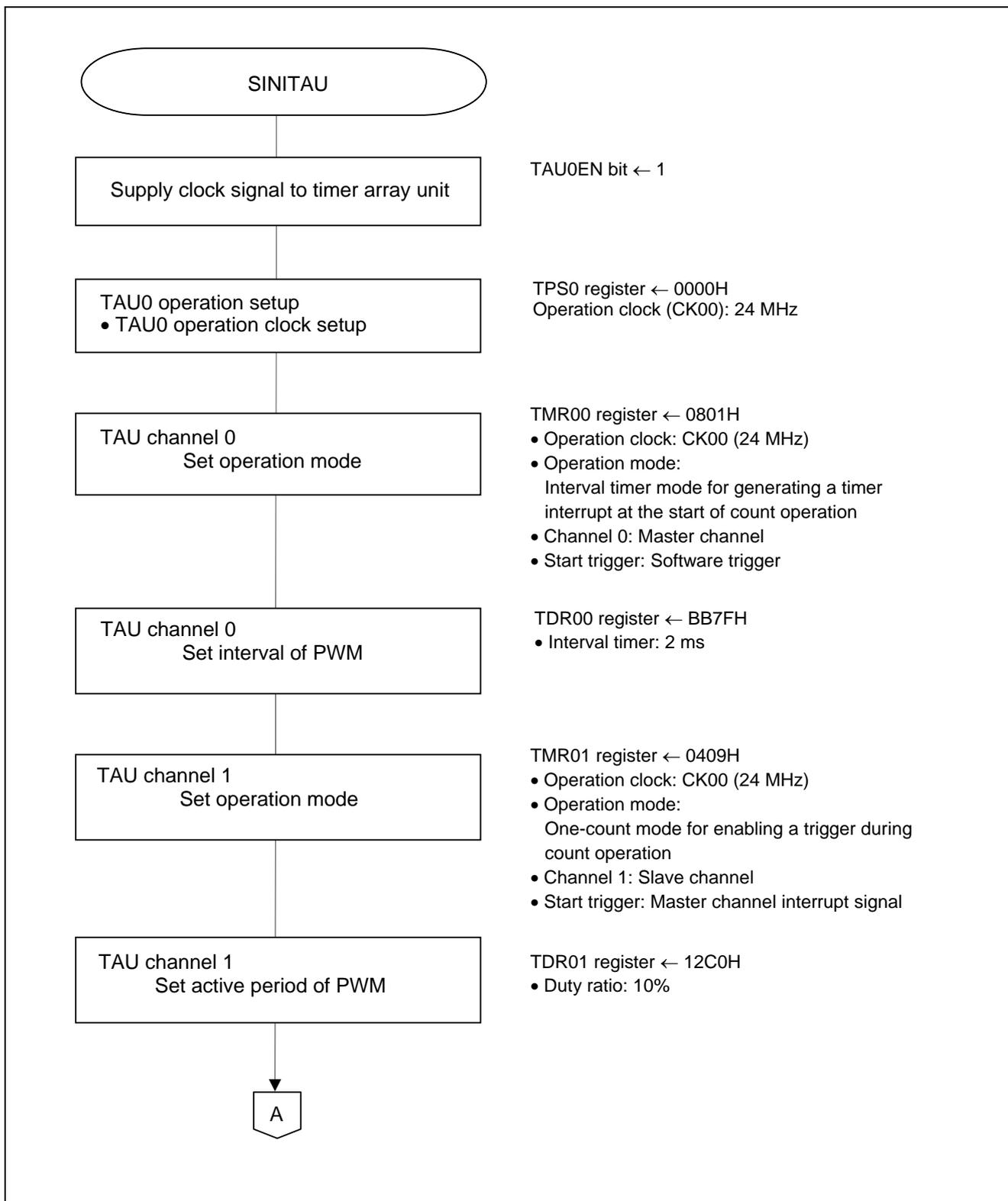


Figure 5.5 Timer Array Unit Setup (1/2)

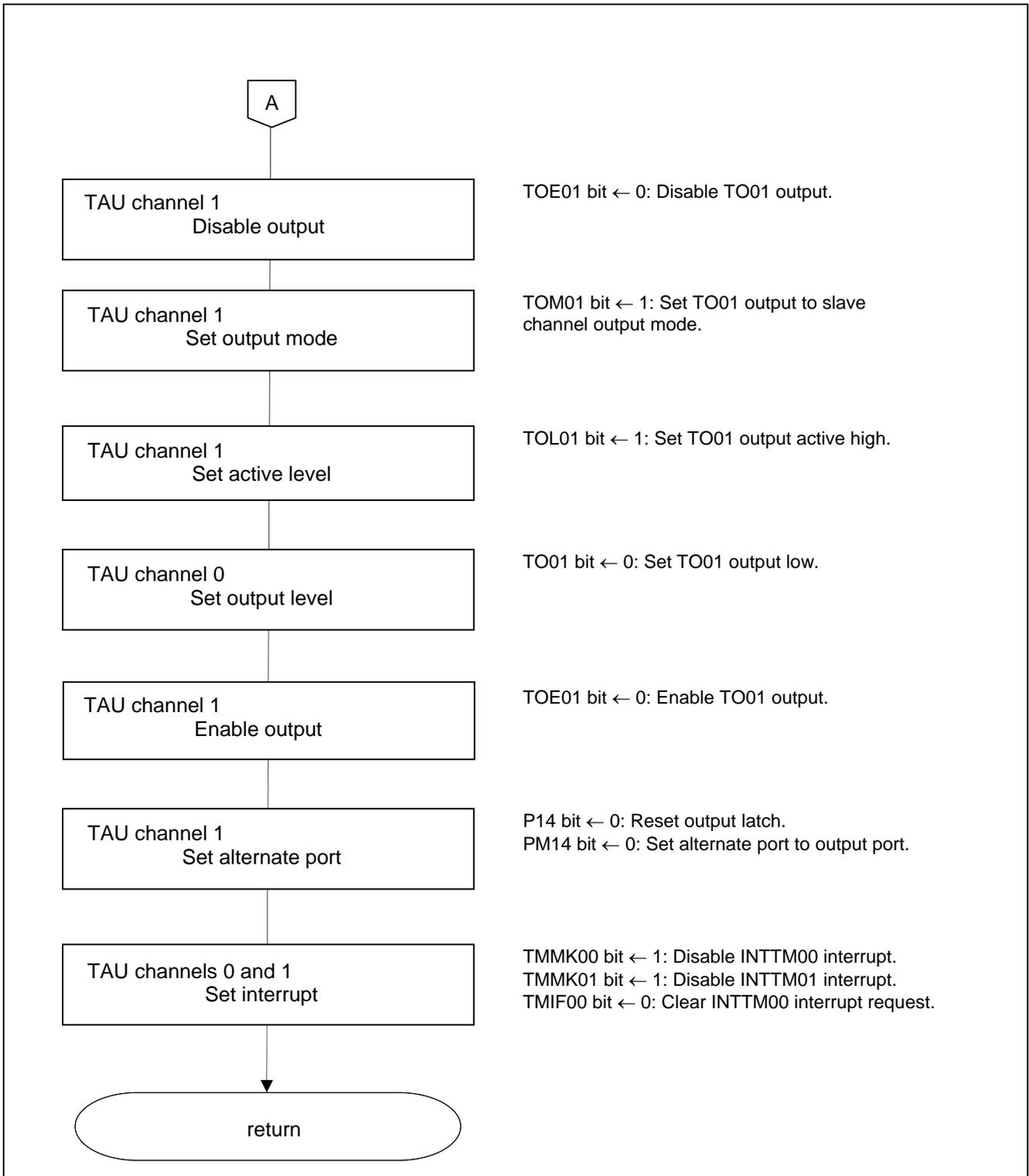


Figure 5.5 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAE	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
x	x	x	x	x	x	0	1

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
				f_{CLK}	$f_{CLK} = 2 \text{ MHz}$	$f_{CLK} = 5 \text{ MHz}$	$f_{CLK} = 10 \text{ MHz}$	$f_{CLK} = 20 \text{ MHz}$	$f_{CLK} = 24 \text{ MHz}$
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	0.75 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.75 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.88 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	23.44 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	11.72 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.47 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)
 - Select an operation clock (f_{MCK}).
 - Select a count clock.
 - Select a start trigger and capture trigger.
 - Select a valid edge for timer input.
 - Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	MAS TER00	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS_{mn0} and CKS_{mn1} bits
1	Valid edge of input signal input from the TI00 pin

Bit 11

MASTER00	Selection between using channel 0 independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	MAS TER 00	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	MAS TER 00	STS 002	STS 001	STS 000	CIS0 01	CIS0 00	0	0	MD0 03	MD0 02	MD0 01	MD0 00
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Bits 3 to 0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Related function	TCR counting operation
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD000 bit operation varies depending on the operation mode (see the table below)

Operation mode (Value set by the MD003 to MD001 bits) (see table above)	MD000	TCR counting operation
<ul style="list-style-type: none"> Interval timer mode (0, 0, 0) Capture mode (0, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
<ul style="list-style-type: none"> Event counter mode (0, 1, 1) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
<ul style="list-style-type: none"> One-count mode (1, 0, 0) 	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
<ul style="list-style-type: none"> Capture & one-count mode (1, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the PWM output pulse cycle time

- Timer data register 00 (TDR00)
Configure the PWM output pulse cycle time.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

$$\text{Pulse cycle time} = (\text{TDR00 setting} + 1) \times \text{Count clock cycle time}$$

$$2 \text{ [ms]} = (1/24\text{[MHz]}) \times (\text{TDR00 setting} + 1)$$

⇒ TDR00 setting = 47999

Setting up the channel 1 operation mode

- Timer mode register 01 (TMR01)
Select an operation clock (f_{MCK}).
Select a count clock.
Select the 16/8-bit timer.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Bits 15 and 14

CKS011	CKS010	Channel 1 operation clock (f_{MCK}) selection
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS01	Selection of count clock (f_{CLK}) of channel 1
0	Operation clock (f_{MCK}) specified with the CKS010 and CKS011 bits
1	Valid edge of the input signal from the TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Bits 10 to 8

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI01 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Others than above			Setting prohibited

Bits 7 and 6

CIS011	CIS010	Selection of TI01 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Bits 3 to 0

MD013	MD012	MD011	MD010	Operation mode of channel 1	Related function	TCR counting operation
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD010 bit operation varies depending on the operation mode (see the table below)

Operation mode (Value set by the MD013 to MD011 bits) (see table above)	MD010	TCR counting operation
<ul style="list-style-type: none"> Interval timer mode (0, 0, 0) Capture mode (0, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
<ul style="list-style-type: none"> Event counter mode (0, 1, 1) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
<ul style="list-style-type: none"> One-count mode (1, 0, 0) 	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
<ul style="list-style-type: none"> Capture & one-count mode (1, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the PWM output duty ratio

- Timer data register 01 (TDR01)
Configure the PWM output duty ratio.

Symbol: TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

$$\text{Duty ratio} = (\text{TDR01 setting}) / (\text{TDR00 setting} + 1) \times 100$$

$$10 [\%] = (\text{TDR01 setting}) / (63999 + 1) \times 100$$

⇒ TDR01 setting = 6400

Setting up the timer output mode

- Timer output mode register 0 (TOM0)
Set up the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOM07	TOM06	TOM05	TOM04	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	x	x	x	x	x	x	1	0

Bit 1

TOM01	Channel 1 timer output mode control
0	Master channel output mode. (Output is toggled with the timer interrupt request signal (INTTM01).)
1	Slave channel output mode. (Output is set with the master channel's timer interrupt request signal (INTTM01) and reset with the slave channel's timer interrupt request signal (INTTM0p).)

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)
Configure the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOL07	TOL06	TOL05	TOL04	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	x	x	x	x	x	x	0	0

Bit 1

TOL01	Channel 1 timer output level control
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	0	x

Bit 1

TO01	Channel 1 timer output
0	Timer output value is 0
1	Timer output value is 1

Enabling the timer output

- Timer output enable register 0 (TOE0)

Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	1	0

Bit 1

TOE01	Timer output enable/disable of channel 1
0	The TO01 operation stopped by count operation (timer channel output bit). Writing to the TO01 bit is enabled. The TO01 pin functions as data output, and it outputs the level set to the TO01 bit. The output level of the TO01 pin can be manipulated by software.
1	The TO01 operation enabled by count operation (timer channel output bit). Writing to the TO01 bit is disabled (writing is ignored). The TO01 pin functions as timer output, and the TOE01 bit is set or reset depending on the timer operation. The TO01 pin outputs the square-wave or PWM depending on the timer operation.

Bit 0

TOE00	Timer output enable/disable of channel 0
0	The TO00 operation stopped by count operation (timer channel output bit). Writing to the TO00 bit is enabled. The TO00 pin functions as data output, and it outputs the level set to the TO00 bit. The output level of the TO00 pin can be manipulated by software.
1	The TO00 operation enabled by count operation (timer channel output bit). Writing to the TO00 bit is disabled (writing is ignored). The TO00 pin functions as timer output, and the TOE00 bit is set or reset depending on the timer operation. The TO00 pin outputs the square-wave or PWM depending on the timer operation.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the PWM output pin

- Port mode register (P1)
Select the PM14 output latch.
- Port mode register (PM1)
Select the PM14 I/O mode.

Symbol: P1

7	6	5	4	3	2	1	0
P17 ^{Note 1}	P16 ^{Note 1}	P15 ^{Note 1}	P14 ^{Note 2}	P13	P12	P11	P10
x	x	x	0	x	x	x	x

Bit 4

P14 ^{Note 2}	P14 I/O mode selection ^{Note 2}
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Symbol: PM1

7	6	5	4	3	2	1	0
PM17 ^{Note 1}	PM16 ^{Note 1}	PM15 ^{Note 1}	PM14 ^{Note 2}	PM13	PM12	PM11	PM10
x	x	x	0	x	x	x	x

Bit 4

PM14 ^{Note 2}	PM14 I/O mode selection ^{Note 2}
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Notes: 1. Only for 30-pin products.

2. For 20- and 24-pin products. PM and PM16 for 30-pin products.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the timer count end interrupts

- Interrupt request flag register (IF0H)
Clear the interrupt request flag.
- Interrupt mask flag register (MK0H)
Mask interrupts.

Symbol: IF0H

7	6	5	4	3	2	1	0
TMIF01	TMIF00	IICAI0	TMIF03H	TMIF01H	SREIF0	SRIF0 CSIF01 IICIF01	STIF0 CSIF00 IICIF00
x	0	x	x	x	x	x	x

Bit 6

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
TMMK01	TMMK00	IICAMK0	TMMK03H	TMMK01H	SREMK0	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00
1	1	x	x	x	x	x	x

Bits 7 and 6

TMMK01 TMMK00	Interrupt processing control
0	Enables interrupt processing.
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.5 Main Processing

Figure 5.6 shows the flowchart for main processing.

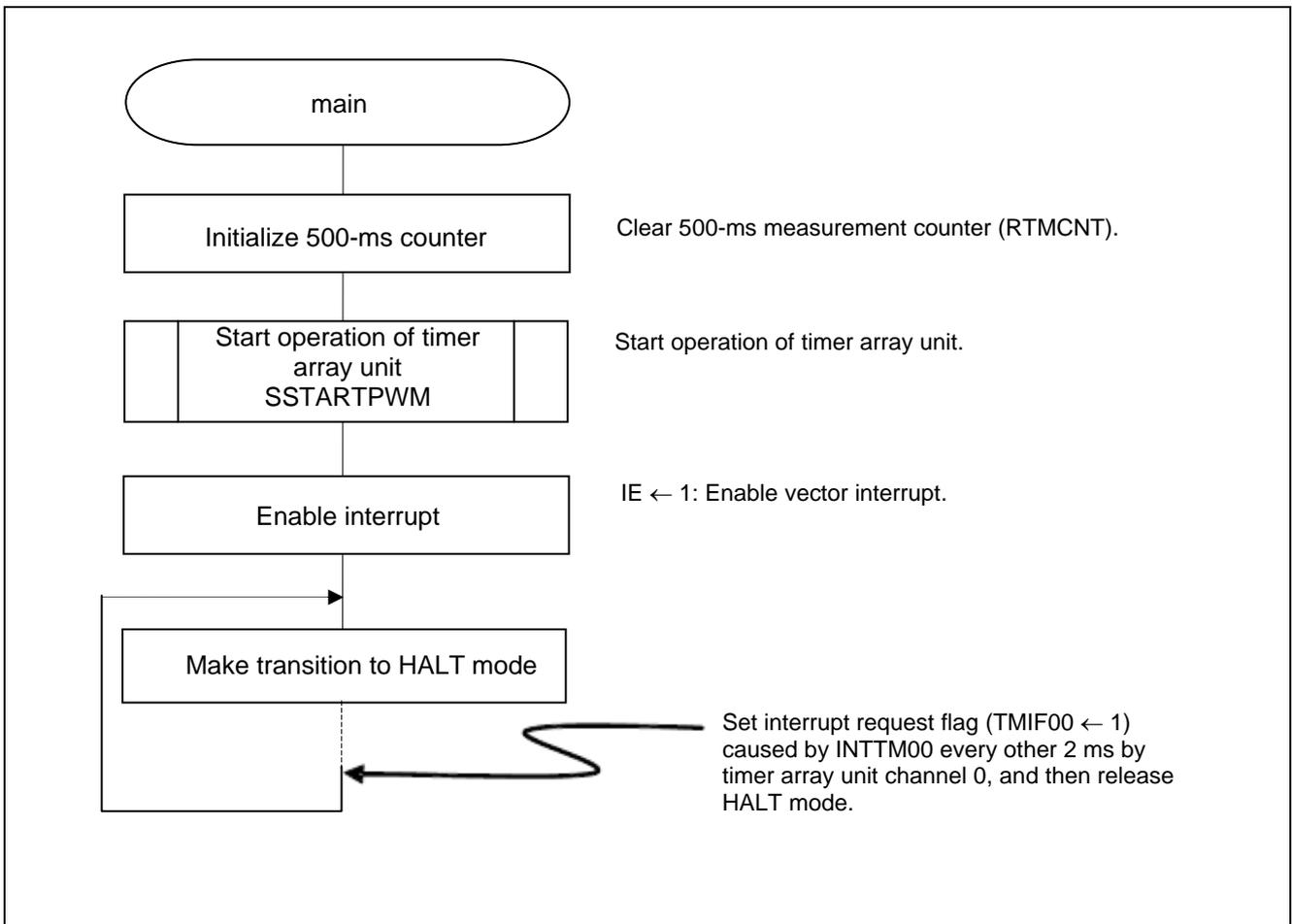


Figure 5.6 Main Processing

5.7.6 Timer Array Unit Startup

Figure 5.7 shows the flowchart for starting the operation of the timer array unit.

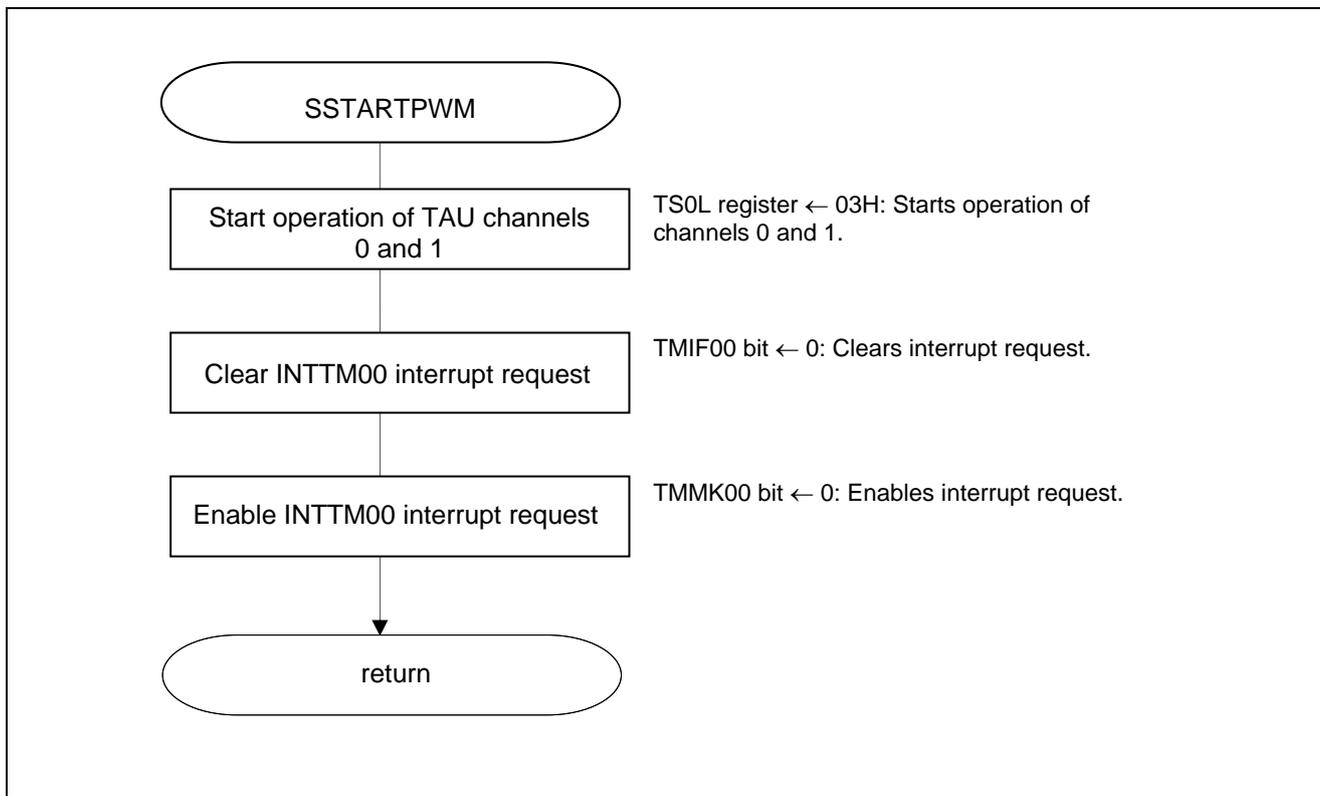


Figure 5.7 Timer Array Unit Startup

Configuring the timer startup

- Timer channel start register 0 (TS0/TSOL)
Enable count operation of channel 0 and channel 1.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH 03	0	TSH 01	0	TS0 7	TS0 6	TS0 5	TS0 4	TS0 3	TS0 2	TS0 1	TS0 0
0	0	0	0	x	0	x	0	x	x	x	x	x	x	1	1

Bit 1

TS01	Operation enable (start) trigger of channel 1
0	No trigger operation
1	The TE01 bit is set to 1 and the count operation becomes enabled. The TCR01 register count operation start in the count operation enabled state varies depending on each operation mode.

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled. The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the timer count end interrupts

- Interrupt request flag register (IF0H)
Clear the interrupt request flag.
- Interrupt mask flag register (MK0H)
Mask interrupts.

Symbol: IF0H

7	6	5	4	3	2	1	0
TMIF01	TMIF00	IICAIF0	TMIF03H	TMIF01H	SREIF0	SRIF0 CSIF01 IICIF01	STIF1 CSIF00 IICIF00
x	0	x	x	x	x	x	x

Bit 6

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
TMMK01	TMMK00	IICAMK0	TMMK03H	TMMK01H	SREMK0	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00
x	0	x	x	x	x	x	x

Bit 6

TMMK00	Interrupt processing control
0	Enables interrupt processing.
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.7 INTTM0 Interrupt Processing

Figure 5.8 shows the flowchart for INTTM0 interrupt processing.

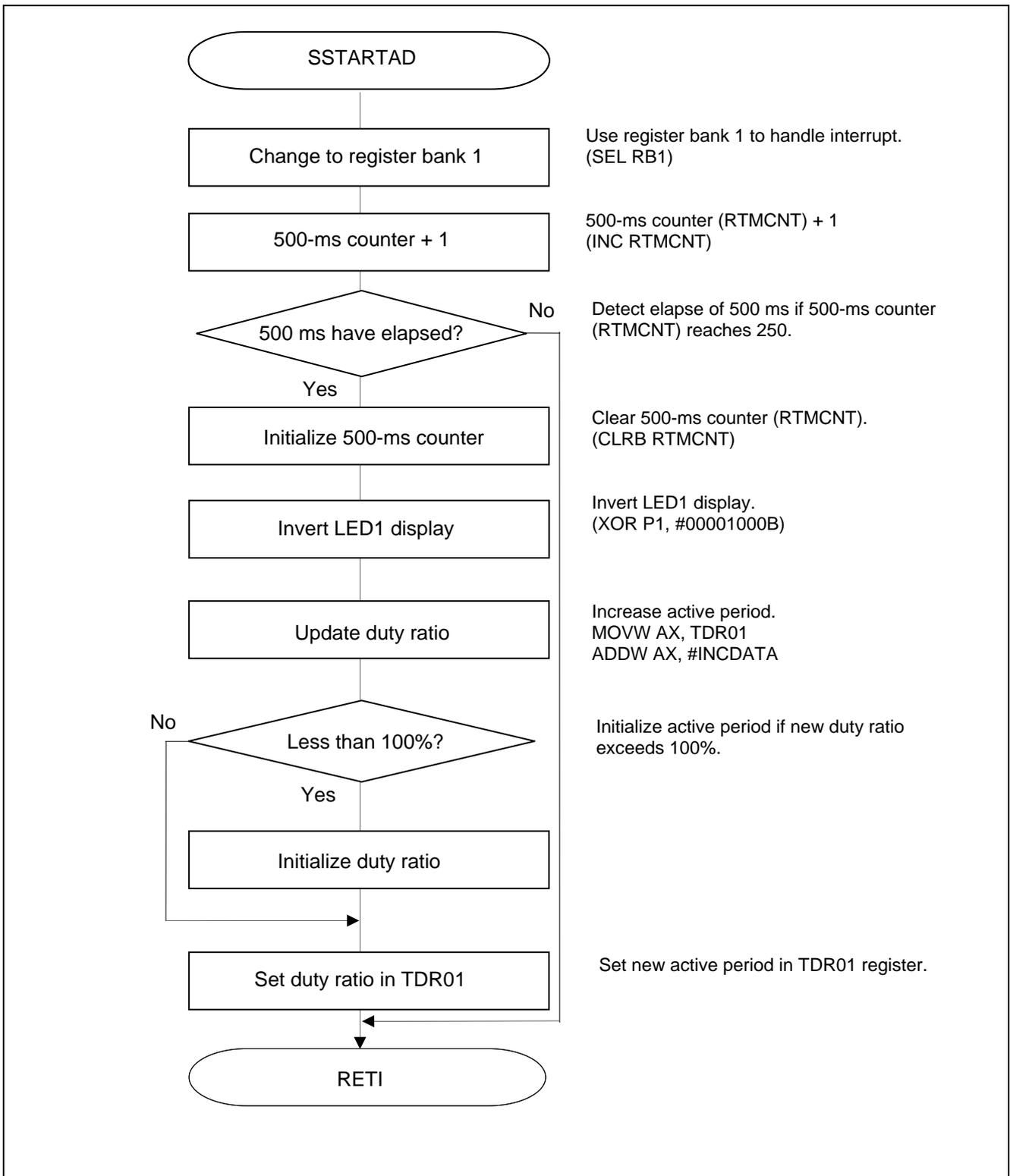


Figure 5.8 INTTM0 Interrupt Service Routine

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G12 User's Manual: Hardware (R01UH0200E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Renesas Electronics Website

- <http://www.renesas.com/index.jsp>

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- <http://www.renesas.com/contact/>

Revision Record	RL78/G12 Timer Array Unit (PWM Output)
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Rev.	Date	Description	
		Page	Summary
1.00	Mar.01, 2013	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
 - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
 - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
 - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
 - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
 - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852-2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

11F., Samik Laviel' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141