RL78/G10

Software-based Multiplexed PWM Output

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Introduction

This application note explains how to achieve multiplexed PWM output of varying duty ratios with software by employing a timer interrupt. Four PWM signals can be output per 1ms cycle, while the PWM output duty can be changed using the external switch controller.

Target Device

RL78/G10 (ROM 2KB, 10 pins） R5F10Y16ASP

When using this application note for other microcomputers, please modify it according to the corresponding specification and evaluate thoroughly before use.

Contents

1. Specifications

This application note explains how to achieve four 254-level PWM output pins with software-based port control using the upper 8 bits of timer array unit (TAU) channel 1 as the interval timer for generating 3.9µs datum timing. PWM duty phases are stored in advance to the flash memory, allowing the PWM duty to be changed via switch input. The term “duty data” indicates the data used to set the duty assigned to the flash memory.

Each PWM output period is approximately 1ms, consisting of 256 times (full count of 8-bit timer) based on 3.9µs datum timing.

Table 1.1 shows the Peripheral Functions and Usage, Figure 1.1 State Transition during Program Execution Figure 1.2 an outline of the Multiplexed PWM Output Operation Overview.

Table 1.1 Peripheral Functions and Usage

Peripheral Function	Usage
TAU channel 1	Upper 8 bits are used as an interval timer to generate the 3.9µs datum timing
Input output ports P0.0～P0.3	Used for PWM signal output
Input port P13.7	Used for PWM signal duty change trigger switch input

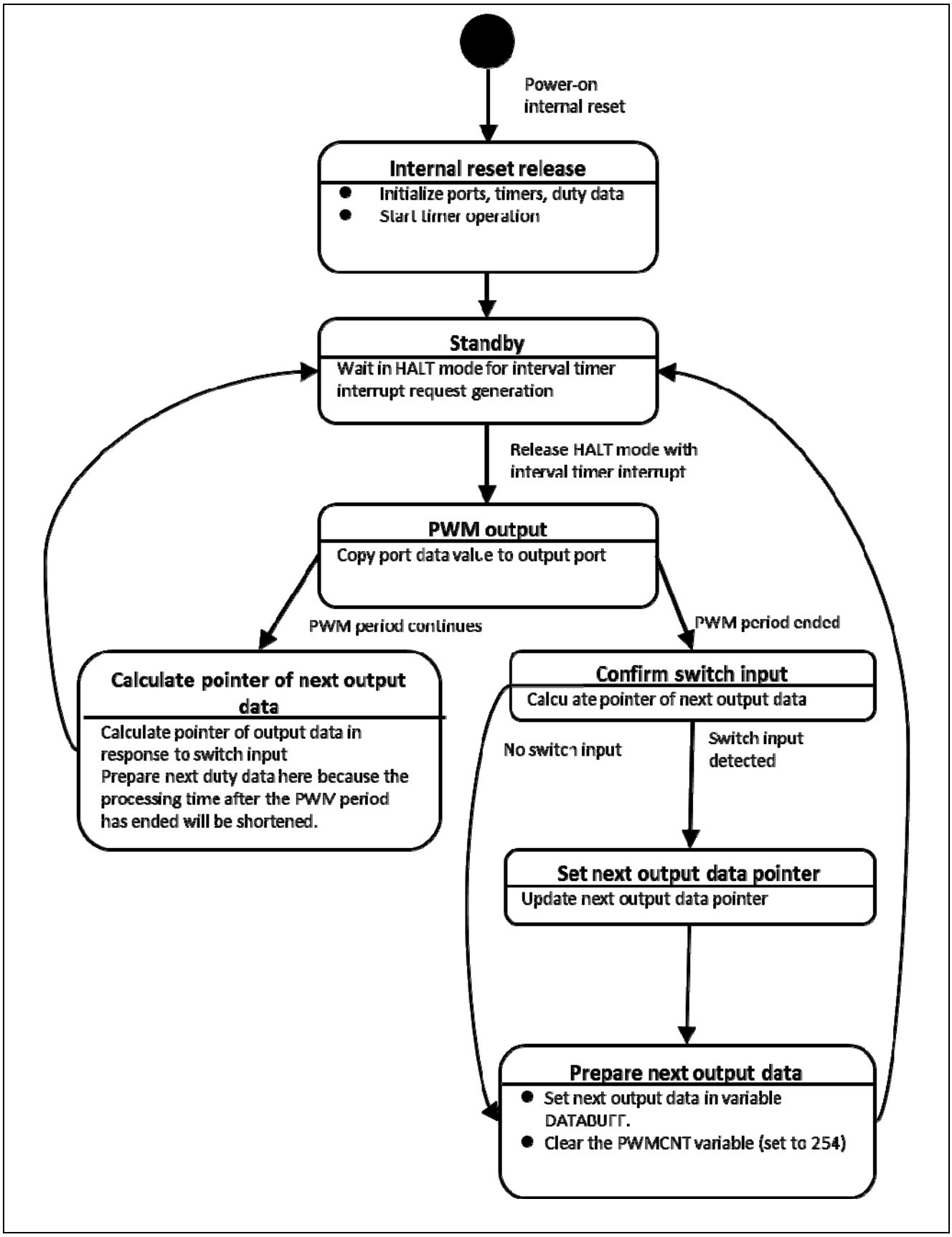

Figure 1.1 State Transition during Program Execution

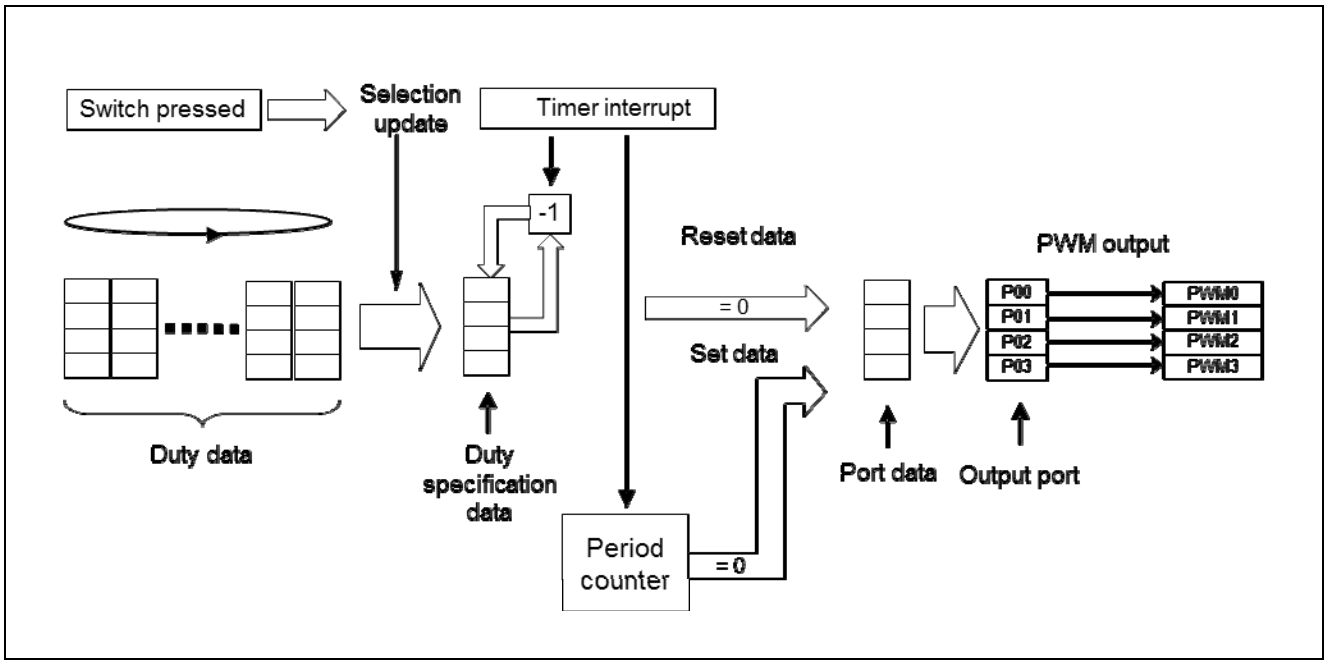

Figure 1.2 Multiplexed PWM Output Operation Overview

A set of data from the duty data is selected and copied to the duty specification data. This duty specification data is decreased by 1 for each fixed period (3.9µs period) timer interrupt. When the duty specification data becomes 0, the data is cleared and output to the port. In addition, period counted is started with the timer interrupt; when the period has ended, the duty specification data and the output data are both reset. All 4 signals are processed, enabling output of PWM signals for 4 separate duty ratios. The timer interrupt waits in HALT mode and processes the output to the ports first, allowing jitter to be mitigated by software.

When switch input occurs, the next set of data is selected from the duty data and the same operation is repeated, allowing the PWM signal duty to be changed. Figure 1.3 provides the Multiplexed PWM Output Timing Chart.

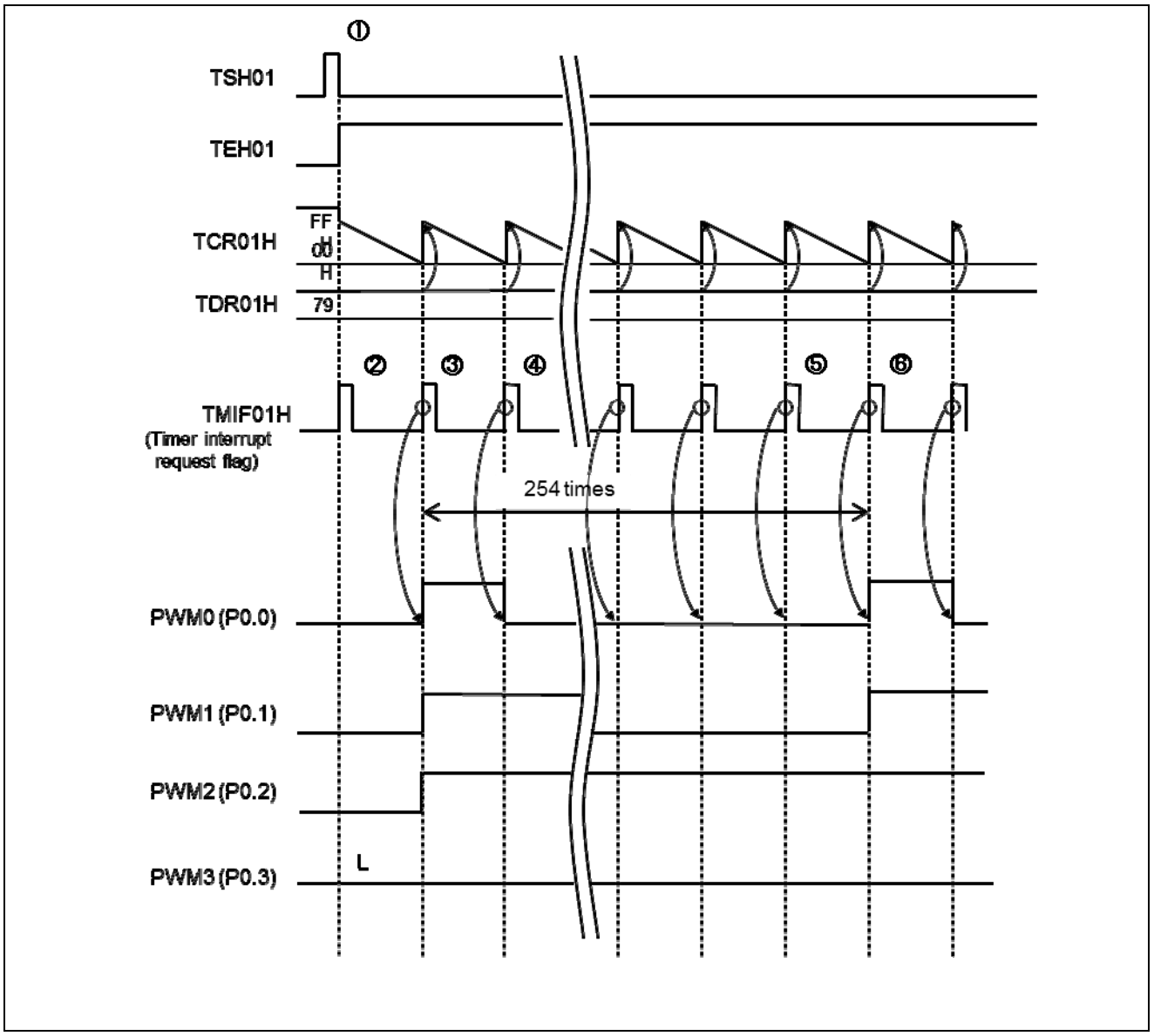

Figure 1.3 Multiplexed PWM Output Timing Chart

① Set the initial value of the output data and start the timer (TAU channel 1). When the specified duty ratio is 0%, set 0 as the initial value and all other values to 1. (Fig. 1.3 shows an example of PWM3 as 0%).

② Interrupts occurring immediately after the timer is started are ignored, even if TAU channel 1 interrupt (INTTM01H) is generated. The CPU waits for the timer interrupt request in HALT mode.

③ When the TAU channel 1 interrupt (INTTM01H) is generated, the previously set initial values are output to the port, and operation is started. At this time, the duty specification counters for each PWM signal start to count down. When a value goes to 0, the next output data for the corresponding output is cleared to 0 (corresponding to PWM0). The counter that specifies the PWM signal period also counts down.

④ The next time the TAU channel 1 interrupt (INTTM01H) occurs, the next set of prepared data is output to the port. At this point, PWM0 output is 0. Both the counter that specifies the duty for the corresponding PWM signal and the counter that specifies the PWM signal period count down at this point as well.

⑤ At the 254th valid INTTM01H interrupt, the counter that specifies the PWM signal period counts down to 0 and the next data returns to the initial value. When duty ratio is 100%, output has not yet 0, and the value remains at 1.

⑥ Steps 3 to 5 are repeated.

Notes As a work-around for the asynchronous issue related to program execution and receiving interrupts (the instruction execution state causes deviations in interrupt receive timing and port control timing, which leads to jitter affecting PWM output), this program is designed to wait for a fixed period interrupt from the interval timer in HALT mode. This ensures stable timing for receiving interrupt requests. To shorten the interrupt processing time as much as possible (8 clocks are required just for the RETI instruction), the vector interrupt is not used and only HALT mode is released.

In addition, the next PWM output data is prepared (output data calculation/internal variable setting/port data preparation, etc.) within one PWM output period to improve programming efficiency. These enhancements enable jitter-mitigated PWM output in the 3.9µs datum timing.

The duty data can be changed by rewriting the contents of datatable.asm, using Figure 5.1 Duty Data Configuration as a datum.

2. Operating Conditions

The sample code described in this application note runs under the following operating conditions.

Table 2.1 Operating Conditions

Item	Description/Specification
MCU used	RL78/G10 (ROM 2KB, 10 pins) R5F10Y16ASP
Operating frequency	● High-speed on-chip oscillator clock (HOCO): 20MHz ● CPU/peripheral hardware clock: 20MHz
Operating voltage	5.0V (valid operations: 2.9V to 5.5V) SPOR operating voltage (TYP): rising power supply 2.90V, falling power supply 2.84V
Integrated development environment	CS+ for CA,CX V3.00.01 (manufactured by Renesas Electronics)
Assembler	CA78K0R Ver1.71 (manufactured by Renesas Electronics)
Evaluation board	RL78/G10 target board (QB-R5F10Y16-TB)

3. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

RL78/G10 Initialization (R01AN1454E) Application Note

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows the example hardware configuration described in this application note.

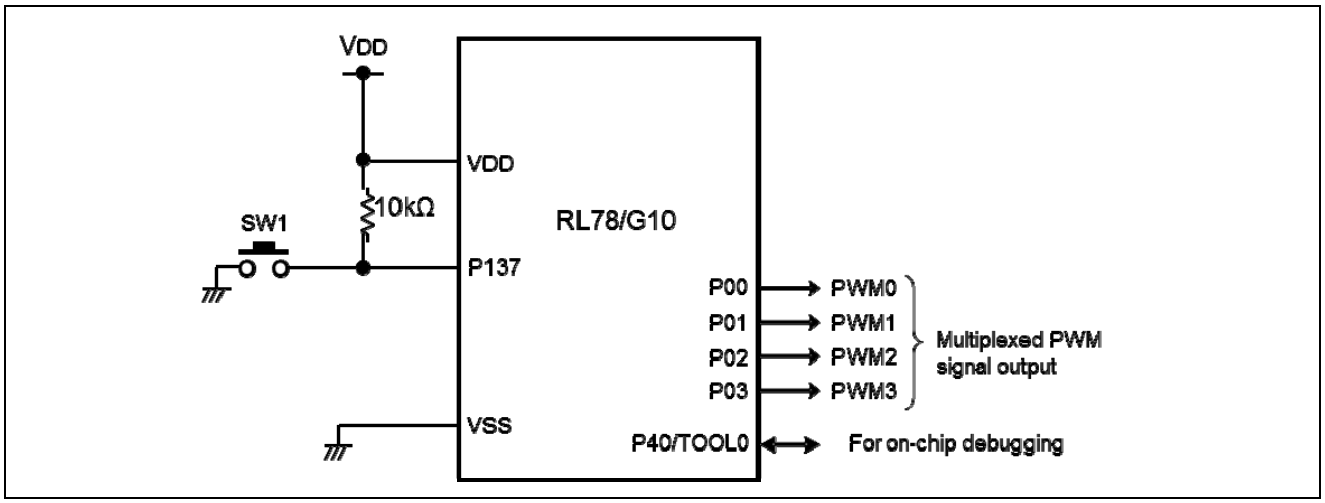

Figure 4.1 Hardware Configuration

Note: 1.This simplified circuit diagram was created to show an overview of connections only.
When designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)
2. Make V_{DD} higher than the RESET release voltage (V_{SPOR}) set in SPOR.

4.2 Pin List

Table 4.1 provides a List of Pins and Functions explained in this document.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P00 to P03	Output	PWM output
P137	Input	Switch (SW1) input

5. Software Explanation

5.1 Operation Outline

The application described in this document generates a 3.9µs interrupt (datum timing) that serves as a base for PWM signals by dividing TAU channel 1 in to two 8-bit timers and using the upper 8 bits as the interval timer.

Jitter is mitigated to a minimum during interrupt processing by making sure prepared data is output at the start of the processing. The PWM output data to be set in the next interrupt is prepared within one PWM output period. When one period has ended, the data for the next period data (initial value) is set. If the external switch (SW1) is pressed at this time, the next period continues with the current PWM output setting and the PWM output is updated with the prepared data in the subsequent period.

(1) TAU is initialized as follows:

<Settings>

- Pins P00 to P03: set to PWM signal output ports
- TAU channel 1 upper 8 bits: set to 3.9µs [Note1] period interval timer mode
- Use TAU channel 1 timer interrupt (INTTM01H)

(2) Interval timer operation is started by setting the TAU channel 1 operation enabled trigger bit to “1” after setting the required variables for multiplexed PWM output. The HALT mode is instruct (disables the vector interrupt) and waits for the TAU channel 1 timer interrupt (INTTM01H).

(3) After timer operation has started, the TAU channel 1 timer interrupt (INTTM01H) is generated every 3.9µs, HALT mode is released, and the multiplexed PWM output operation starts.

(4) The multiplexed PWM output operation first reflects the port data value in the output port, then checks the PWM output period. If a full period of PWM output has not ended, the next port data value for PWM output is calculated. If PWM output has completed one period, external switch input is checked. If switch input is detected, duty data is updated and the next port data is prepared. After this entire process is completed, the operation transitions to the standby state (HALT mode) and waits for an interval timer interrupt.

Note 1. Defined as a fixed interval in the header file (DEV&TIMER.inc).

Note 2. Defined in the data table file (datatable.asm).

5.2 Option Byte Settings

Table 5.1 shows the option byte settings.

Table 5.1 Option Byte Settings

Address	Setting Value	Description
000C0H	11101110B	Watchdog timer operation stops (counting stopped after reset)
000C1H	11110111B	SPOR detection voltage When power supply falls: TYP. 2.84V When power supply rises: TYP. 2.90V P125/KR1/RESET pin control: RESET input
000C2H	11111001B	HOCO: 20MHz
000C3H	10000101B	Enables on-chip debug operation

5.3 Constants

Table 5.2 lists the Sample Code Constants. Figure 5.1 shows the Duty Data Configuration

Table 5.2 Sample Code Constants

Constant Name	Setting Value	Description
CLKFREQ	20000	Clock frequency expressed in kHz
PERIOD	1000	PWM signal period express in µs (micro seconds)
COUNT	CLKFREQ × PERIOD/1000	PWM signal period expressed as clock frequency
INTERVAL	COUNT/254	Interval timer count
PWMP	P0	PWM signal output port
PWM0DATA	00000000B	Initial value of PWM signal
PWMPM	PM0	PWM signal port mode
PWMDATA	Voluntary (defined in DB in 4-byte)	Assigned address of PWM signal data duty (value must be an even number)
DATAEND	—	Last assigned address of PWM signal data duty
SCALE	254	PWM output signal levels
DF00 to DF100	00H, (SCALE x 5 + 50)/100 to (SCALE x 95 + 50)/100, SCALE	Data indicating the length of high period corresponding to the PWM signal duty expressed in 5% increments[Note 1]

Note 1 Used when setting the PWM signal duty data in datatable.asm, representing the high period in 5% increments for consecutive 2-digit/3-digit numbers in DF addresses.

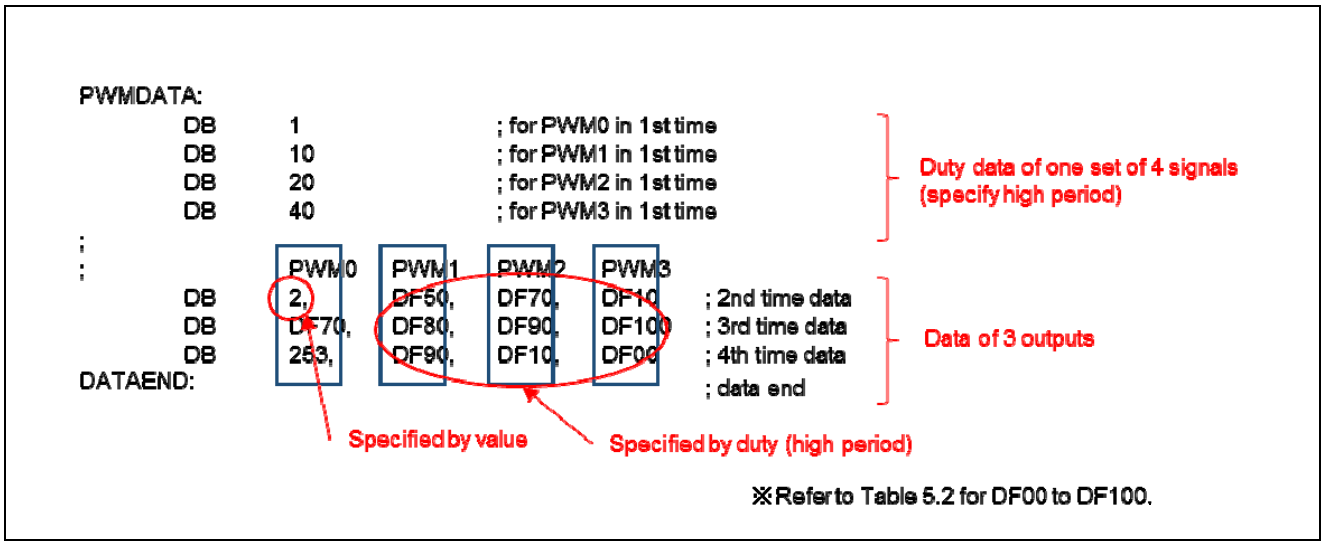

Figure 5.1 Duty Data Configuration

Duty data is treated independently as datatable.asm. To changed the PWM signal duty dynamically, prepare the appropriate data based on the configuration in Figure 5.1

Data is assigned from address 200H and can be set to within the range of the flash memory.

5.4 Variables

Table 5.3 lists the variables used in the sample code.

Table 5.3 Sample Code Variables

Function Name	Description
SWSTATUS (16 bits)	Used to confirm switch status and prevent chattering
NEXTPOINTER (16 bits)	Stores pointer for the next PWM duty (high period) data
PWMCNTBUF0 (16 bits)	Duty data for PWM0 and PWM1 signals
PWMCNTBUF1 (16 bits)	Duty data for PWM2 and PWM3
PWMCNT	Variable for PWM signal cycle count
DATABUFF	Stores data for the next PWM signal to be output

5.5 Functions (subroutines)

Table 5.4 lists the Functions (subroutines) used in the sample code.

Table 5.4 Functions (subroutines)

Function Name	Description
RESET_START	Overall flow
SINIPORT	Initializes input/output ports
SINICLK	Sets clock generation circuit
SINITAU	Processes TAU operation mode settings
SINIINTP0	Initializes INTP0
SSTARTINTV	Starts interval timer operation for TAU channel 1
COPYPWMDATA	Copies data to the PWM duty data work area
GETNEXT	Processing to prepares initial value data for PWM duty
IINTTM01H	TAU channel 1 timer interrupt processing section in main processing

5.6 Function (subroutine) Specifications

The following are the specifications of functions (subroutines) used in the sample code.

Function Name: RESET_START

Outline	Overall flow
Description	Initializes stack pointer, port function CPU clock and TAU, then calls main function.
Argument	None
Return Value	None
Notes	None

Function Name: SINIPORT

Outline	P0 initialization
Description	Sets P01/ANI0 to P03/ANI2 pins to digital output, sets P00 to P03 to Low.
Argument	None
Return Value	None
Notes	None

Function Name: SINICLK

Outline	CPU and peripheral hardware clock settings
Description	Sets CPU and peripheral hardware clock frequency to 20MHz.
Argument	None
Return Value	None
Notes	None

Function Name: SINITAU

Outline	TAU operation mode setting processing
Description	Sets TAU channel 1 to two 8-bit timers, sets upper channels to 3.9μs interval timer, and masks interrupt requests.
Argument	None
Return Value	None
Notes	None

Function Name: SINIINTP0

Outline	INTP0 initialization
Description	Disables INTP0 interrupt.
Argument	None
Return Value	None
Notes	None

Function Name: SSTARTINTV

Outline	TAU channel 1 interval timer operation start processing
Description	Starts TAU channel 1 count operation, clears interrupt request (TMIF01H), and releases interrupt mask (TMMK01H).
Argument	None
Return Value	None
Notes	None

Function Name: COPYPWMDATA

Outline	PWM duty data operation area copy processing
Description	Copies duty setting data of 4 PWM signals from flash memory to variable area.
Argument	None
Return Value	None
Notes	Six clocks are required for each read operation from the flash memory. The peak processing time can be shortened by copying data to the RAM, which can be accessed by 2 clocks.

Function Name: GETNEXT

Outline	PWM duty initialization data preparation processing
Description	Prepares PWM signal data (initial value) from the variable area duty setting data to be output in the next TAU channel 1 interrupt (INTTM01H).
Argument	None
Return Value	None
Notes	None

Function Name: IINTTM01H (part of main processing)

Outline	TAU channel 1 timer interrupt processing
Description	HALT mode is released with the TAU channel 1 interrupt (INTTM01H) request, and the prepared data is output to P0. If the full PWM signal period has not ended, this function also prepares the next data. If the PWM signal period has ended, the function prepares the next period data (initial value).If the switch is pressed at this time, the pointer that reads duty data from the flash memory is updated. Note that this data will be reflected two periods later.
Argument	None
Return Value	None
Notes	The period for the interrupt processing cannot be shortened to less than 3.9µs when outputting 4 PWM signals because the number of clocks is limited

5.7 Flowcharts

The sample code is described in assembly language. Therefore, RET is used as the termination symbol to indicates the return from the function (subroutine).

Figure 5.2 shows the Overall Flow of the sample code described in this application note.

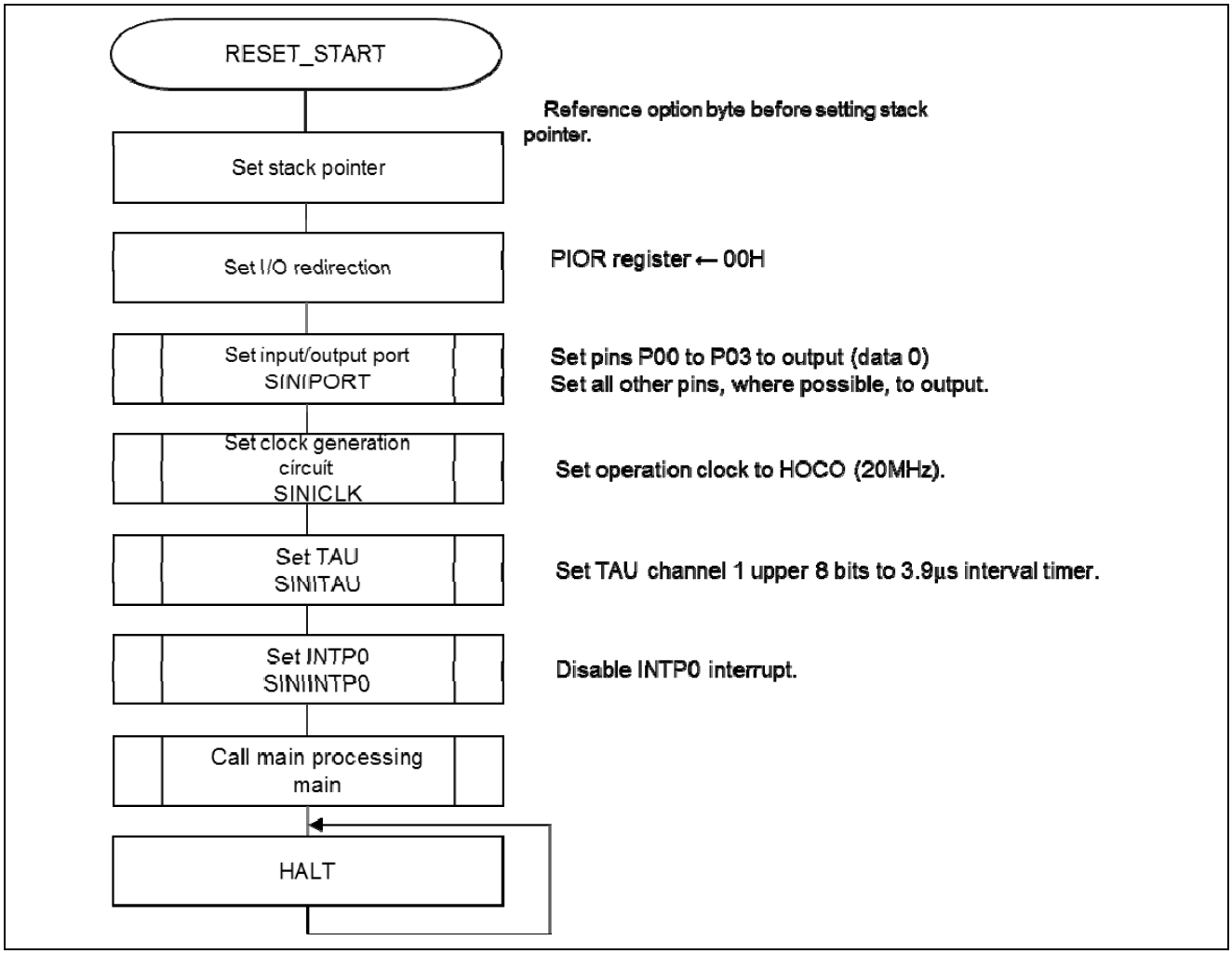

Figure 5.2 Overall Flow

5.7.1 I/O Port Settings

Figure 5.3 shows the flowchart for I/O Port Settingss.

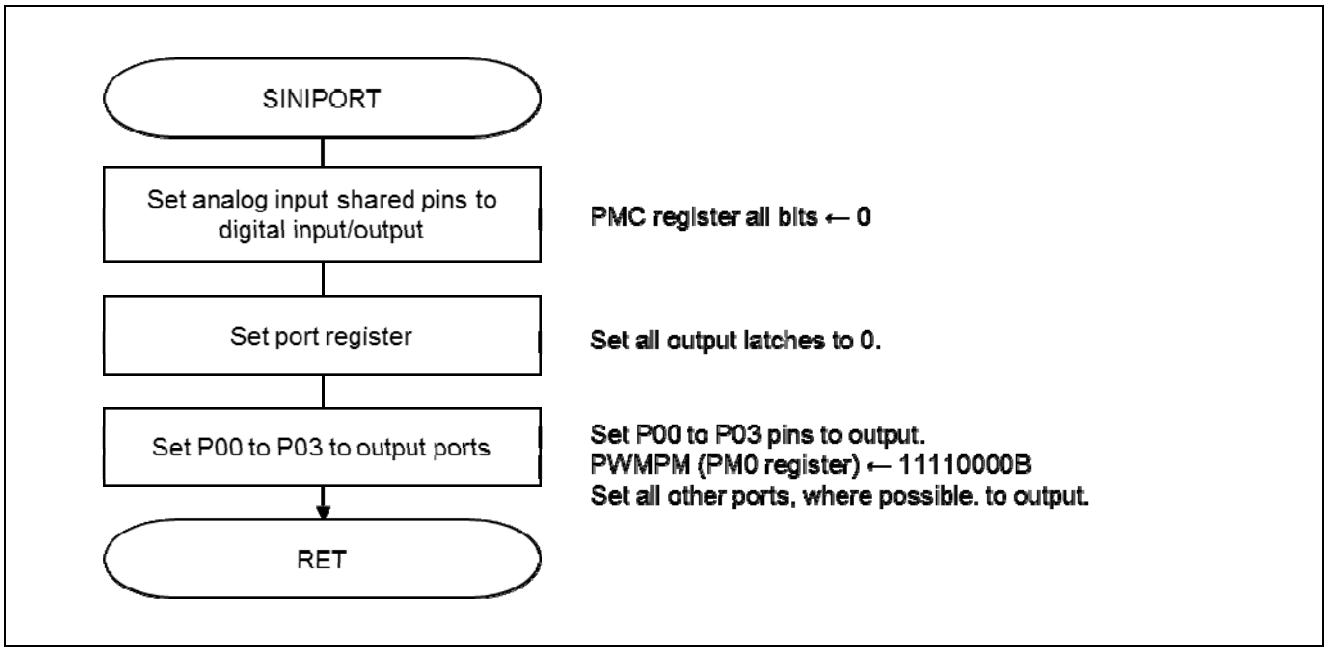

Figure 5.3 I/O Port Settings

Note: For more details concerning unused port settings, please refer to refer to the flowchart in RL78/G10 Initialization (R01AN2668E) Application Note.

Note: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

PWM signal output pin setting

・Port mode register (PM0)
Select P0 input/output mode.

Symbol: PM0

7	6	5	4	3	2	1	0
PM07[Note]	PM06[Note]	PM05[Note]	PM04	PM03	PM02	PM01	PM00
0[Note]/1	0[Note]/1	0[Note]/1	0	**0**	**0**	**0**	**0**

Note 16-pin products only

Bits 3 - 0

PM0n	Selection of PM0n input output mode
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

5.7.2 Clock Generation Circuit Setting

Figure 5.4 shows the flowchart for the .

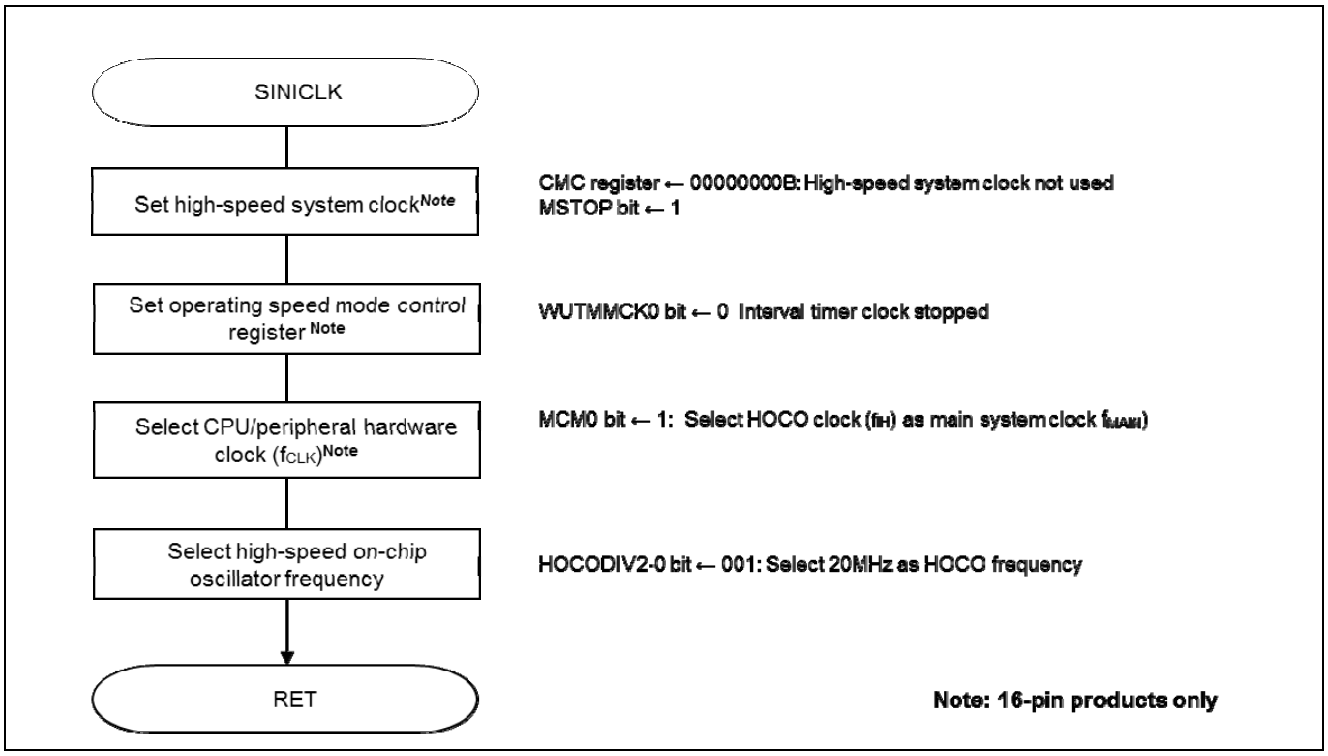

Figure 5.4 Clock Generation Circuit Settings

Note: For more details concerning CPU clock generation settings (SINICLK), refer to the flowchart in RL78/G10 Initialization (R01AN2668E) Application Note.

5.7.3 Timer Array Unit Setting

Figure 5.5 shows the flowchart for the .

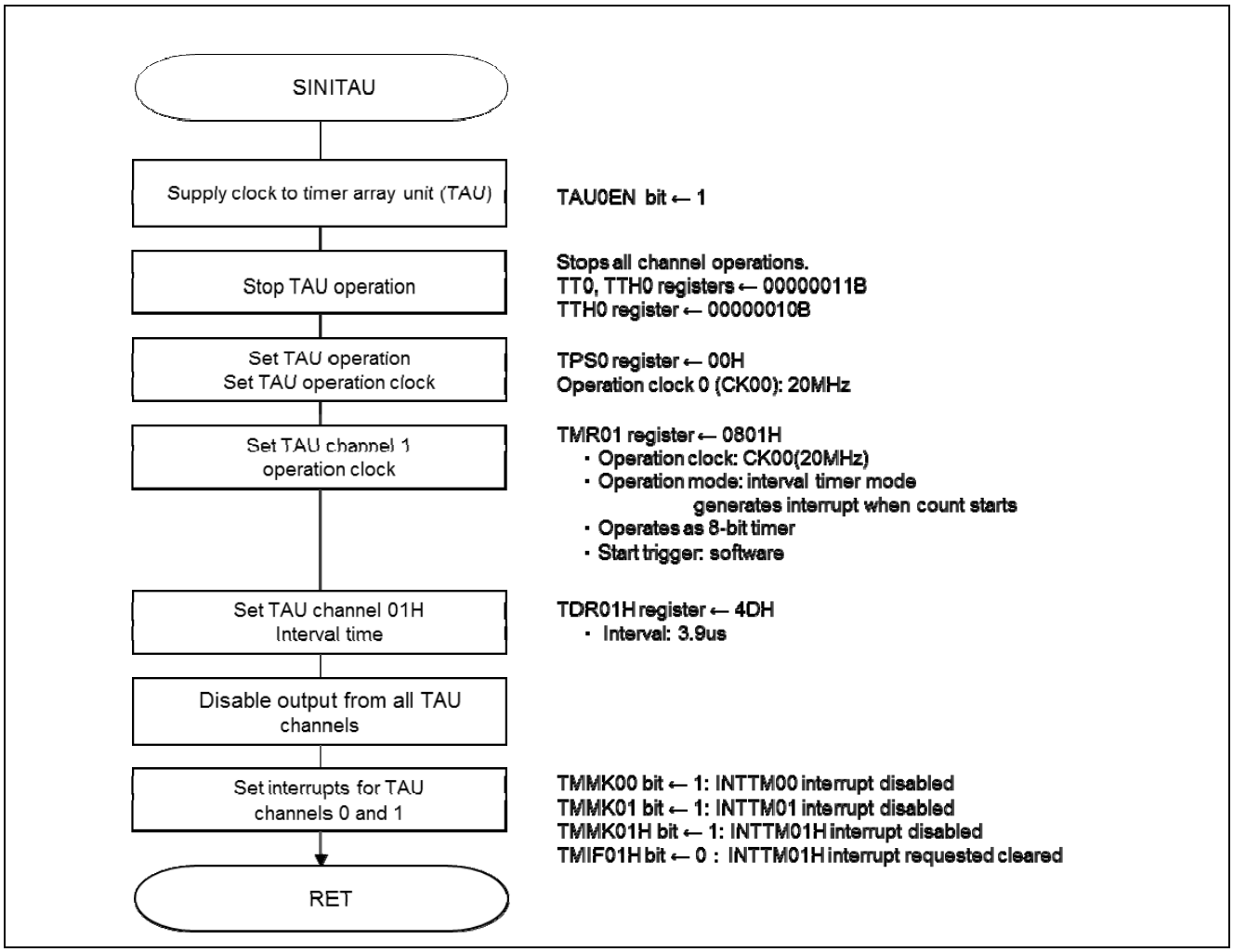

Figure 5.5 Timer Array Unit Setting

Start clock supply to timer array unit 0

・Peripheral enable register 0 (PER0)

Set clock supply start/stop to timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN	CMPEN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
x	0	x	x	0	x	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Timer operation stop

・Timer channel stop register 0 (TT0, TTH0)
Set the timer channel to stop.

Symbol: TT0

7	6	5	4	3	2	1	0
0	0	0	0	TT03 注	TT02 注	TT01	TT00
0	0	0	0	**1** 注	**1** 注	**1**	**1**

7	6	5	4	3	2	1	0
0	0	0	0	TT03H 注	0	TT01H	0
0	0	0	0	**1** 注	0	**1**	0

Note: 16-pin products only

Bit n

TT0n	Operation stop trigger of channel n (n = 1, 3)
0	No trigger operation
1	Clears the TE0n bit to 0 and stops the count operation (stop trigger generator)

Timer clock frequency setting

・Timer clock select register 0 (TPS0)
Select operation clock for timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	**f_{CLK}= 20MHz**
0	**0**	**0**	**0**	**f_{CLK}**	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	312.5 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156.2 kHz	312.5 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78.1 kHz	156.2 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39.1 kHz	78.1 kHz	156.2 kHz	312.5 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39.1 kHz	78.1 kHz	156.2 kHz	312.5 kHz
0	1	1	1	$f_{CLK}/2^7$	9.76 kHz	19.5 kHz	39.1 kHz	78.1 kHz	156.2 kHz
1	0	0	0	$f_{CLK}/2^8$	4.88 kHz	9.76 kHz	19.5 kHz	39.1 kHz	78.1 kHz
1	0	0	1	$f_{CLK}/2^9$	2.44 kHz	4.88 kHz	9.76 kHz	19.5 kHz	39.1 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.44 kHz	4.88 kHz	9.76 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	610 Hz	1.22 kHz	2.44 kHz	4.88 kHz	9.76 kHz
1	1	0	0	$f_{CLK}/2^{12}$	305 Hz	610 Hz	1.22 kHz	2.44 kHz	4.88 kHz
1	1	0	1	$f_{CLK}/2^{13}$	153 Hz	305 Hz	610 Hz	1.22 kHz	2.44 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	153 Hz	305 Hz	610 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	153 Hz	305 Hz	610 Hz

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

Channel 1 operation mode setting

・Timer mode register 01 (TMR01H, TMR01L)

Select operation clock ($f_{MCK.}$).
Select count clock.
Set start trigger and capture trigger.
Select timer input valid edge.
Set operation mode.

Symbol: TMR01H

7	6	5	4	3	2	1	0
CKS011	0	0	CCS01	SPLIT01	STS012	STS011	STS010
0	0	0	**0**	**1**	**0**	**0**	**0**

Bit 7

CKS011	Selection of channel 1 operation clock (f_{MCK})
0	Operation clock CK00 set by timer clock select register 0 (**TPS0)**
1	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS01	Selection of channel 1 count clock (f_{TCLK})
0	**Operation clock (f_{MCK}) specified by the CKS011 bit**
1	Valid edge of the input signal from the TI00 pin

Bit 3

SPLIT01	Selection of channel 13 8-bit/16-bit timer operation
0	Operates as 16-bit timer
1	**Operates as 8-bit timer**

Bits 2 - 0

STS012	STS011	STS010	Setting of channel 1 start trigger/capture trigger
0	**0**	**0**	**Only software trigger start valid (other trigger sources are invalid)**
0	0	1	Use TI00 pin input valid edge as both start trigger and capture trigger
0	1	0	Use both edges of TI00 pin input as triggers, one each for start/capture
1	0	0	Use master channel interrupt signal (when using multiple channel concurrent operational functions of slave channel)
Other than the above			Setting prohibited

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Symbol: TMR01L

7	6	5	4	3	2	1	0
CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**0**	0	0	**0**	**0**	**0**	**1**

Bits 7 - 6

CIS011	CIS0100	Selection of TI01 pin valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: falling edge; Capture trigger: rising edge
1	1	Both edges (when high-level width is measured) Start trigger: rising edge; Capture trigger: falling edge

Bits 3 - 0

MD013	MD012	MD011	MD010	Setting of operation mode of channel 1	Corresponding function	Count operation of TCR
0	**0**	**0**	**1** /0	**Interval timer mode**	**Interval timer/square wave output divider function/PWM output (master)**	**Down count**
0	1	0	1/0	Capture mode	Input pulse width measurement	Up count
0	1	1	0	Event counter mode	External event counter	Down count
1	0	0	1/0	One-count mode	Delay counter/one-shot pulse output/PWM output (slave)	Down count
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width input signal	Up count
Other than the above				Setting prohibited		

PWM output pulse period setting

・Timer data register 01H (TDR01H)
Set interval timer period.

Symbol: TDR01H

TDR01H

7	6	5	4	3	2	1	0

Pulse period = (TDR01H setting value + 1) x count clock period
4[μs] = (1 / 20[MHz]) x (TDR00 setting value + 1)

→**TDR01** setting value = **77**

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer output disable setting

・Timer output enable register 0 (TOE0)

Set each channel timer to output enabled/disabled.

Symbol: TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03 注	TOE02 注	TOE01	TOE00
0	0	0	0	x	x	**0**	**0**

Note 16-pin products only

Bit 1

TOE01	Channel 1 timer output enable/disable
0	**TO01 (timer channel output bit) operation is disabled by the count operation.** **Write operation to T01 bit is enabled.** **TO01 pin operates as data output function, the level set in TO01 bit is output from TO01 pin.** **TO01 pin output level can be controlled by software.**
1	TO01 (timer channel output bit) operation is enabled by count operation. Write operation to TO01 bit is disabled (write operation is ignored). TO01 pin operates as timer output function, timer operation executes set/reset. TO01 pin square wave output or PWM output is output from TO01 pin based on timer operation.

Bit 0

TOE00	Channel 0 timer output enable/disable
0	**TO00 (timer channel output bit) operation is disabled by the count operation.** **Write operation to T00 bit is enabled.** **TO00 pin operates as data output function, the level set in TO00 bit is output from TO00 pin.** **TO00 pin output level can be controlled by software.**
1	TO00 (timer channel output bit) operation is enabled by count operation. Write operation to TO00 bit is disabled (write operation is ignored). TO00 pin operates as timer output function, timer operation executes set/reset. TO00 pin square wave output or PWM output is output from TO00 pin based on timer operation.

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer count complete interrupt setting

- Interrupt request flag register (IF0L)
  Clear interrupt request flag register.
- Interrupt mask flag register (MK0L, MK0H)
  Set interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	**0**	x	x	x	x	x	x

Bit 6

TMIF01H	Interrupt request flag
0	Interrupt request signal is not generated
1	Interrupt request signal is generated, goes to interrupt request state

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
1	**1**	x	x	x	x	x	x

Bit 7

TMMK00	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Bit 6

TMMK01H	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	x	**1**

Bit 0

TMMK01	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

5.7.4 External Interrupt Processing

Figure 5.6 shows the flowchart for .

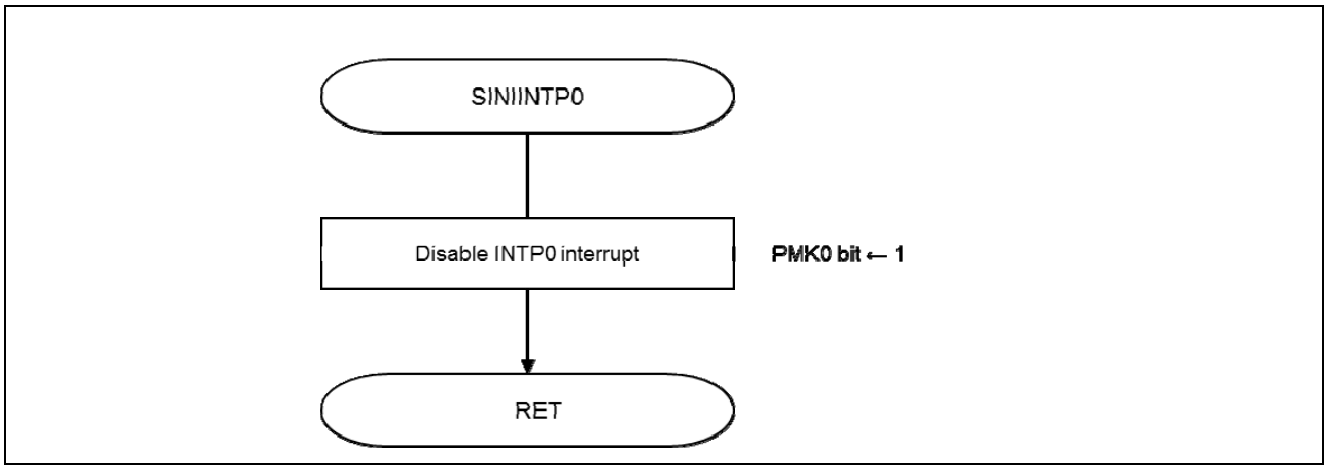

Figure 5.6 External Interrupt Processing

・Interrupt mask flag register (MK0L)

Set interrupt mask.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	x	x	x	x	**0/1**	x

Bit 1

PMK0	Interrupt processing control
0	Interrupt processing enabled
1	**Interrupt processing disabled**

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

5.7.5 Main Processing

Figure 5.7 to Figure 5.9 show flowcharts for the main processing.

Symbols A through D connect to figures on subsequent pages.

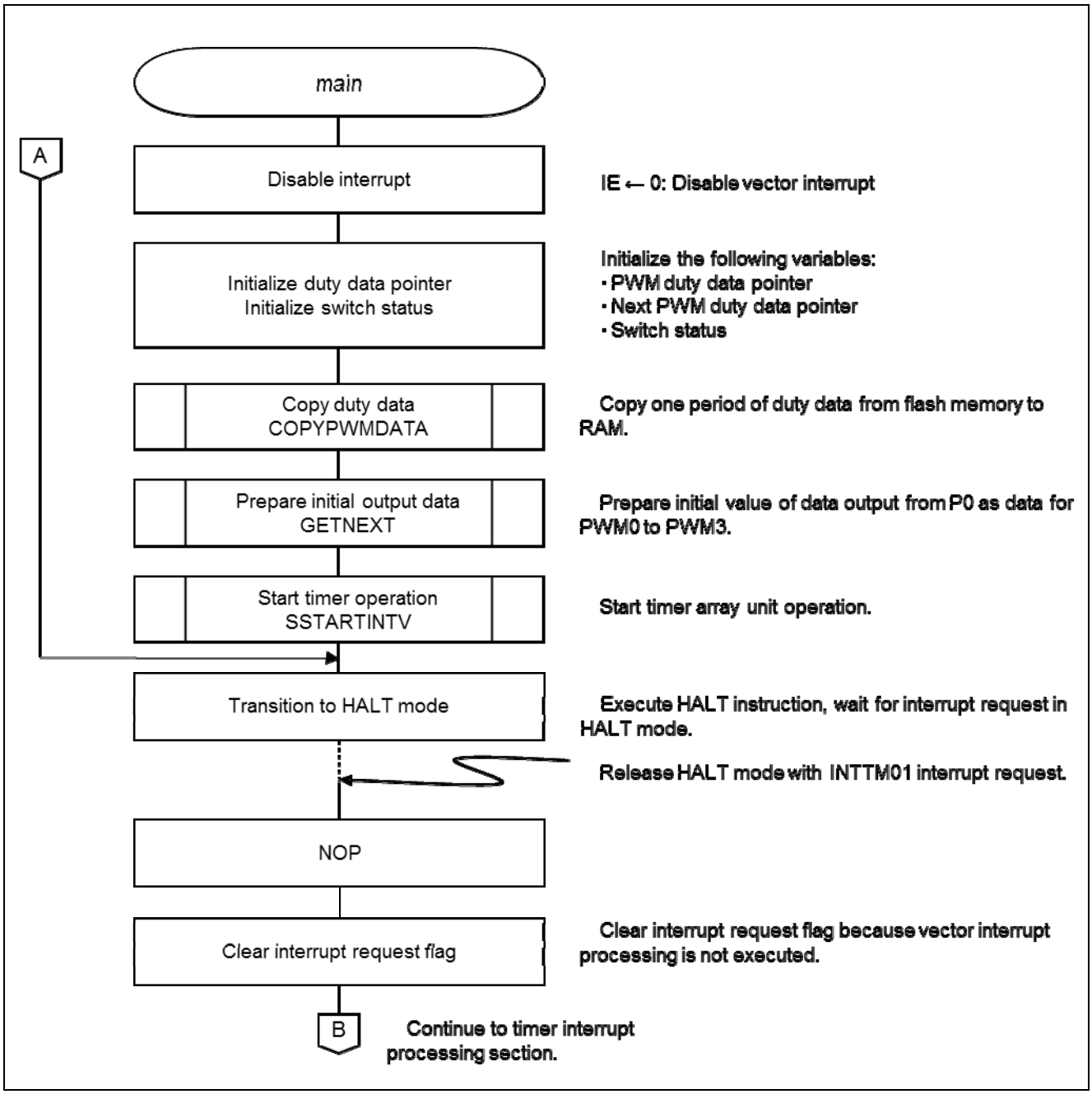

Figure 5.7 Main Processing (1/3)

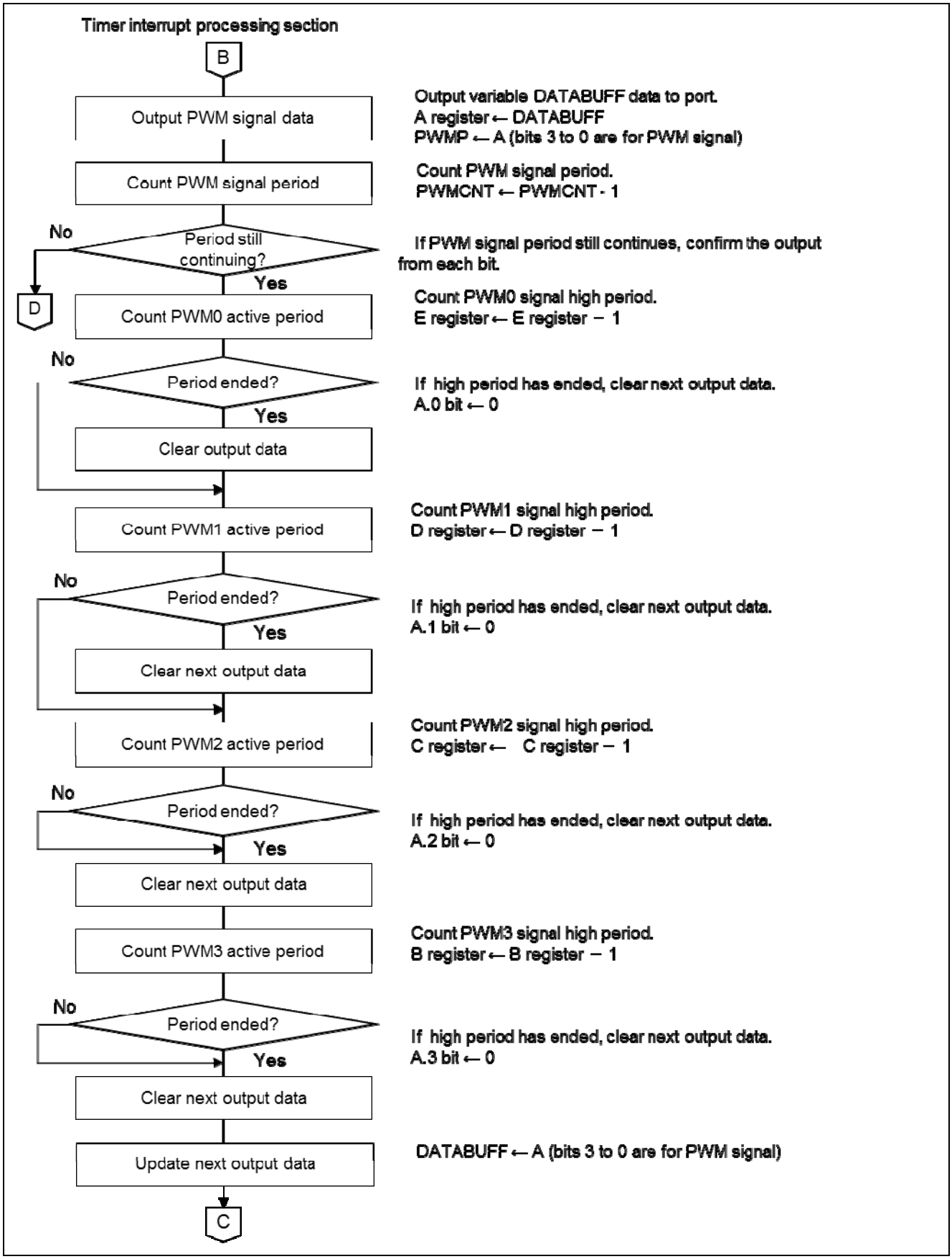

Figure 5.8 Main Processing (2/3)

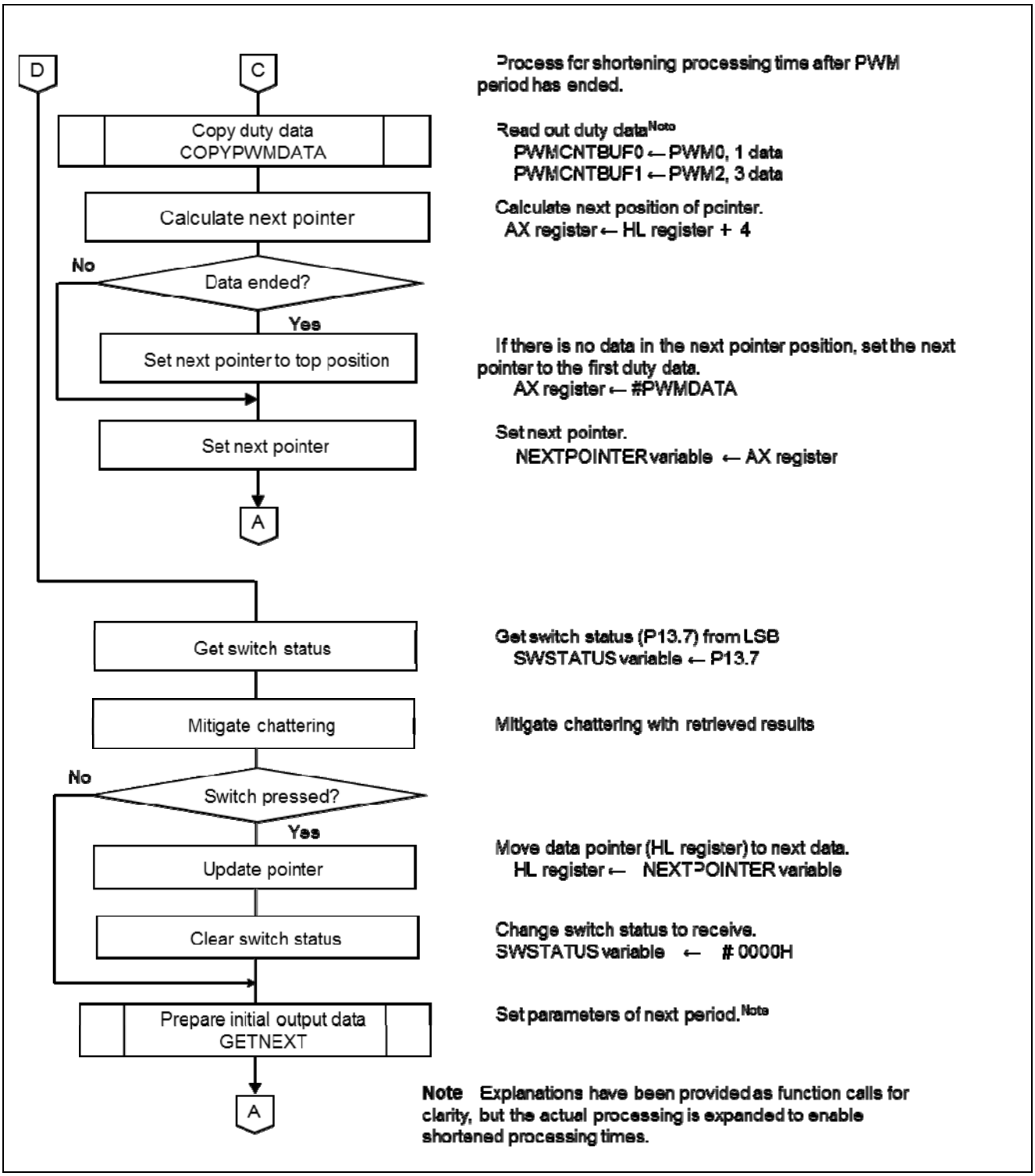

Figure 5.9 Main Processing (3/3)

5.7.6 Timer Array Unit Operation Start

Figure 5.10 shows the flowchart for starting the .

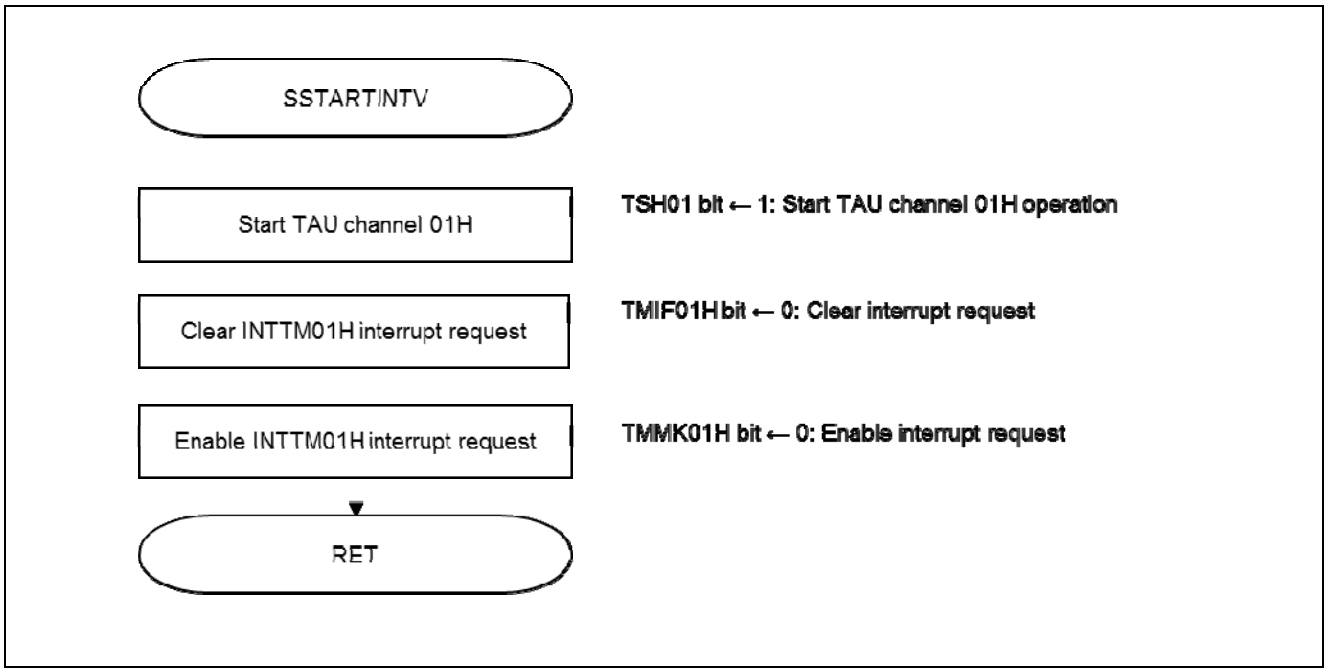

Figure 5.10 Timer Array Unit Operation Start

Timer operation enable setting

・Timer channel start register 0 (TSH0)
Start channel 1 count operation.

Symbol: TSH0

7	6	5	4	3	2	1	0
0	0	0	0	TSH03 Note	0	TSH01	0
0	0	0	0	0	0	**1**	0

Note 16-bit products only

Bit 1

TSH01	Operation enable (start) trigger of channel 1H
0	No trigger operation
1	**Sets TE01 bit to 1 and enters the count operation enabled state.** **When enabled, the count operation of the TCR01 register starts at different times depending on the operation mode.**

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer count completed interrupt setting

- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Set interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	**0**	x	x	x	x	x	x

Bit 6

TMIF01H	Interrupt request flag
0	**Interrupt request signal in not generated**
1	Interrupt request signal is generated, goes to interrupt request state.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	**0**	x	x	x	x	x	x

Bit 6

TMMK01H	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

5.7.7 Duty Data Copy Processing

Figure 5.11 shows the flowchart for the .

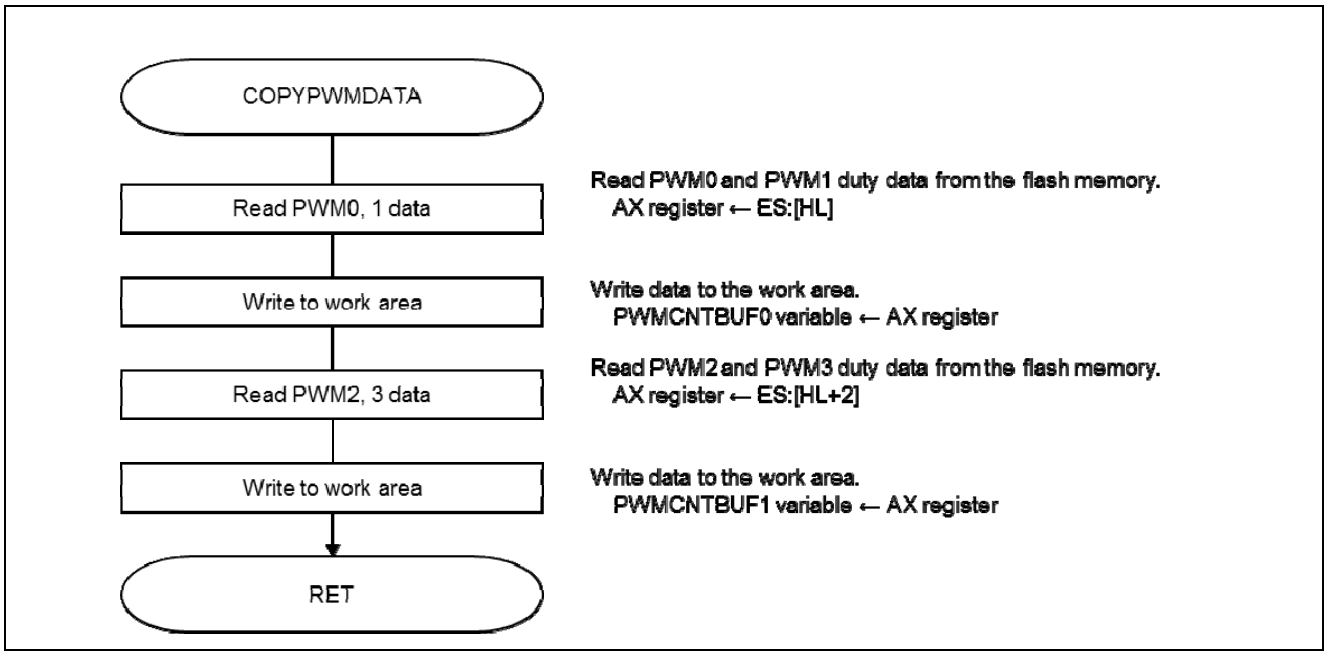

Figure 5.11 Duty Data Copy Processing

5.7.8 Initial Output Data Preparation Processing

Figure 5.12 and Figure 5.13 show the flowchart for initial output data preparation processing.

Symbol E is continued in the second part of the figure (2/2).

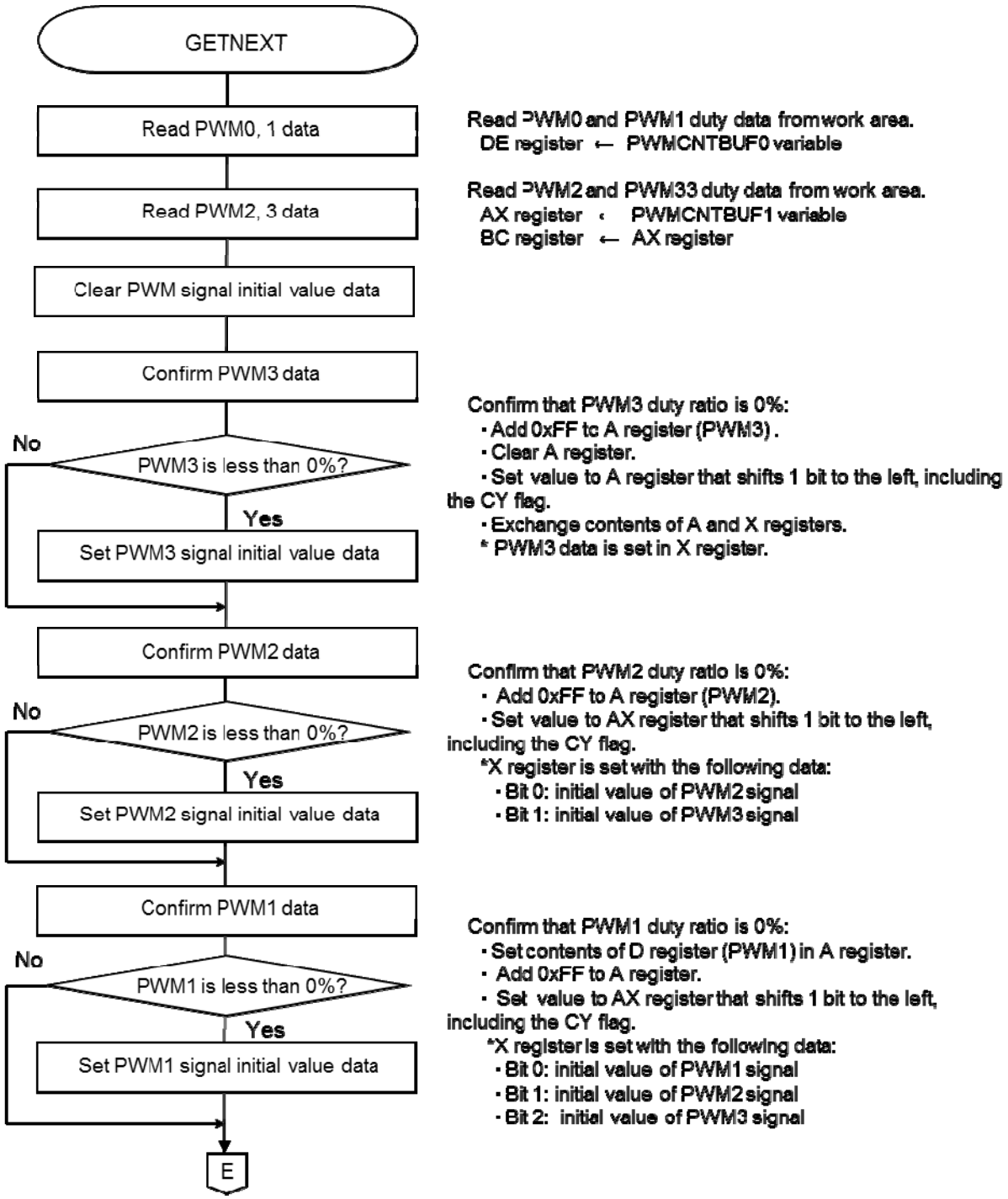

Figure 5.12 Initial Output Data Preparation Processing (1/2)

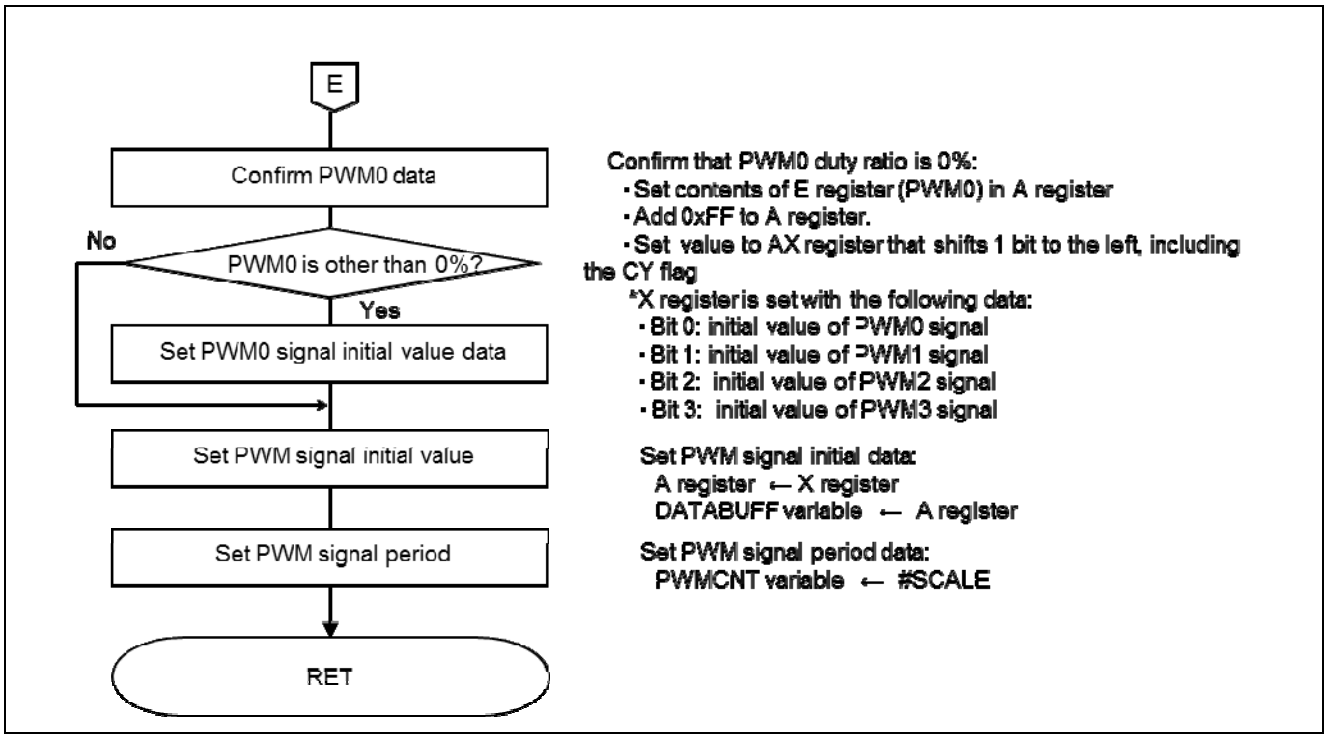

Figure 5.13 Initial Output Data Preparation Processing (2/2)

6. Multiplexed PWM Output Waveform Measurements

6.1 Multiplexed PWM Initial Output Waveform

Table 6.1 lists the pulse width, duty ratio, and duty data setting value of each PWM. Figure 6.1 shows the multiplexed PWM initial output waveform.

Refer to section 5.3Constants for duty data settings values.

Table 6.1 PWM Pulse Width, Duty Ratio, Duty Data Setting Value

PWM	Pulse Width [µs]	Duty Ratio [%]	Duty Data Setting Value
PWM0	3.89	0.39	1
PWM1	39.44	3.98	10
PWM2	78.11	7.88	20
PWM3	156.10	15.70	40

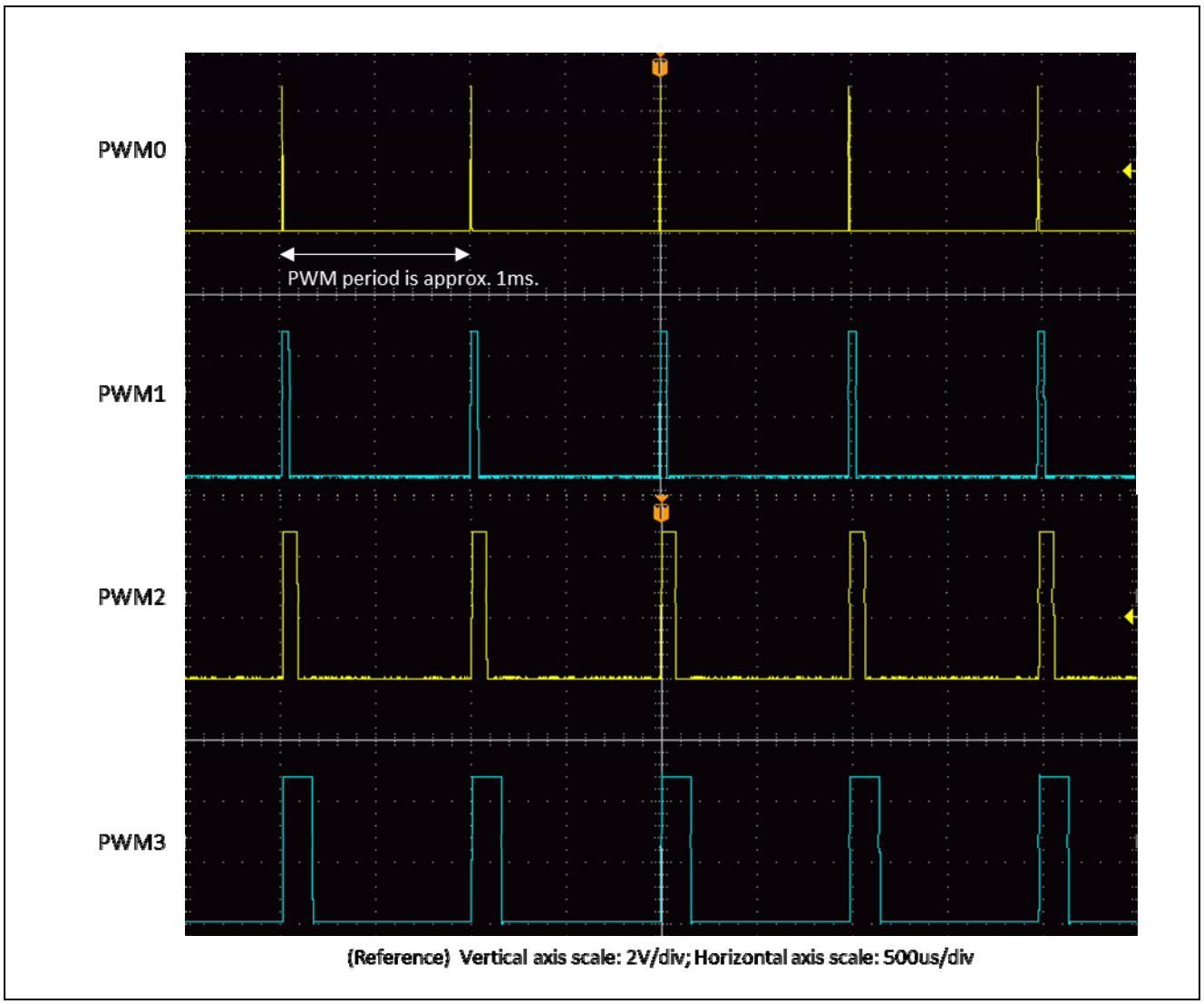

Figure 6.1 Multiplexed PWM Output Initial Waveform

6.2 Multiplexed PWM Output Waveform after External Switch Pressed 1 Time

Table 6.2 lists the pulse width, duty ratio, and duty data setting value of each PWM. Figure 6.2 shows the multiplexed PWM initial output waveform after the external switch is pressed 1 time.

Refer to section 5.3 Constants for duty data settings values.

Table 6.2 PWM Pulse Width, Duty Ratio, Duty Data Setting Value

PWM	Pulse Width [µs]	Duty Ratio [%]	Duty Data Setting Value
PWM0	7.8	0.78	2
PWM1	495.8	49.90	DF50
PWM2	695.4	70.10	DF70
PWM3	97.6	9.84	DF10

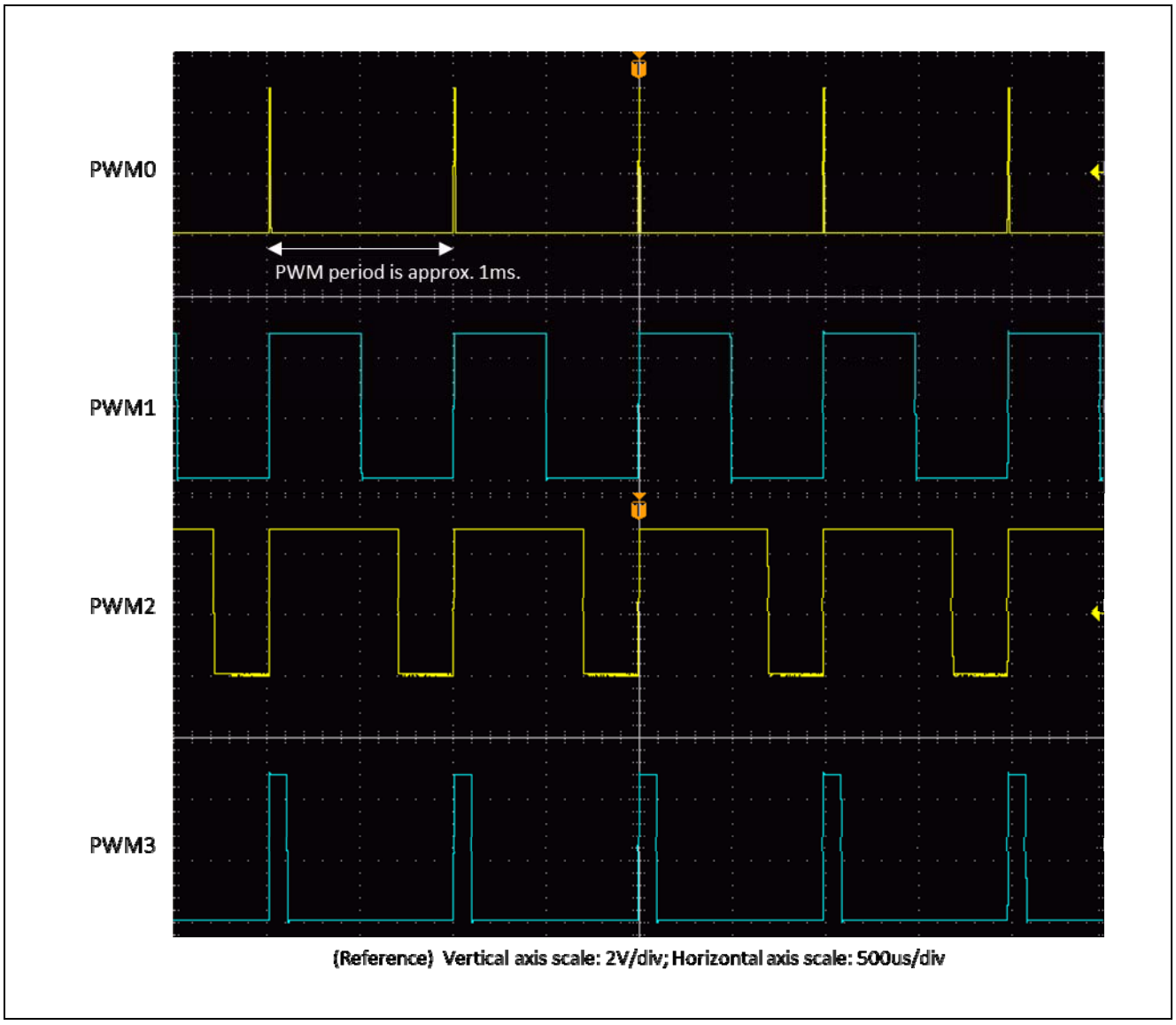

Figure 6.2 Multiplexed PWM Output Waveform after External Switch Pressed 1 Time

6.3 Multiplexed PWM Output Waveform after External Switch Pressed 2 Times

Table 6.3 lists the pulse width, duty ratio, and duty data setting value of each PWM. Figure 6.3 shows the multiplexed PWM initial output waveform after the external switch is pressed 2 times.

Refer to section 5.3 Constants for duty data settings values.

Table 6.3 PWM Pulse Width, Duty Ratio, Duty Data Setting Value

PWM	Pulse Width [µs]	Duty Ratio [%]	Duty Data Setting Value
PWM0	695.3	70.1	DF70
PWM1	792.7	79.9	DF80
PWM2	894.1	90.1	DF90
PWM3	- (fixed to Hi)	100.0	DF100

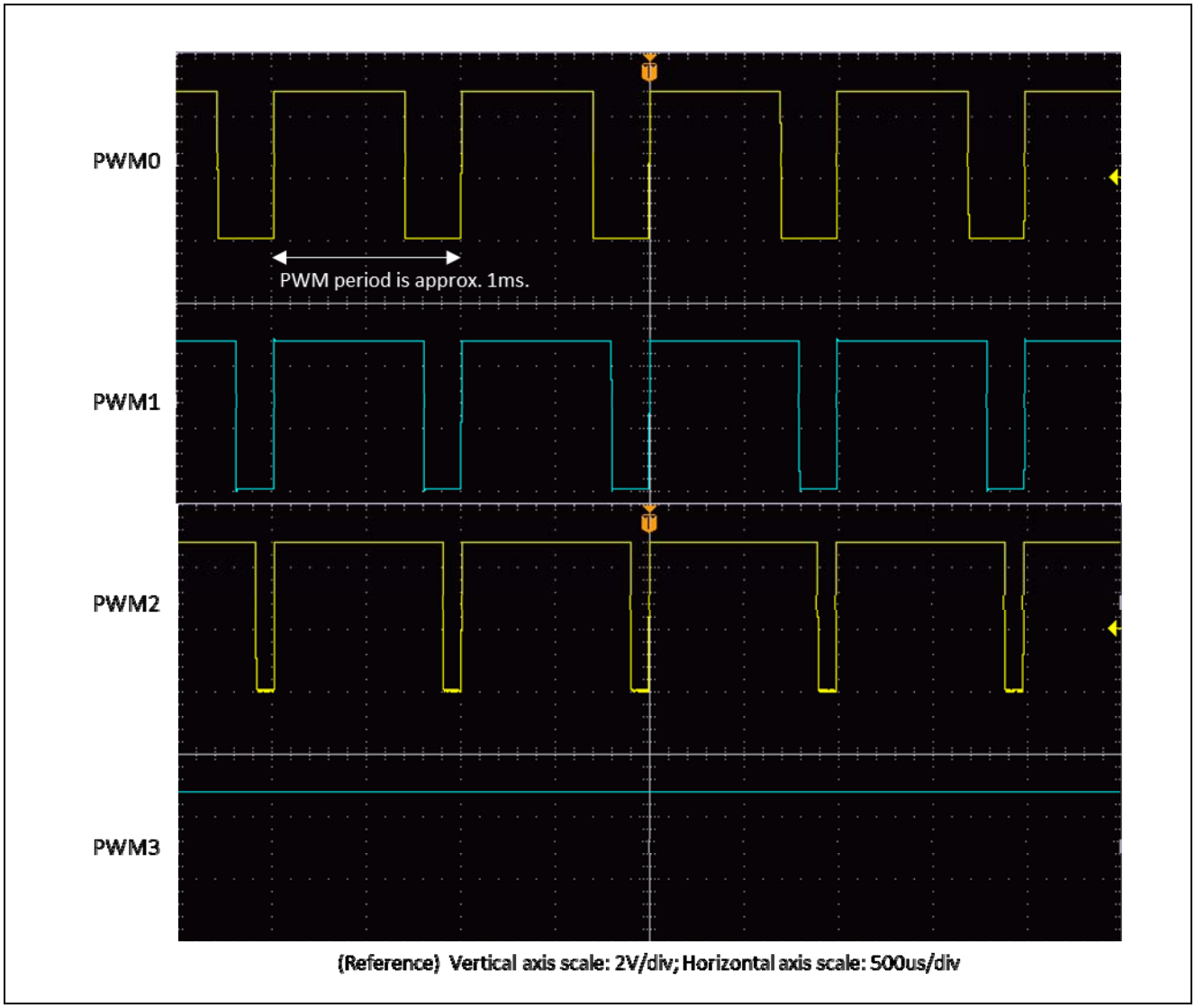

Figure 6.3 Multiplexed PWM Output Waveform after External Switch Pressed 2 Times

6.4 Multiplexed PWM Output Waveform after External Switch Pressed 3 Times

Table 6.4 lists the pulse width, duty ratio, and duty data setting value of each PWM. Figure 6.4 shows the multiplexed PWM initial output waveform after the external switch is pressed 3 times.

Refer to section 5.3s Constants for duty data settings values.

Table 6.4 PWM Pulse Width, Duty Ratio, Duty Data Setting Value

PWM	Pulse Width [µs]	Duty Ratio [%]	Duty Data Setting Value
PWM0	987.8	99.6	253
PWM1	894.0	90.1	DF90
PWM2	97.8	9.9	DF10
PWM3	- (fixed to L)	0.0	DF00

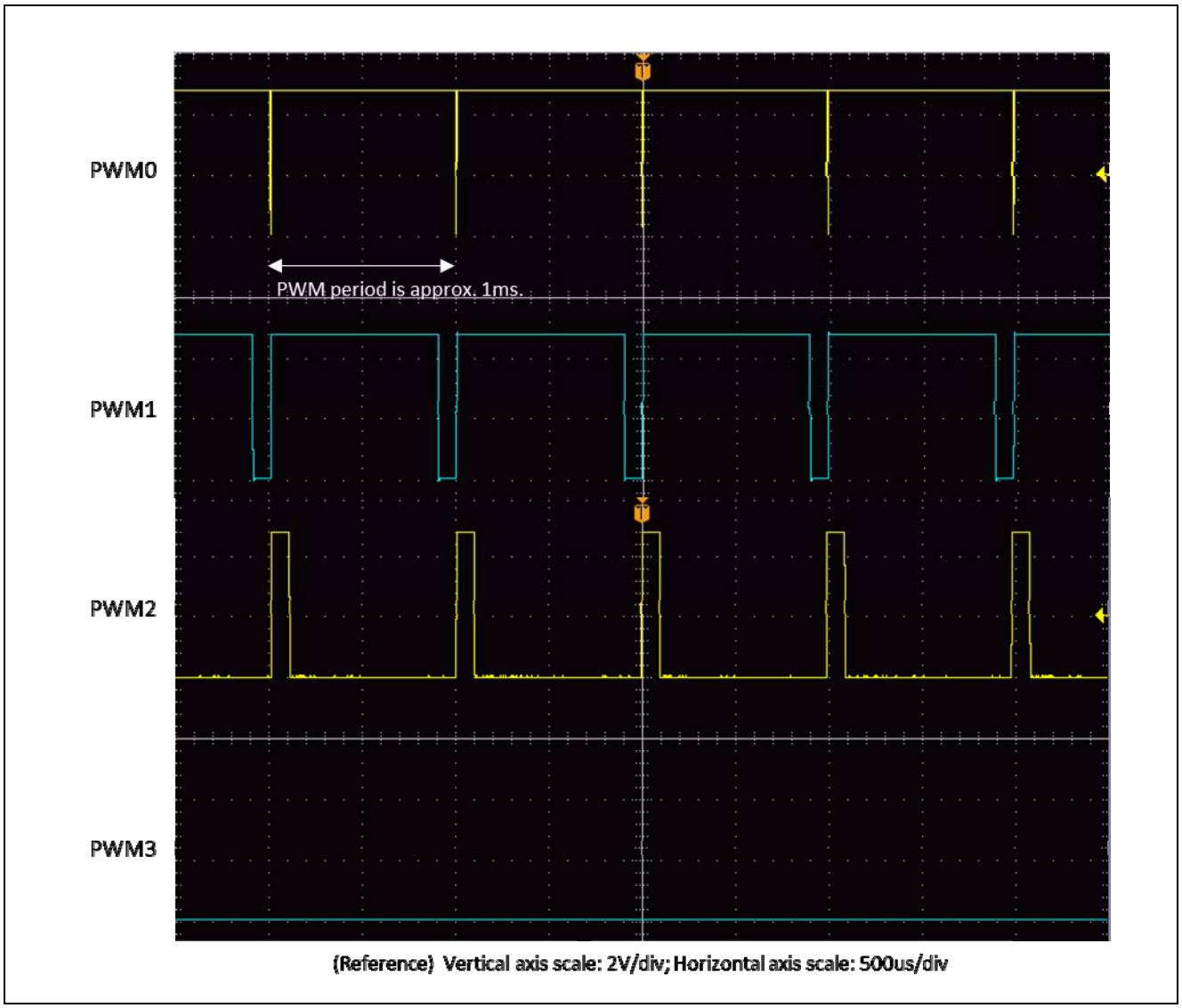

Figure 6.4 Multiplexed PWM Output Waveform after External Switch Pressed 3 Times

7. Sample Code

The sample code is available on the Renesas Electronics Website.

8. Documents for Reference

RL78/G10 User's Manual: Hardware Rev.3.00 (R01UH0384E)

RL78 Family User's Manual: Software Rev.2.20 (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record	RL78/G10 Software-based Multiplexed PWM Output CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	2016.03.11	—	First edition issued

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
  - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
  - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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