RL78/F13, F14

DTC Usage Example (High-Speed Transfer): A/D Converter

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Summary

This document describes how to use the high-speed transfer mode of the data transfer controller (DTC) to transfer A/D conversion results to the conversion result storage area located in the RAM.

Contents

1. Overview of DTC (High-Speed Transfer) Operation

During DTC (high-speed transfer) operation, control data dedicated for high-speed transfer is read when the DTC activation source selected by the high-speed DTC channel select register is generated. Based on the control data information, data is read from the transfer source address and written to the transfer destination address. After writing of the data finishes, control data (transfer counter, transfer source address, and transfer destination address) is written back. The number of clock cycles required for a DTC (high-speed transfer) is four (minimum), in contrast to the eight (minimum) clock cycles required for a normal transfer.

1.1 Normal Mode and Repeat Mode

DTC (high-speed transfer) transfer has two modes: normal mode and repeat mode.

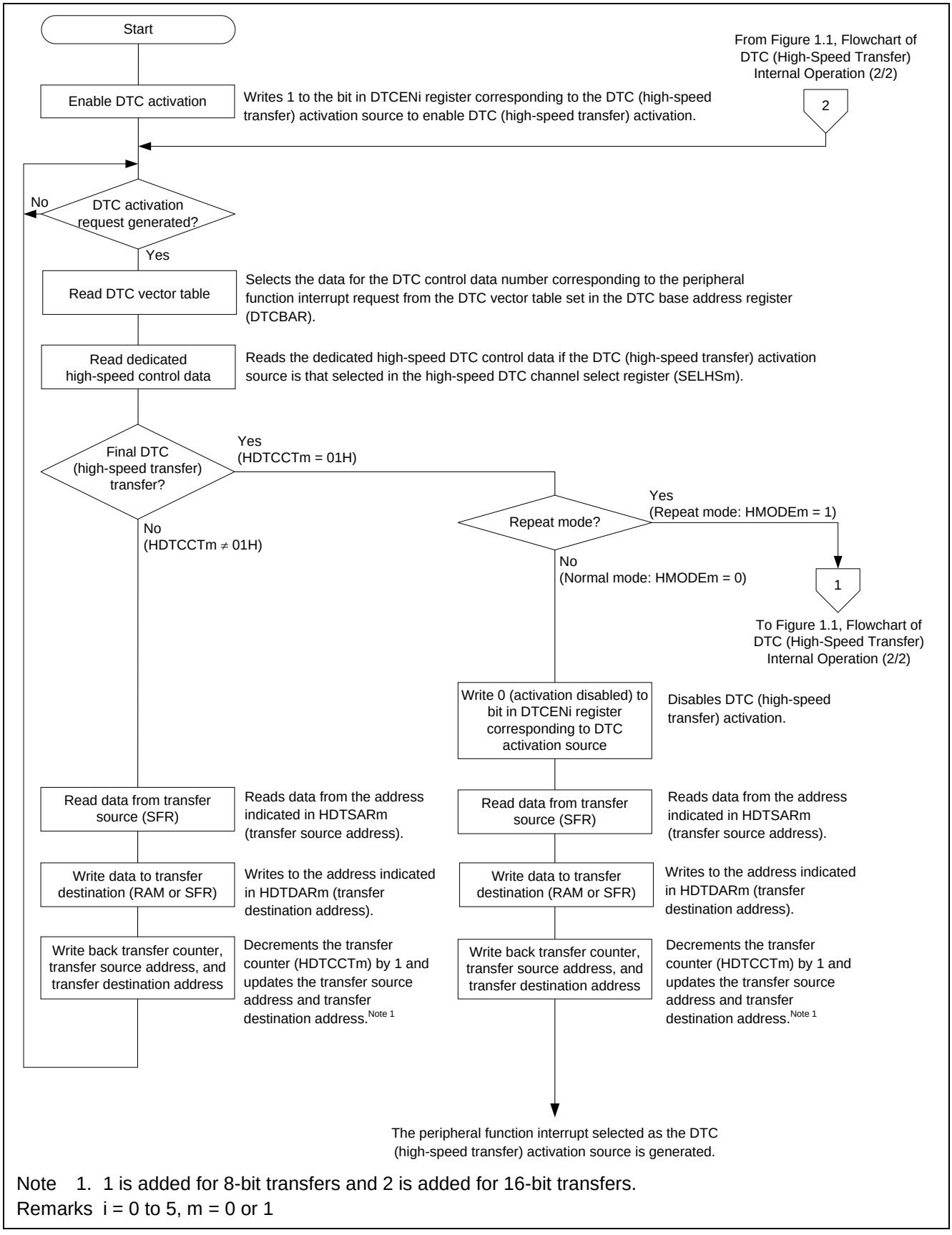
1.1.1 Normal Mode

In normal mode either 8 or 16 bits of data are transferred for each activation. The transfer count can be 1 to 256. Data is transferred and the transfer count is decremented each time the activation source is generated until the specified transfer count reaches 0. When the transfer count value is 0, DTC (high-speed transfer) activation is disabled, and after the data transfer ends a DTC transfer-end interrupt is generated.

1.1.2 Repeat Mode

In repeat mode either 8 or 16 bits of data are transferred for each activation. The transfer count can be 1 to 255. Data is transferred and the transfer count is decremented each time the activation source is generated until the specified transfer count reaches 0. If generation of the DTC transfer-end interrupt is disabled, when the specified transfer count reaches 0, the control data is initialized **(the transfer counter is reloaded, and the repeat area address is initialized)**, and data transfer is repeated. If generation of the DTC transfer-end interrupt is enabled, when the specified transfer count reaches 0, DTC (high-speed transfer) activation is disabled, and after the data transfer ends a DTC transfer-end interrupt is generated.

Figure 1.1 is a flowchart of DTC (high-speed transfer) internal operation in normal mode and repeat mode.



Note 1. 1 is added for 8-bit transfers and 2 is added for 16-bit transfers.

Remarks i = 0 to 5, m = 0 or 1

Figure 1.1 Flowchart of DTC (High-Speed Transfer) Internal Operation (1/2)

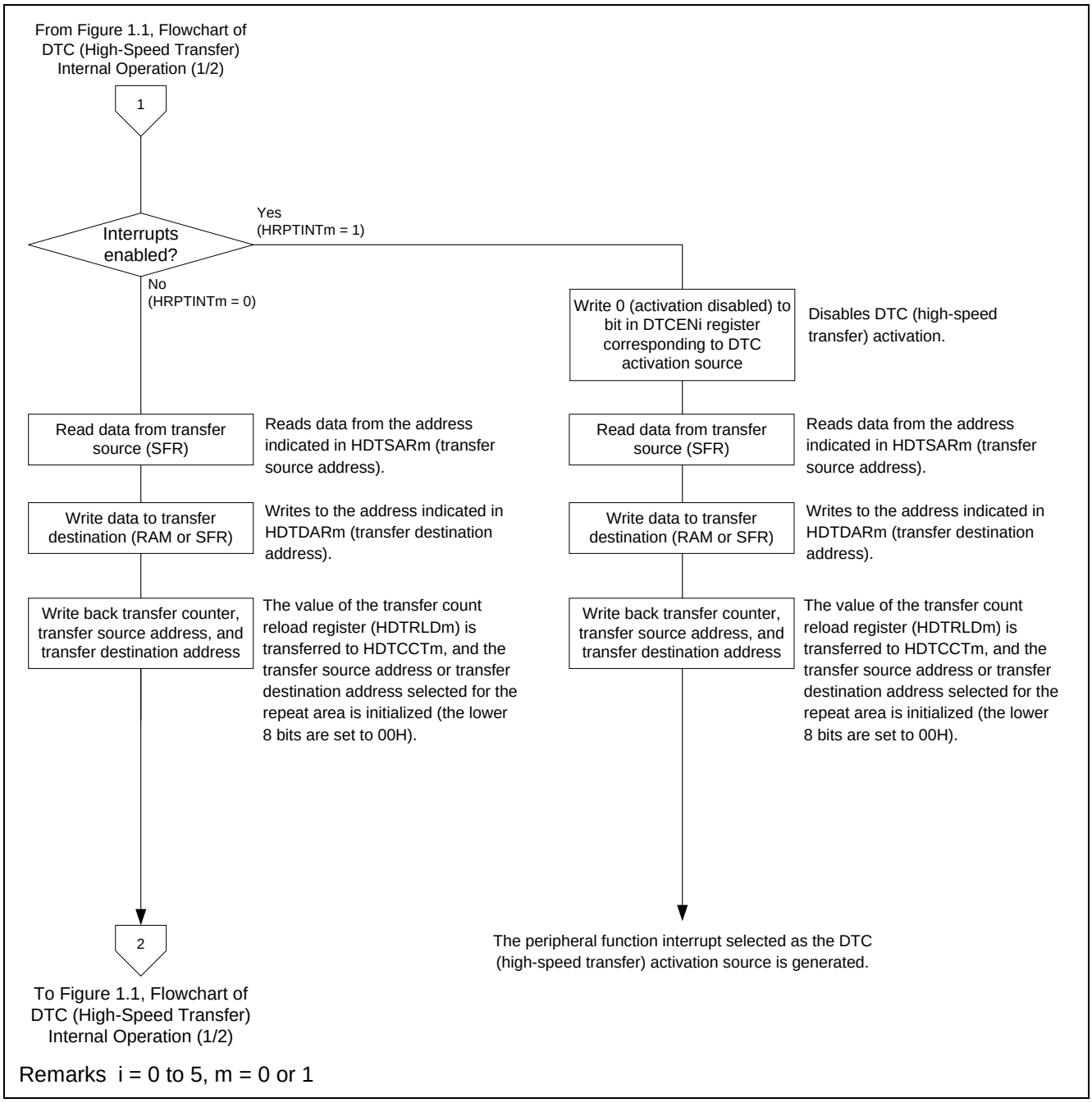


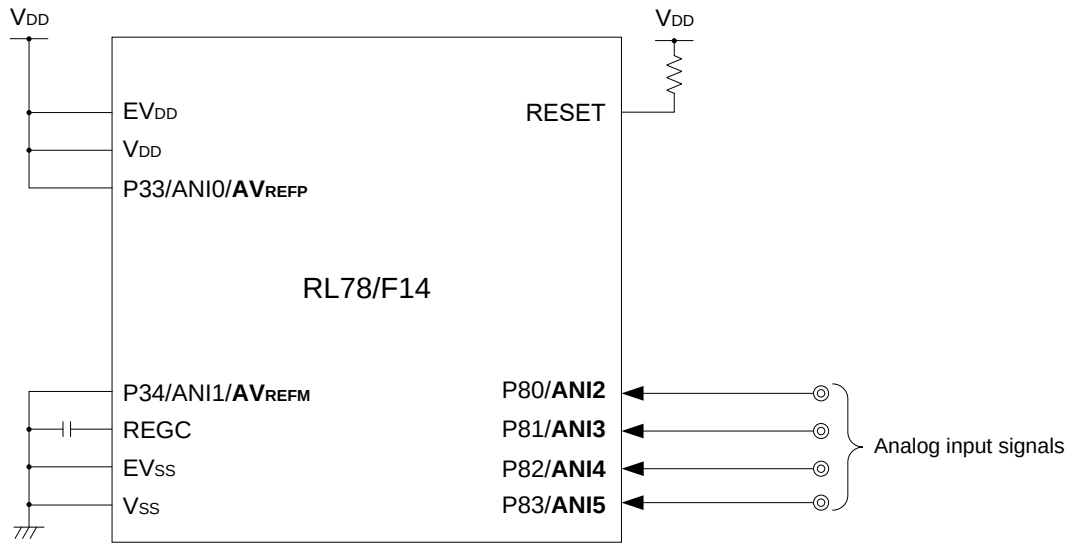
Figure 1.2 Flowchart of DTC (High-Speed Transfer) Internal Operation (2/2)

2. Specifications

A usage example combining DTC (high-speed transfer), the A/D converter, and timer array unit (TAU) channels 0 (TAU00) and channel 1 (TAU01) is presented below.

TAU00 (2 ms) and TAU01 (1 ms) count in coordinated fashion, and the A/D converter uses the TAU01 interrupt request signal as the trigger to start A/D conversion. The DTC uses A/D conversion end as the DTC activation source and stores the A/D conversion result in RAM. Thereafter the processing is repeated.

Figure 2.1 is a connection diagram showing the pins used, Table 2.1 lists the peripheral functions used and their applications, Figure 2.2 is a configuration diagram of the peripheral functions used, and Figure 2.3 shows the DTC (high-speed transfer) transfer timing.



In the application described in this document AV_{REFP}, AV_{REFM}, ANI2, ANI3, ANI4, and ANI5 are used.

Figure 2.1 Connection Diagram of Pins Used

Table 2.1 Peripheral Functions Used and Their Applications

Peripheral Function	Application
DTC (high-speed transfer)	Transfers the A/D conversion results to RAM at A/D conversion end. • DTC (high-speed transfer) activation source: A/D conversion end • Transfer source address: ADCR register • Transfer destination address: RAM • Transfer count: 4 • Operating mode: Repeat mode
A/D converter	Performs A/D conversion on the analog input signals from pins ANI2 to ANI5. • 10-bit resolution • Hardware trigger no-wait mode (source: INTTM01 signal) • Scan mode (4-pin) • One-shot conversion mode
TAU00	Constant-period timer • Interval timer mode (2 ms) • Used as master channel.
TAU01	Generates A/D conversion trigger (INTTM01 signal). • One-count mode (1 ms) • Used as slave channel.

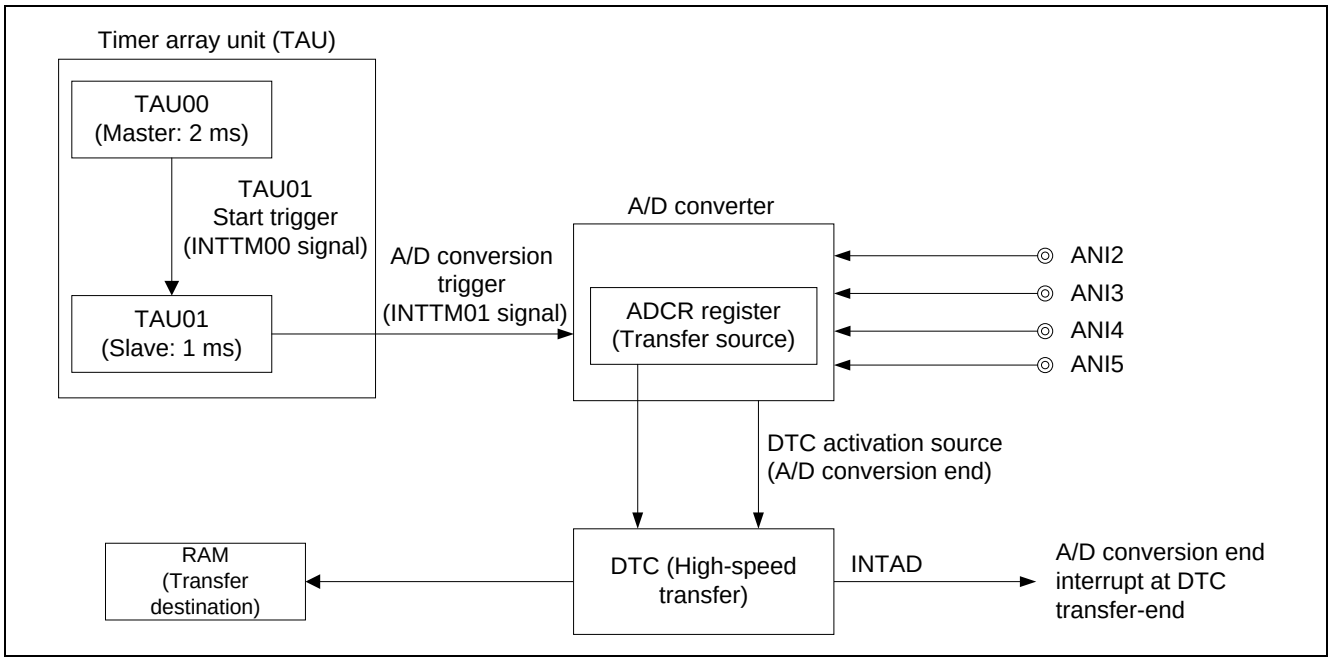
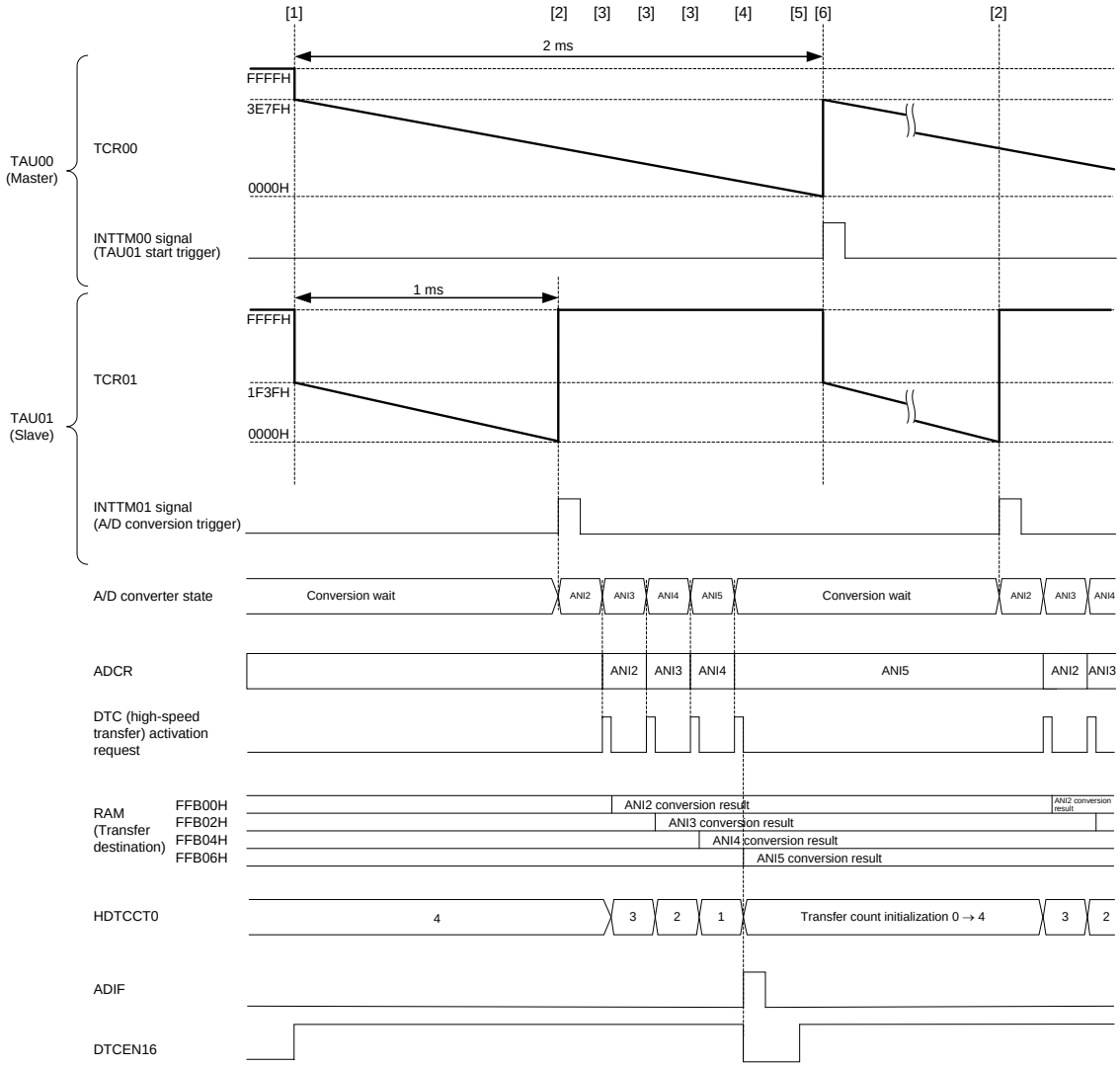


Figure 2.2 Configuration Diagram of Peripheral Functions Used



[1] The DTCEN16 bit in the DTCEN1 register is set to 1 (DTC (high-speed transfer) activation enabled (source: A/D conversion end)) by software. Also, bits TS00 and TS01 in the TS0 register are set to 1 (TAU00 and TAU01 start counting) by software.
[2] When TAU01 finishes counting, the INTTM01 signal is output. Also, A/D conversion starts, using this signal as the trigger.
[3] At A/D conversion end, the DTC (high-speed transfer) performs a memory transfer (ADCR register → RAM). Also, HDTCCT0 is decremented and the DTC (high-speed transfer) transfer destination address is incremented when the DTC (high-speed transfer) transfer takes place.
[4] When the transfer that causes the value of HDTCCT0 to change from 1 to 0 is executed, the following operations are performed:
- The DTCEN16 bit is cleared to 0 (DTC (high-speed transfer) activation disabled).
- The ADIF bit changes to 1 (generation of A/D conversion end interrupt request at DTC (high-speed transfer) transfer-end).
- A DTC (high-speed transfer) data transfer is performed (ADCR register → RAM).
- The value of HDTRLD0 is stored in HDTCCT0 (initialization of DTC (high-speed transfer) transfer count).
- 00H is stored in the lower byte in HDTDAR0 (initialization of transfer destination address).

[5] The DTCEN16 bit in the DTCEN1 register is set to 1 (DTC (high-speed transfer) activation enabled (source: A/D conversion end)) by software.
[6] When TAU00 finishes counting, the INTTM00 signal is output (generation of TAU00 interrupt request signal). Also, TAU01 (slave) starts counting.

Notes: TCR00: Timer counter register 00
INTTM00 signal: TAU00 count-end/capture-end interrupt request signal
TCR01: Timer counter register 01
INTTM01 signal: TAU01 count-end/capture-end interrupt request signal
(Used as A/D conversion trigger.)
ADCR: 10-bit A/D conversion result register
DTC (high-speed transfer) activation request: A/D conversion end interrupt signals for each pin
FFB00H to FFB07H: RAM area (conversion result storage area) indicated by HDTDAR0
(DTC (high-speed transfer) transfer destination address in DTC control data area)
HDTCCT0: High-speed DTC transfer count register 0
ADIF: A/D conversion end interrupt flag
DTCEN16: DTCEN16 bit in DTCEN1 register
The TAU count clock is CK02 (8 MHz).

Figure 2.3 DTC (High-Speed Transfer) Timing

3. Setting Procedures of Peripheral Functions

The setting procedures of the peripheral functions (DTC (high-speed transfer), A/D converter, TAU00, and TAU01) are described in this section.

3.1 Peripheral Function Initialization Procedure

Initialization of the peripheral functions (DTC (high-speed transfer), A/D converter, TAU00, and TAU01) is described below.

Figure 3.1 shows the peripheral function initialization procedure.

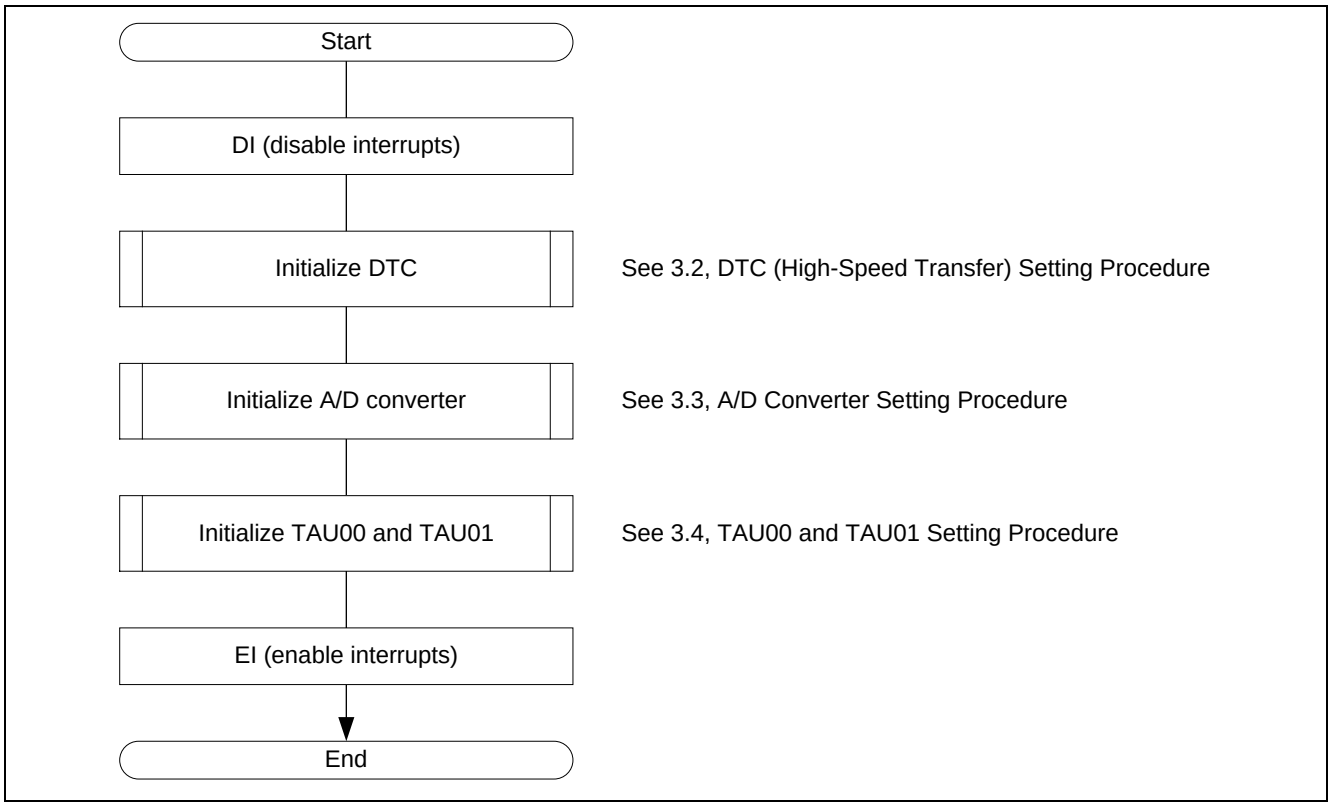


Figure 3.1 Peripheral Function Initialization Procedure

3.2 DTC (High-Speed Transfer) Setting Procedure

The DTC transfers the A/D conversion results to the conversion result storage area in RAM, using the end of A/D conversion as the activation source.

Figure 3.2 shows the DTC (high-speed transfer) initialization procedure.

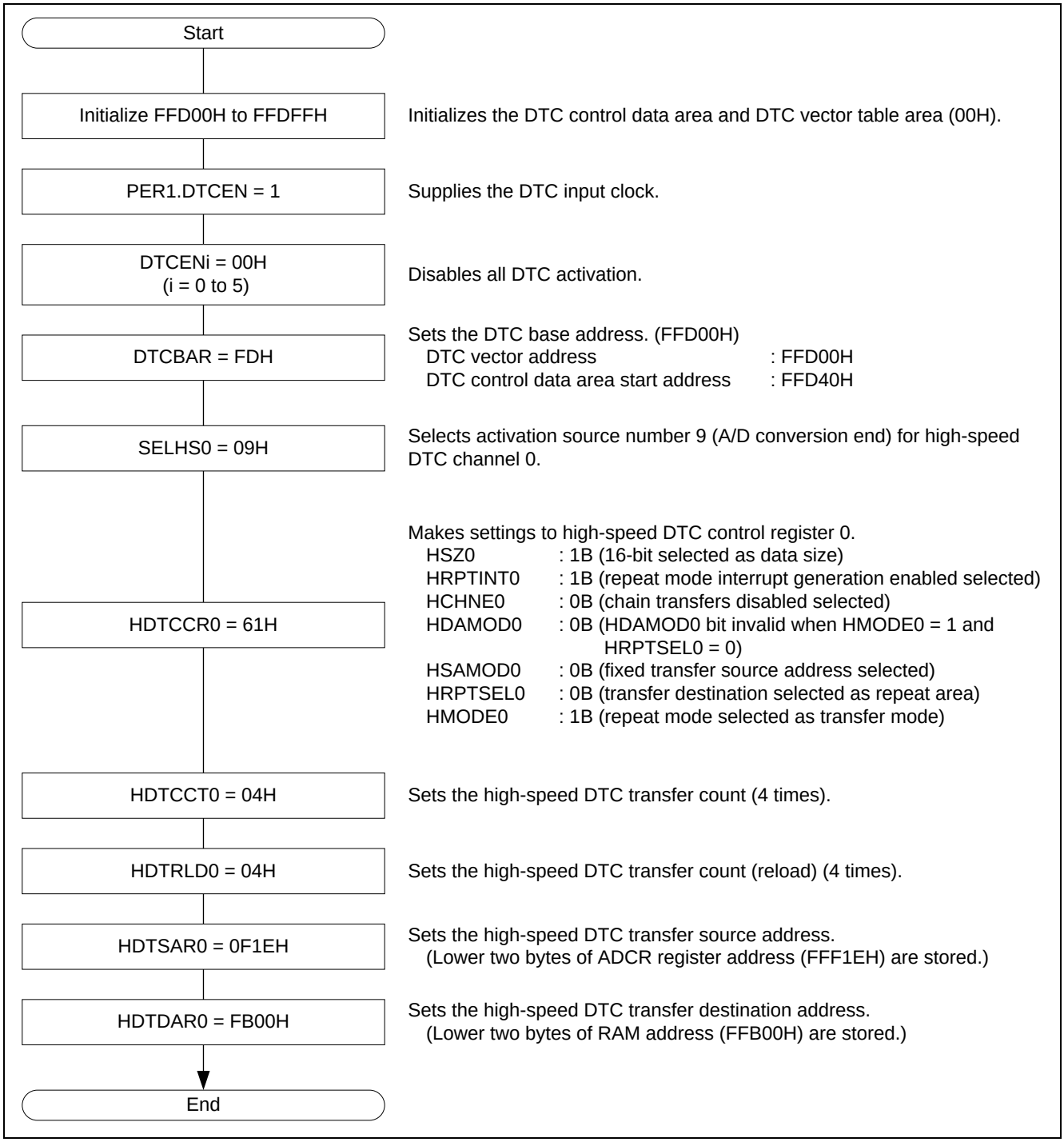


Figure 3.2 DTC (High-Speed Transfer) Initialization Procedure

3.3 A/D Converter Setting Procedure

The following settings are used to perform A/D conversion of the analog input signals on pins ANI2 to ANI5.

Figure 3.3 shows the initialization procedure for the A/D converter.

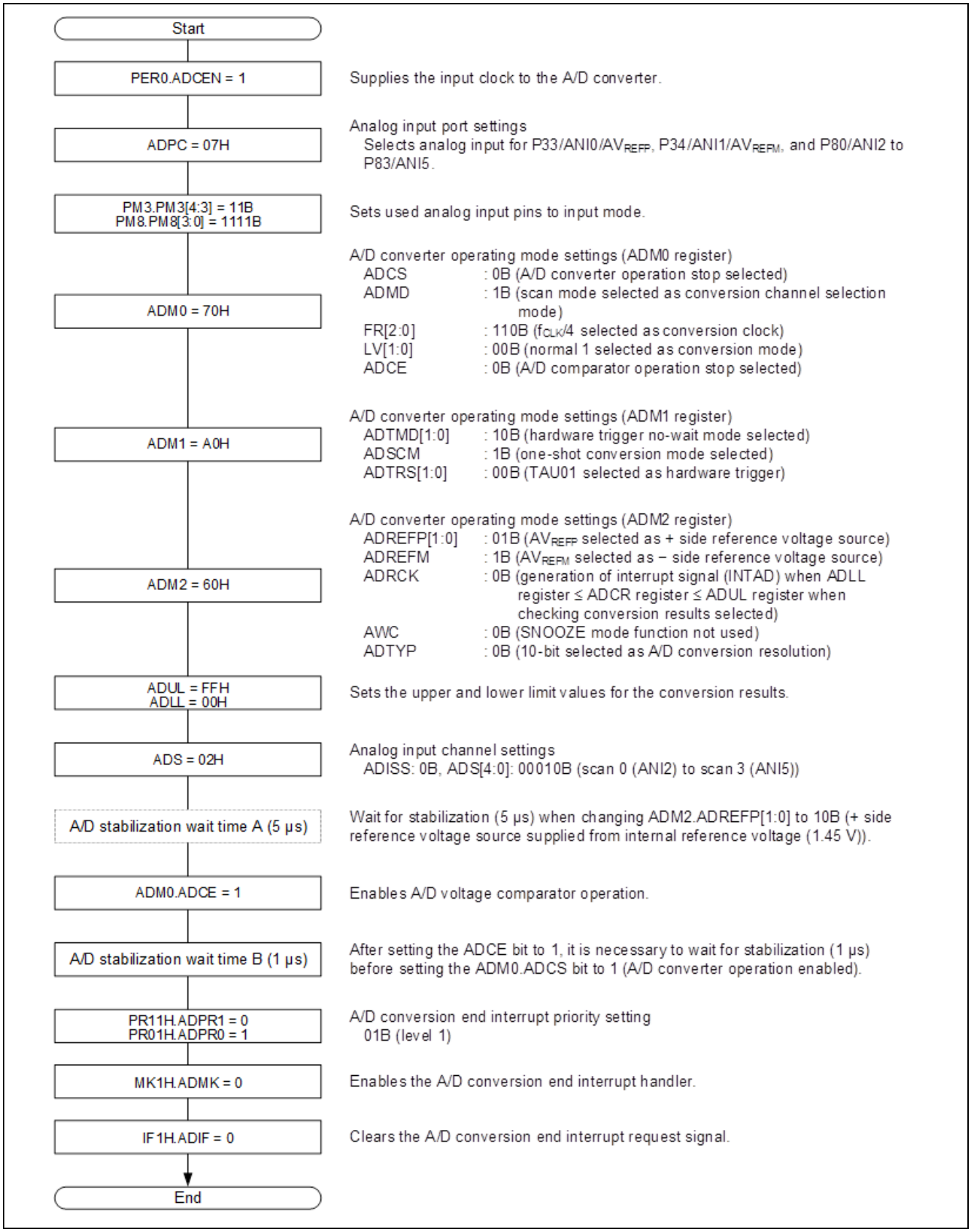


Figure 3.3 A/D Converter Initialization Procedure

3.4 TAU00 and TAU01 Setting Procedure

The timer array unit (TAU) is used as a PWM function. TAU00 is set as the master channel and TAU01 as the slave channel, and a PWM signal is generated with a period of 2 ms and 50% duty. Note that PWM waveforms are not used in this example.

Figure 3.4 shows the initialization procedure for TAU00 and TAU01.

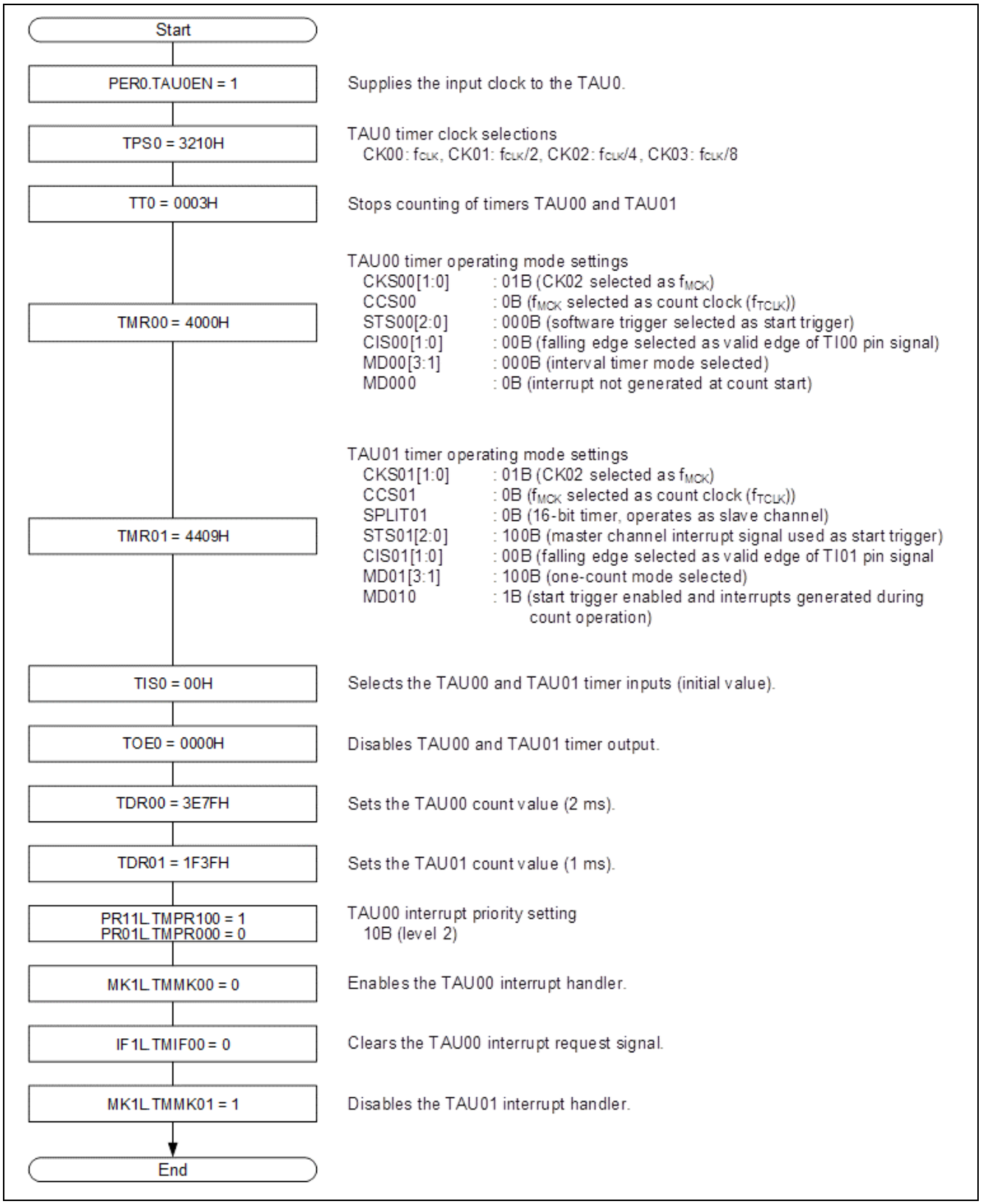
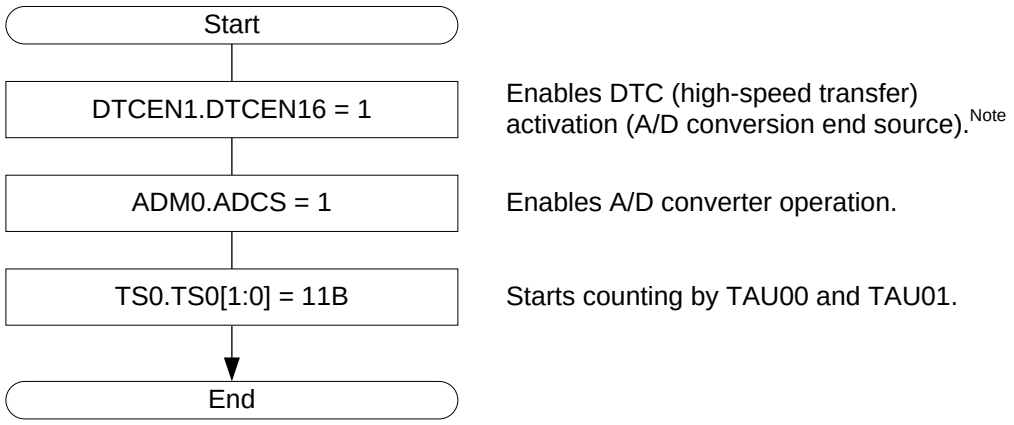


Figure 3.4 TAU00 and TAU01 Initialization Procedure

3.5 Procedure for Enabling Peripheral Functions (DTC (High-Speed Transfer) Transfer Start)

After initializing the peripheral functions (DTC (high-speed transfer), A/D converter, TAU00, and TAU01), the operation is enabled (started).

Figure 3.5 shows the procedure for enabling the operation of the peripheral functions (DTC (high-speed transfer) transfer start).



Note Writing to the DTCEN16 bit should be performed when interrupt sources for which DTC (high-speed transfer) activation is enabled in the DTCEN1 register, and the interrupt source (A/D conversion end) set as activation-enabled, will not be generated.

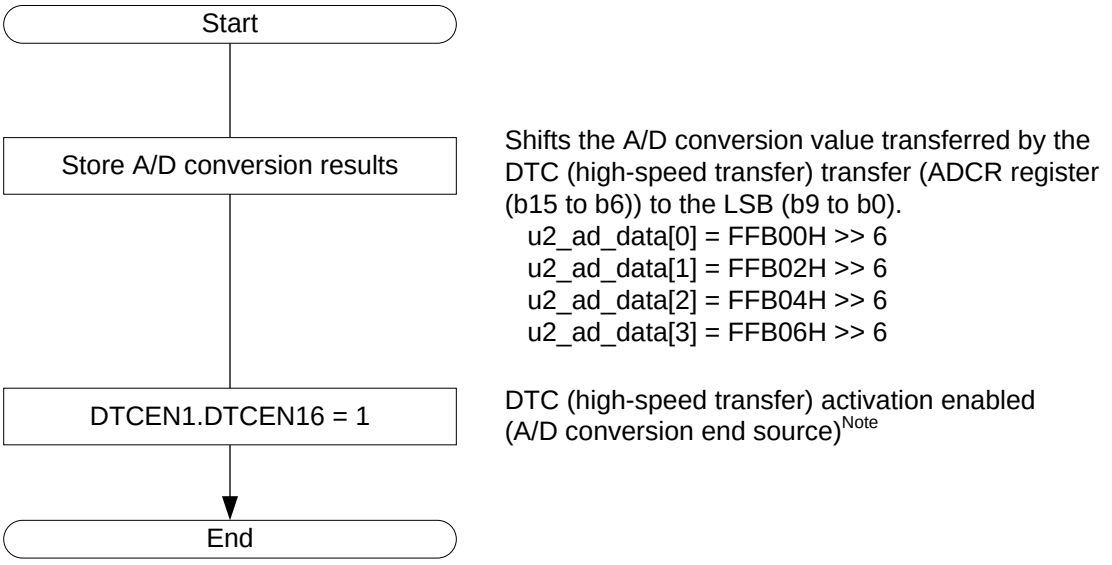
Figure 3.5 Procedure for Enabling Peripheral Functions (DTC (High-Speed Transfer) Transfer Start)

3.6 DTC (High-Speed Transfer) Transfer-End Interrupt Handler

It is possible to generate an interrupt corresponding to the end of DTC (high-speed transfer) transfer operation (the A/D conversion end interrupt in the example described in this document).

Figure 3.6 shows the DTC (high-speed transfer) transfer-end interrupt (A/D conversion end interrupt) handler.

The contents of the upper 10 bits (b15 to b6) of the A/D conversion results stored in memory after the DTC (high-speed transfer) transfer are shifted to the lower 10 bits (b9 to b0). Then, DTC (high-speed transfer) activation is re-enabled.



Note Writing to the DTCEN16 bit should be performed when interrupt sources for which DTC (high-speed transfer) activation is enabled in the DTCEN1 register, and the interrupt source (A/D conversion end) set as activation-enabled, will not be generated.

Figure 3.6 DTC (High-Speed Transfer) Transfer-End Interrupt (A/D Conversion End Interrupt) Handler

4. Important Points

4.1 DTC Transfer Cycle Count

When using the DTC (high-speed transfer) under the specifications indicated in the usage example presented in this document, the DTC transfer cycle count is four clock cycles per transfer. See Table 4.1 for details.

Table 4.1 DTC (High-Speed Transfer) Transfer Clock Cycle Count (Transfer Source: ADCR Register, Transfer Destination: RAM, Repeat Mode)

Vector Read	Control Data		Data Read	Data Write	Total
	Read	Write-Back			
1		1	1	1	4

Note: See Table 4.2 for the control data write-back clock cycle count, Table 4.3 for the data read clock cycle count, and Table 4.4 for the data write clock cycle count. The settings used in the example presented in this document are indicated in Table 4.2 to Table 4.4 by the white unshaded cells.

Table 4.2 Clock Cycle Count Necessary for DTC (High-Speed Transfer) Control Data Write-Back

HDTCCRm Register Settings				Address Settings		Write-Back Control Registers				Clock Cycles
HDAMODm	HSAMODm	HRPTSELm	HMODEm	Transfer Source	Transfer Destination	HDTCCTm	HDTRLDm	HDTSARm	HDTDARm	
0	0	X	0	Fixed	Fixed	Write-back	—	—	—	1
0	1	X	0	Incremented	Fixed	Write-back	—	Write-back	—	1
1	0	X	0	Fixed	Incremented	Write-back	—	—	Write-back	1
1	1	X	0	Incremented	Incremented	Write-back	—	Write-back	Write-back	1
0	X	1	1	Repeat	Fixed	Write-back	—	Write-back	—	1
1	X	1	1	Repeat	Incremented	Write-back	—	Write-back	Write-back	1
X	0	0	1	Fixed	Repeat	Write-back	—	—	Write-back	1
X	1	0	1	Incremented	Repeat	Write-back	—	Write-back	Write-back	1

Note: X: 0 or 1, —: no write-back, m = 0, 1

Table 4.3 DTC (High-Speed Transfer) Data Read Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
—	—	—	1	1	1 + wait cycle count

Note A wait (1 clock cycle) is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

Table 4.4 DTC (High-Speed Transfer) Data Write Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
1	—	—	1	1	1 + wait cycle count

Note A wait (1 clock cycle) is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

4.2 DTC Usage Notes

- Do not use a DTC transfer to access DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCCTm, HDTRLDm, HDTSARm, and HDTDARm) or the DTC control data area, DTC vector table area, or general-register (FFEE0H-FFEFFH) space in the RAM. Also, when using self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function, do not access the memory areas associated with those functions.
- Write to or change the DTCENi register only when the interrupt sources for which the DTC activation is enabled in the target register, and the interrupt sources set as activation-enabled will not be generated.
- Do not use the memory areas associated with the general-register (FFEE0H-FFEFFH) space, self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function as the DTC control data area or DTC vector table area.
- Only make changes to the DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCCTm, HDTRLDm, HDTSARm, and HDTDARm), the registers assigned to the DTC control data area (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj), and the DTC vector table area when all DTC activation sources are set as activation-disabled (corresponding bits in DTCENi register cleared to 0).
- Make initial settings (write random values) to the DTC control data area and DTC vector table area in the RAM. The DTC vector table area (64 bytes; including reserved areas) must not be used as general-purpose RAM by user programs. Note that portions of the DTC control data area (192 bytes) that are not used by the DTC can be used as general-purpose RAM.
- Do not overwrite DTCBAR more than once.
- When a DTC transfer-pending instruction (call or return instruction, unconditional or conditional branch instruction, instruction for accessing code flash memory, instruction for accessing interrupt-related registers (IFxx, MKxx, and PRxx) or PSW, instruction for accessing the data flash, or multiply, divide, or multiply-and-accumulate instruction - except for the MULU instruction) is executed, the DTC transfer does not take place and the request is put on hold. Also, no DTC transfer takes place during a PREFIX instruction and for a period equal to one instruction immediately following it.
- If a data flash access instruction is executed during the period equal to one instruction after the activation of a DTC data transfer, a wait of three clock cycles occurs due to the specifications of the internal bus.
- The DTC transfer is put on hold when an access is made to an SFR requiring a wait (CAN or LIN register, or the TRJ0 register of timer RJ).
- From the point at which a DTC activation source is generated until the point at which the DTC transfer completes, the same activation source should not be generated again.
- If there is a conflict between DTC activation sources, the priorities of the activation sources are considered. The source with the higher priority (based on the source number) takes effect, and the source with the lower priority is put on hold.
- In order to read from the DTC control data area and DTC vector table area during high-speed transfer operation, write random values to them before enabling DTC transfer operation.
- In repeat mode, the lower byte of the address (setting value) of the repeat area must have a value of 00H. Also note that the transfer count and reload transfer count will differ according to the transfer data size.
  - 8-bit transfer: 01H to FFH (1 to 255 times)
  - 16-bit transfer: 01H to 7FH (1 to 127 times)

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Revision History

Rev.	Date	Description	
		Page	Summary
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