RL78/F12

Option Byte Setting

Introduction

This application note gives additional information on the description of the Option Bytes (User Option Byte and On-Chip Debug Option Byte) in the RL78/F12 User's Manual: Hardware. This document explains considerations when each value of the Option Byte is selected, such as the grade (J-grade or K-grade), supply voltage, and operation frequency. For details, refer to the User's Manual: Hardware.

Contents

1. Option Bytes of RL78/F12

The Option Bytes of the RL78/F12 are located in the address range 000C0H to 000C3H of the flash memory. The Option Bytes consist of the User Option Byte (000C0H to 000C2H) and On-Chip Debug Option Byte (000C3H). Automatically referenced at a power-on reset or a reset release, the Option Bytes control each corresponding function. When using boot swap function, set the same value in the memory address range 000C0H to 000C3H and 010C0H to 010C3H in order to switch boot cluster 0 (00000H to 00FFFH) and boot cluster 1 (01000H to 01FFFH). This document describes considerations when setting the Option Bytes of the RL78/F12 products.

1.1 User Option Byte (000C0H)

The User Option Byte (000C0H) specifies the watchdog timer operation. The bits of the User Option Byte (000C0H) are shown in Figure 1, and the setting considerations are shown in Table 1.

b7	b6	b5	b4	b3	b2	b1	b0
WDTINT	WINDOW [1:0]		WDTON	WDCS [2:0]			WDSTBYON

Bit Symbol	Function
WDSTBYON	0: Counter operation stopped in HALT / STOP mode 1: Counter operation enabled in HALT / STOP mode
WDCS [2:0]	Watchdog timer overflow time (Count source: f_{IL} Note 1) 000B: $2^6/f_{IL}$ (3.71 ms to 5.02 ms) 001B: $2^7/f_{IL}$ (7.42 ms to 10.04 ms) 010B: $2^8/f_{IL}$ (14.84 ms to 20.08 ms) 011B: $2^9/f_{IL}$ (29.68 ms to 40.16 ms) 100B: $2^{11}/f_{IL}$ (118.72 ms to 160.63 ms) 101B: $2^{13}/f_{IL}$ (474.90 ms to 642.51 ms) 110B: $2^{14}/f_{IL}$ (949.80 ms to 1285.02 ms) 111B: $2^{16}/f_{IL}$ (3799.19 ms to 5140.08 ms)
WDTON Note 2	0: Counter operation disabled (counting stopped after reset) 1: Counter operation enabled (counting started after reset)
WINDOW [1:0]	01B: Watchdog timer window open period: 50 % 10B: Watchdog timer window open period: 75 % Note 3 11B: Watchdog timer window open period: 100 % 00B: Setting prohibited
WDTINT	0: Interval interrupt of watchdog timer is not used 1: Interval interrupt of watchdog timer is generated

Notes: 1. Oscillator characteristic of f_{IL} (Low-speed on-chip oscillator clock frequency) is 12.75 kHz to 17.25 kHz. Take this oscillator characteristic of f_{IL} into consideration when clearing the watchdog timer counter.
2. The invalid memory access detection function is always enabled when WDTON = 1, regardless of the setting of the IAWEN bit of the IAWCTL register.
3. If the watchdog timer counter clear instruction (writing “ACH” to the WDTE register) is executed when the watchdog timer counter reaches 50 % of the overflow time with the setting of the window open period to 75 %, the counter might not be cleared and a watchdog timer reset might be caused. Refer to technical update “TN-RL*-A068A/E”.

Figure 1. User Option Byte (000C0H)

Table 1. User Option Byte (000C0H) Setting Considerations

Bit Symbol	Setting Considerations
WDSTBYON	• Watchdog timer window open period is 100 % when this bit is 0, regardless of the value of the WINDOW [1:0] bits.
WDCS [2:0]	• In consideration of oscillator characteristic, clear the watchdog timer counter within the watchdog timer window open period (configured with the WINDOW [1:0] bits).
WDTON	• The invalid memory access detection function is enabled when this bit is 1. When not using watchdog timer, clear this bit to 0.
WINDOW [1:0]	• Be sure to set any one of 01B, 10B, or 11B. • When these bits are set to 10B (the window open period: 75 %), the watchdog timer counter must be cleared except when the counter reaches 50 %. • Watchdog timer window open period is 100 % when the WDSTBYON bit is 0, regardless of the value of these bits.
WDTINT	• Set this bit to 1 when using the interval interrupt of watchdog timer and reading the WDTIIF bit of the IF0L register to check if an interrupt request has been generated.

Caution: Set the same value at addresses 000C0H and 010C0H when the boot swap operation is used.

1.2 User Option Byte (000C1H)

The User Option Byte (000C1H) specifies the operation of voltage detector. The bits of User Option Byte (000C1H) are shown in Figure 2, and the setting considerations are shown in Table 4.

b7	b6	b5	b4	b3	b2	b1	b0
VPOC [2:0]			1	LVIS [1:0]		LVIMDS [1:0]	

Bit Symbol	Function
LVIMDS [1:0]	These bits specify the operation mode of the voltage detector 01B: Interrupt mode 10B: Interrupt & reset mode 11B: Reset mode 00B: Setting prohibited
LVIS [1:0]	The functions of these bits depend on the operation mode of the voltage detector. Refer to Table 2 and Table 3.
VPOC [2:0]	

Figure 2. User Option Byte (000C1H)

Table 2. Setting of VPOC [2:0] and LVIS [1:0] Bits When Interrupt Mode Note 1 or Reset Mode is Selected

VPOC [2:0]	LVIS [1:0]	Rise / Fall Detection Voltage
000B	−	Setting prohibited
001B	00B	V_{LVI2} selected. [Rise] 3.13 V (3.06 V to 3.28 V) / [Fall] 3.06 V (2.99 V to 3.20 V)
	01B	V_{LVI9} selected. [Rise] 2.09 V (2.04 V to 2.21 V) / [Fall] 2.04 V (1.99 V to 2.14 V) Note 2
	10B	V_{LVI10} selected. [Rise] 1.98 V (1.93 V to 2.09 V) / [Fall] 1.94 V (1.89 V to 2.04 V) Note 2
	11B	V_{LVI11} selected. [Rise] 1.88 V (1.83 V to 1.99 V) / [Fall] 1.84 V (1.79 V to 1.94 V) Notes 2, 3
010B	00B	V_{LVI1} selected. [Rise] 3.75 V (3.66 V to 3.93 V) / [Fall] 3.67 V (3.58 V to 3.83 V)
	01B	V_{LVI6} selected. [Rise] 2.71 V (2.64 V to 2.85 V) / [Fall] 2.65 V (2.59 V to 2.77 V) Note 2
	10B	V_{LVI7} selected. [Rise] 2.61 V (2.55 V to 2.74 V) / [Fall] 2.55 V (2.49 V to 2.67 V) Note 2
	11B	V_{LVI8} selected. [Rise] 2.50 V (2.44 V to 2.63 V) / [Fall] 2.45 V (2.39 V to 2.57 V) Note 2
011B	00B	V_{LVI0} selected. [Rise] 4.06 V (3.96 V to 4.25 V) / [Fall] 3.98 V (3.89 V to 4.15 V)
	01B	V_{LVI3} selected. [Rise] 3.02 V (2.95 V to 3.17 V) / [Fall] 2.96 V (2.89 V to 3.09 V)
	10B	V_{LVI4} selected. [Rise] 2.92 V (2.85 V to 3.07 V) / [Fall] 2.86 V (2.79 V to 2.99 V)
	11B	V_{LVI5} selected. [Rise] 2.81 V (2.74 V to 2.95 V) / [Fall] 2.75 V (2.68 V to 2.88 V) Note 4
100B to 111B	−	The voltage detector is not used.

Notes: 1. The falling reset voltage is V_{PDR} (1.45 V to 1.58 V) in the interrupt mode. However, the V_{PDR} is outside the operating voltage range of the RL78/F12 products. Therefore, disable the other interrupts when the power voltage supplied after an interrupt generation is within the operation range (*), and after that, put the device into STOP mode by software (for example, by executing an illegal instruction or using the internal reset of the watchdog timer function). When supply voltage exceeds selected V_{LVI}, reset is released.
(*). Operation range of the power supply voltage (V_{DD})
・1.8 V to 5.5 V [J-grade products (T_A = -40 to 85 °C), f_{CLK} = 1 MHz to 8 MHz]
・2.7 V to 5.5 V [J-grade products (T_A = -40 to 85 °C), f_{CLK} = 1 MHz to 32 MHz]
・2.7 V to 5.5 V [K-grade products (T_A = -40 to 125 °C), f_{CLK} = 1 MHz to 24 MHz]
f_{CLK}: CPU / Peripheral hardware clock frequency
2. Setting is prohibited because the use of K-grade or J-grade products under the condition where V_{DD} is 2.7 V to 5.5 V is not supported.
3. Reset mode can be selected but interrupt mode cannot be selected when J-grade products are used under the conditions where V_{DD} is 1.8 V to 5.5 V and f_{CLK} is 1 MHz to 8 MHz.
4. Reset mode is selectable but interrupt mode is not when J-grade or K-grade products are used under the condition where V_{DD} is 2.7 V to 5.5 V. Both the reset mode and interrupt mode are selectable when J-grade products are used under the conditions where V_{DD} is 1.8 V to 5.5 V and f_{CLK} is 1 MHz to 8 MHz.

Caution: When using voltage detector, be sure to select a value that is within the acceptable range of the power supply to be used. Also, be sure to use an external reset circuit when not using the voltage detector.

Table 3. Setting of VPOC [2:0] Bits and LVIS [1:0] Bits When Interrupt & Reset Mode Is Selected

VPOC [2:0]	LVIS [1:0]	Reset / Reset Release / Interrupt Detection Voltage
000B	–	Setting prohibited
001B	00B	V_{LVI2} selected. [Reset] 1.84 V (1.79 V to 1.94 V) / [Reset release] 3.13 V (3.06 V to 3.28 V) / [Interrupt] 3.06 V (2.99 V to 3.20 V) Note
	01B	V_{LVI9} selected. [Reset] 1.84 V (1.79 V to 1.94 V) / [Reset release] 2.09 V (2.04 V to 2.21 V) / [Interrupt] 2.04 V (1.99 V to 2.14 V) Note
	10B	V_{LVI10} selected. [Reset] 1.84 V (1.79 V to 1.94 V) / [Reset release] 1.98 V (1.93 V to 2.09 V) / [Interrupt] 1.94 V (1.89 V to 2.04 V) Note
	11B	Setting prohibited
010B	00B	V_{LVI1} selected. [Reset] 2.45 V (2.39 V to 2.57V) / [Reset release] 3.75 V (3.66 V to 3.93 V) / [Interrupt] 3.67 V (3.58 V to 3.83 V) Note
	01B	V_{LVI6} selected. [Reset] 2.45 V (2.39 V to 2.57V) / [Reset release] 2.71 V (2.64 V to 2.85 V) / [Interrupt] 2.65 V (2.59 V to 2.77 V) Note
	10B	V_{LVI7} selected. [Reset] 2.45 V (2.39 V to 2.57V) / [Reset release] 2.61 V (2.55 V to 2.74 V) / [Interrupt] 2.55 V (2.49 V to 2.67 V) Note
	11B	Setting prohibited
011B	00B	V_{LVI0} selected. [Reset] 2.75 V (2.68 V to 2.88 V) / [Reset release] 4.06 V (3.96 V to 4.25 V) / [Interrupt] 3.98 V (3.89 V to 4.15 V)
	01B	V_{LVI3} selected. [Reset] 2.75 V (2.68 V to 2.88 V) / [Reset release] 3.02 V (2.95 V to 3.17 V) / [Interrupt] 2.96 V (2.89 V to 3.09 V)
	10B	V_{LVI4} selected. [Reset] 2.75 V (2.68 V to 2.88 V) / [Reset release] 2.92 V (2.85 V to 3.07 V) / [Interrupt] 2.86 V (2.79 V to 2.99 V)
	11B	Setting prohibited
100B to 111B	–	Setting prohibited

Note: This setting is possible only when using the J-grade products (T_A = -40 to 85 °C) under the conditions where V_{DD} is 1.8 V to 5.5 V and f_{CLK} is 1 MHz to 8 MHz. The use of the K-grade products (T_A = -40 to 125 °C) or J-grade products under the condition where V_{DD} is 2.7 V to 5.5 V is not supported, so the setting is prohibited.
f_{CLK}: CPU / Peripheral hardware clock frequency

Caution: When using voltage detector, be sure to set a value that is within the range of the power supply to be used. Also, be sure to use an external reset circuit when not using the voltage detector.

Table 4. User Option Byte (000C1H) Setting Considerations

Bit Symbol	Setting Considerations
LVIMDS [1:0]	• Do not set these bits to 00B.
LVIS [1:0]	• When the voltage detector is not used, set these bits to 01B or 11B. • When the voltage detector is used, be sure to set a value that is within the range of the power supply to be used. For the Interrupt mode or Reset mode, refer to Table 2. For the Interrupt & Reset mode, refer to Table 3.
b4	• Be sure to set this bit to 1.
VPOC [2:0]	• When the voltage detector is not used, set these bits to 1xxB (x: any bit value). • When the voltage detector is used, do not set any values other than 001B, 010B, or 011B for these bits. Also, be sure to set a value that is within the range of the power supply to be used.

Caution: Set the same value at addresses 000C1H and 010C1H when the boot swap operation is used.

1.3 User Option Byte (000C2H)

User Option Byte (000C2H) specifies the frequency of high-speed on-chip oscillator, threshold voltage of ports (V_{IL}), and LS / HS operation mode. The bits of User Option Byte (000C2H) are shown in Figure 3, and the setting considerations are shown in Table 5.

b7	b6	b5	b4	b3	b2	b1	b0
1	CMODE0	ITHL	0	FRQSEL [3:0]			

Bit Symbol	Function
FRQSEL [3:0]	Frequency of the high-speed on-chip oscillator 0000B: 24 MHz 0001B: 12 MHz 1000B: 32 MHz 1001B: 16 MHz 1010B: 8 MHz 1011B: 4 MHz 1101B: 1 MHz Other than above: Setting prohibited
ITHL	Threshold voltage of ports (V_{IL}) 0: The V_{IL} (MAX.) is: ・0.5 EV_{DD} (4.0 V ≤ EV_{DD} ≤ 5.5 V) ・0.4 EV_{DD} (2.7 V ≤ EV_{DD} < 4.0 V) ・0.3 EV_{DD} (1.8 V ≤ EV_{DD} < 2.7 V) 1: The V_{IL} (MAX.) is 0.2 EV_{DD}.
CMODE0	0: LS (low speed main) mode 1: HS (high speed main) mode

Figure 3. User Option Byte (000C2H)

Table 5. User Option Byte (000C2H) Setting Considerations

Bit Symbol	Setting Considerations
FRQSEL [3:0]	• Be sure to set any one of 0000B, 0001B, 1000B, 1001B, 1010B, 1011B, or 1101B. When using J-grade products (T_A = -40 to 85 °C) under the condition where V_{DD} (supply voltage) is 1.8 V to 2.7 V, be sure to set any one of 1010B (8 MHz), 1011B (4 MHz), or 1101B (1 MHz). Also, when using K-grade products (T_A = -40 to 125 °C), do not set to 1000B (32 MHz).
b4	• Be sure to set this bit to 0.
ITHL	• All the following ports are applicable. Applicable ports: P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147 However, when TTL input buffer is selected for these ports through the PIM0, PIM1, and PIM5 registers, the threshold voltage for these ports becomes TTL input. The setting of the ITHL bit is not applicable to any ports other than the above ports (*). (*): P20 to P27, P60 to P63, P121 to P124, P137
CMODE0	• Be sure to set 1 when the following use conditions are not satisfied. Conditions for setting this bit to 0: J-grade products are used and f_{CLK} (CPU / Peripheral hardware clock frequency) is 1 MHz to 8 MHz.
b7	• Be sure to set this bit to 1.

Caution: Set the same value at addresses 000C2H and 010C2H when the boot swap operation is used.

1.4 On-Chip Debug Option Byte (000C3H)

On-Chip Debug Option Byte (000C3H) specifies the operation when on-chip debugger is connected. The bits of On-Chip Debug Option Byte (000C3H) are shown in Figure 4, and the setting considerations are shown in Table 7.

b7	b6	b5	b4	b3	b2	b1	b0
OCDENSET	0	0	0	0	1	0	OCDERSD

Bit Symbol	Function
OCDERSD	Together with the OCDENSET bit, it controls the operation when an on-chip debugger is connected. Refer to Table 6.
OCDENSET	Together with the OCDERSD bit, it controls the operation when an on-chip debugger is connected. Refer to Table 6.

Figure 4. On-Chip Debug Option Byte (000C3H)

Table 6. Setting of OCDENSET and OCDERSD Bits

OCDENSET	OCDERSD	Function
0	0	Disables on-chip debug operation Note 1
0	1	Setting prohibited
1	0	Enables on-chip debugging. Erases data of flash memory in the case of failures in authenticating on-chip debug security ID. Notes 2, 3
1	1	Enables on-chip debugging. Does not erase data of flash memory in the case of failures in authenticating on-chip debug security ID. Notes 2, 3

Notes: 1. This setting disables connecting to an on-chip debugger. However, erasing / writing can be performed via a flash memory programmer.
2. The on-chip debug security ID written to the 10-byte area located in the address range 000C4H to 000CDH.
3. Both areas of code flash memory and data flash memory are targeted.

Table 7. On-Chip Debug Option Byte (000C3H) Setting Considerations

Bit Symbol	Setting Considerations
OCDERSD	• Do not set this bit to 1 when the OCDENSET bit is 0.
b6 to b1 Note	• Be sure to set these bits to 000010B.
OCDENSET	• Do not clear this bit to 0 when the OCDERSD bit is 1.

Note: When on-chip debug function is used, the value of bits 3 to 1 changes to any value other than 010B. Be sure to write these bits to 010B when writing.

Caution: Set the same value at addresses 000C3H and 010C3H when the boot swap operation is used.

2. Setting Range of Option Bytes

The value to be set to the Option Bytes of the RL78/F12 depends on the products to be used and use conditions (V_{DD} and f_{CLK}) (*). The setting range of the Option Bytes is shown in the Table 8.

(*). V_{DD}: Power supply voltage, f_{CLK}: CPU / Peripheral hardware clock frequency

Table 8. Setting Range of Option Bytes

Option Bytes		J-grade Products (T_A = -40 to 85 °C)		K-grade Products (T_A = -40 to 125 °C)
		[Conditions] V_{DD} = 1.8 V to 5.5 V, f_{CLK} = 1 MHz to 8 MHz	[Conditions] V_{DD} = 2.7 V to 5.5 V, f_{CLK} = 1 MHz to 32 MHz	[Conditions] V_{DD} = 2.7 V to 5.5 V, f_{CLK} = 1 MHz to 24 MHz
000C0H	WDSTBYON	0 or 1	same as on the left	same as on the left
	WDCS [2:0]	000B to 111B	same as on the left	same as on the left
	WDTON	0 or 1	same as on the left	same as on the left
	WINDOW [1:0]	01B, 10B, or 11B	same as on the left	same as on the left
	WDTINT	0 or 1	same as on the left	same as on the left
000C1H	LVIMDS [1:0] Note 1	01B, 10B, or 11B	same as on the left	same as on the left
	LVIS [1:0] Note 1	・LVIMDS=01B, VPOC=001B: 00B to 11B ・LVIMDS=01B, VPOC=010B: 00B to 11B ・LVIMDS=01B, VPOC=011B: 00B to 11B ・LVIMDS=10B, VPOC=001B: 00B, 01B, or 10B ・LVIMDS=10B, VPOC=010B: 00B, 01B, or 10B ・LVIMDS=10B, VPOC=011B: 00B, 01B, or 10B ・LVIMDS=11B, VPOC=001B: 00B to 11B ・LVIMDS=11B, VPOC=010B: 00B to 11B ・LVIMDS=11B, VPOC=011B: 00B to 11B	・LVIMDS=01B, VPOC=001B: 00B ・LVIMDS=01B, VPOC=010B: 00B ・LVIMDS=01B, VPOC=011B: 00B to 11B ・LVIMDS=10B, VPOC=011B: 00B, 01B, or 10B ・LVIMDS=11B, VPOC=001B: 00B ・LVIMDS=11B, VPOC=010B: 00B ・LVIMDS=11B, VPOC=011B: 00B to 11B	same as on the left
	VPOC [2:0] Note 1	・LVIMDS=01B: 001B, 010B, 011B, or 1xxB ・LVIMDS=10B: 001B, 010B, or 011B ・LVIMDS=11B: 001B, 010B, 011B, or 1xxB	・LVIMDS=01B: 001B, 010B, 011B, or 1xxB ・LVIMDS=10B: 011B ・LVIMDS=11B: 001B, 010B, 011B, or 1xxB	same as on the left
000C2H	FRQSEL [3:0]	1010B, 1011B, or 1101B	・CMODE0=1: 0000B, 0001B, 1000B,1001B, 1010B, 1011B, or 1101B ・CMODE0=0: 1010B, 1011B, or 1101B	0000B, 0001B, 1001B, 1010B, 1011B, or 1101B
	ITHL Note 2	0 or 1	same as on the left	same as on the left
	CMODE0	0 or 1	・f_{CLK} is less than 8 MHz: 0 or 1 ・f_{CLK} is greater than 8 MHz: 1	Fixed with 1
000C3H	OCDERSD	[OCDENSET, OCDERSD] bits: [0, 0], [1, 0], or [1, 1]	same as on the left	same as on the left
	OCDENSET			

Notes: 1. Select the value corresponding to the detection voltage range to be used.
2. When the ITHL bit is 0, V_{IL} (Input voltage, Low) depends on the supply voltage. For details, refer to the User's manual: Hardware.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb.20.19	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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