R8C/L38C and R8C/LA8A Groups

Differences between R8C/L38C and R8C/LA8A Groups

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1. Abstract

This document is reference material for identifying differences between the R8C/L38C Group and R8C/LA8A Group.

2. Introduction

This document applies to the following microcomputers (MCUs):

- MCUs: R8C/L38C Group, R8C/LA8A Group

3. Upward Compatibility of Functions

(1) Timer RJ for the R8C/LA8A Group is an upward compatibility of timer RA.
(2) Timer RH for the R8C/LA8A Group is an upward compatibility of timer RE.

4. Differences between Groups

4.1 Function and Specification Differences

Table 4.1 to Table 4.4 list differences in the functions and specifications. For more details and electrical characteristics, refer to the documents listed in 6. Reference Documents.

Table 4.1 Function and Specification Differences (1)

Item		R8C/L38C Group	R8C/LA8A Group
Flash Memory	ROM/RAM	• 48 KB/6 KB • 64 KB/8 KB • 96 KB/10 KB • 128 KB/10 KB	•16 KB/2 KB • 32 KB/2 KB • 48 KB/3.5 KB • 64 KB/3.5 KB
I/O Ports		I/O ports: 68 High current drive ports: 8	I/O ports: 72 High current drive ports: 10
Clock Generation Circuit	Peripheral function clocks	• f16 not included • fOCO40M included • fOCO20M not included • fC2 included • fC4 included • fC-TRH not included	• f16 included • fOCO40M not included • fOCO20M included • fC2 not included • fC4 not included • fC-TRH included
High-speed on-chip oscillator		• Clock frequency: approximately 40 MHz • Division ratio: Divide-by-2 to divide-by-9 (set to divide-by-8 or more when VCC is 1.8 to 2.7 V) • Adjustable frequency: 40 MHz, 36.864 MHz, and 32 MHz.	• Clock frequency: approximately 20 MHz • Division ratio: Divide-by-1 to divide-by-8 (set to divide-by-4 or more when VCC is 1.8 to 2.7 V) • Adjustable frequency: 20 MHz and 18.432 MHz.
Power Control	Exit wait mode (flash memory operates)	• Internal power stabilization time: 0 μs • Exit time for flash memory: System clock period × 1 cycle + 60 μs (max.)	• Internal power stabilization time: 100 μs • Exit time for flash memory: System clock period × 1 cycle
	Exit stop mode (flash memory operates)	• Exit time for flash memory: System clock period × 1 cycle + 60 μs (max.)	• Exit time for flash memory: System clock period × 1 cycle
	Power-off mode	• Perform processing to enter power-off mode when exit conditions are met: Enter power-off mode (1)	• Perform processing to enter power-off 0 mode when exit conditions are met: Do not enter power-off 0 mode (1)
	Power-off 2 mode	Not included	Included
Interrupts		• Number of interrupt sources: 40 • External interrupt input: 16 ($\overline{INT}$ × 8, key input × 8)	• Number of interrupt sources: 39 • External interrupt input: 16 ($\overline{INT}$ × 8, key input × 8)
Data Transfer Controller (DTC)		Included	Not included

Note:

1. R8C/L38C Group: When performing power-off mode enter processing while exit conditions for power-off mode are met (low pulse input to the $\overline{WKUP0}$ pin), the MCU exits power-off mode and executes the reset sequence immediately after it enters power-off mode.
   R8C/LA8A Group: When performing power-off 0 mode enter processing while exit conditions for power-off 0 mode are met (low pulse input to the $\overline{WKUP0}$ pin or the $\overline{WKUP1}$ pin), the MCU does not enter power-off 0 mode and program execution continues.

Table 4.2 Function and Specification Differences (2)

Item		R8C/L38C Group	R8C/LA8A Group
Timer RJ (timer RA)	Number of timers	1 (timer RA)	3 (timer RJ0, timer RJ1, and timer RJ2)
	Counter	8-bit timer with 8-bit prescaler	16-bit timer
	Module standby bit	Not included	Included
	Underflow cascade connection	Not included	Cascade connectable for timer RJ0, RJ1, and RJ2 sequentially.
Timer RB	Number of timers	1 (timer RB)	2 (timer RB0 and timer RB1)
	Module standby bit	Not included	Included
Timer RC	Pulse output forced cutoff signal	“L”	“L” or “H”
Timer RD		Included	Not included
Timer RH (timer RE)	Module standby bit	Not included	Included
	Alarm function	Not included	Included
	Specified second interrupt	Not included	Included
	Second adjustment function	Not included	Included
	Clock error correction function	Not included	Included
	Protect bit	Not included	Included
Timer RH (timer RE) (real-time clock mode)	TRHO output (TREO pin output)	Output of f2, fC, f4, 1 Hz, or f8	Output of f4, fC-TRH, f8, 1 Hz, f16, 64 Hz, or f32
	Counter	Date, month, and year cannot be counted	Date, month, and year (supporting leap years from 2000 to 2099) can be counted
Timer RH (timer RE) (output compare mode)	TRHO output (TREO pin output)	Output of f2, fC, f4, f8, or compare output	Output of f4, fC-TRH, f8, f16, f32, or compare output
	Count source	f4, f8, f32, or fC4	f8, f32, f128, f256, f512, f2048, f4096, or f8192
Timer RG		Included	Not included
Serial Interface	UART0	Module standby bit not included	Module standby bit included
	UART1	Included	Not included
	UART2	Module standby bit not included	Module standby bit included
Hardware LIN		Included	Not included

Table 4.3 Function and Specification Differences (3)

Item		R8C/L38C Group	R8C/LA8A Group
LCD Drive Control	LCD drive waveform	• Segment panel control waveform • Dot matrix panel control waveform	• Segment panel control waveform • Drive waveform of memory-type liquid crystal panel
	Segment output	Max. 48 pins	Max. 40 pins
	Common output	Max. 8 pins	Max. 4 pins
	LCD power supply	4 pins (dedicated pin)	3 pins (I/O port shared)
	Bias control	1/4 bias included	1/4 bias not included
	Interrupt according to the LCD display period	Not included	Included
	LCD display control	Blink or invert included	Blink or invert not included
	Internal voltage multiplier	Included	Not included
	Clock source division	Divide-by-128 not included	Divide-by-128 included
A/D Converter	Module standby bit	Not included	Included
	Gain amplifier	Not included	Included
	Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.3 V, ϕAD = 16 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 2.2 V, ϕAD = 5 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
	Analog input pins	16 (AN0 to AN15)	12 (AN0 to AN11)
	Timer used as A/D conversion trigger	Timer RD	Timer RH
	Internal temperature sensor	Not included	Included
D/A Converter		Included	Not included

Table 4.4 Function and Specification Differences (4)

Item		R8C/L38C Group	R8C/LA8A Group
Flash Memory	Program ROM (size per block)	4 KB/8 KB/16 KB/32 KB	4 KB/8 KB/16 KB
	Data flash	1 KB × 4 blocks	1 KB × 2 blocks
	BGO function	Included	Not included
	Rewrite control program executable area	When rewriting data flash area in EW0 mode: Executable on program ROM area	When rewriting data flash area in EW0 mode: RAM (The rewrite control program must be transferred before being executed.)
	Programming method	Byte units or word units	Byte units
	Suspend function	• Erase suspend included • Program suspend not included	• Erase suspend included • Program suspend included
	Programming and erasure endurance	• Program ROM: 1,000 times • Data flash: 10,000 times	• Program ROM: 10,000 times • Data flash: 10,000 times
	Block erase time	0.3 s	0.12 s
	Time delay from suspend request until suspend	5 ms + CPU clock × 3 cycles	0.25 ms + CPU clock × 3 cycles
	Programming and erasure voltage	2.7 to 5.5 V	1.8 to 5.5 V
Current Consumption		• Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) • Typ. 3.6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) • Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) • Typ. 2 μA (VCC = 3.0 V, stop mode) • Typ. 0.02 μA (VCC = 3.0 V, power-off mode)	• Typ. 4.7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) • Typ. 2.3 mA (VCC = 3.0 V, f(XIN) = 10 MHz) • Typ. 1.7 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) • Typ. 0.5 μA (VCC = 3.0 V, stop mode) • Typ. 1.5 μA (VCC = 3.0 V, power-off 2 mode, timer RH enabled) • Typ. 0.01 μA (VCC = 3.0 V, power-off 0 mode, timer RH disabled)

4.2 Pin Function Differences

Table 4.5 to Table 4.8 list differences in the I/O ports assigned to the peripheral function pins. For more details, refer to the documents listed in 6. Reference Documents.

Table 4.5 Pin Function Differences of R8C/L38A and R8C/LA8A Groups (1)

Pin Name	R8C/L38C Group	R8C/LA8A Group
$\overline{\text{WKUP1}}$	—	P7_0
XIN	P12_0	P9_0
XOUT	P12_1	P9_1
$\overline{\text{INT0}}$	P11_0, P3_0	P3_0, P0_3
$\overline{\text{INT1}}$	P11_1, P3_1	P3_1, P8_0
$\overline{\text{INT2}}$	P11_2, P3_2	P3_2, P8_7
$\overline{\text{INT3}}$	P11_3, P3_3	P3_3, P8_1
$\overline{\text{INT4}}$	P11_4, P3_4	P3_4, P1_4
$\overline{\text{INT5}}$	P11_5, P3_5	P3_5, P1_5
$\overline{\text{INT6}}$	P11_6, P3_6	P3_6, P1_6
$\overline{\text{INT7}}$	P11_7, P3_7	P3_7, P0_1
$\overline{\text{KI0}}$	P2_0	P0_2
$\overline{\text{KI1}}$	P2_1	P0_3
$\overline{\text{KI2}}$	P2_2	P0_4
$\overline{\text{KI3}}$	P2_3	P0_5
$\overline{\text{KI4}}$	P2_4	P0_6
$\overline{\text{KI5}}$	P2_5	P0_7
$\overline{\text{KI6}}$	P2_6	P1_2
$\overline{\text{KI7}}$	P2_7	P1_3
TRAIO	P11_4	—
TRAO	P11_5	—
TRBO	P11_6	—
TRB0O	—	P8_7, P7_6, P6_6
TRB1O	—	P7_5, P6_5
TRCCLK	P4_3	P0_1
TRCIOA	P4_4	P0_0
TRCIOB	P4_7, P4_6, P4_5	P6_7, P6_6, P6_5
TRCIOC	P4_6	P6_6
TRCIOD	P4_7	P6_5

The symbol "—" indicates there is no pin for the peripheral function.

Table 4.6 Pin Function Differences of R8C/L38A and R8C/LA8A Groups (2)

Pin Name	R8C/L38C Group	R8C/LA8A Group
TRCTRG	P4_4, P4_3, P3_7	P0_2, P0_1, P0_0
TRDCLK	P6_0	—
TRDIOA0	P6_0	—
TRDIOB0	P6_1	—
TRDIOC0	P6_2	—
TRDIOD0	P6_3	—
TRDIOA1	P6_4	—
TRDIOB1	P6_5	—
TRDIOC1	P6_6	—
TRDIOD1	P6_7	—
TREO	P11_7	—
TRHO	—	P0_7
TRJ0IO	—	P8_3, P6_2
TRJ0O	—	P7_2
TRJ1IO	—	P8_2, P6_1
TRJ1O	—	P7_1
TRJ2IO	—	P6_0
TRJ2O	—	P7_0
CLK0	P13_3	P8_4
TXD0	P13_1	P8_5
RXD0	P13_2, P11_4	P8_6
CLK1	P4_2	—
TXD1	P4_0	—
RXD1	P4_1	—
CLK2	P11_0	P8_4, P7_0
TXD2	P11_2, P11_1	P8_5, P7_2, P7_1
RXD2	P11_2, P11_1	P8_6, P7_2, P7_1
SCL2	P11_2, P11_1	P8_6, P7_2, P7_1
SDA2	P11_2, P11_1	P8_5, P7_2, P7_1
$\overline{\text{CTS2}}$	P11_3	P8_7, P7_3
$\overline{\text{RTS2}}$	P11_3	P8_7, P7_3

The symbol "—" indicates there is no pin for the peripheral function.

Table 4.7 Pin Function Differences of R8C/L38A and R8C/LA8A Groups (3)

Pin Name	R8C/L38C Group	R8C/LA8A Group
SSI	P11_1	P8_1, P6_2
$\overline{SCS}$	P11_3	P8_0, P6_1
SSCK	P11_0	P8_2, P6_3
SSO	P11_2	P8_3, P6_4
SCL	P11_0	P8_2, P6_3
SDA	P11_2	P8_3, P6_4
AN0	P13_0	P7_4
AN1	P13_1	P7_5
AN2	P13_2	P7_6
AN3	P13_3	P6_0
AN4	P0_0	P6_1
AN5	P0_1	P6_2
AN6	P0_2	P6_3
AN7	P0_3	P6_4
AN8	P0_4	P6_5
AN9	P0_5	P6_6
AN10	P0_6	P6_7
AN11	P0_7	P0_0
AN12	P1_0	—
AN13	P1_1	—
AN14	P1_2	—
AN15	P1_3	—
$\overline{ADTRG}$	P11_7, P3_7	P0_1
DA0	P13_0	—
DA1	P13_1	—
IVCMP1	P11_1	P8_0
IVREF1	P11_0	P6_5
IVCMP3	P11_3	P8_1
IVREF3	P11_2	P6_6
COMEXP	—	P4_7

The symbol "—" indicates there is no pin for the peripheral function.

Table 4.8 Pin Function Differences of R8C/L38A and R8C/LA8A Groups (4)

Pin Name	R8C/L38C Group	R8C/LA8A Group
SEG12	—	P1_4
SEG13	—	P1_5
SEG14	—	P1_6
SEG15	—	P1_7
SEG44	P6_0	—
SEG45	P6_1	—
SEG46	P6_2	—
SEG47	P6_3	—
SEG48	P6_4	—
SEG49	P6_5	—
SEG50	P6_6	—
SEG51	P6_7	—
SEG52	P7_0	—
SEG53	P7_1	—
SEG54	P7_2	—
SEG55	P7_3	—
COM0	P7_7	P5_3
COM1	P7_6	P5_2
COM2	P7_5	P5_1
COM3	P7_4	P5_0
COM4	P7_3	—
COM5	P7_2	—
COM6	P7_1	—
COM7	P7_0	—
VL1	(Note 1)	P5_4
VL2	(Note 1)	P5_5
VL3	(Note 1)	P5_6
VL4	(Note 1)	—
CL1	P12_2	—
CL2	P12_3	—

Note:
1. These pins are dedicated pins.

4.3 SFR Differences

Table 4.9 to Table 4.14 list differences in the SFRs. Changes from the R8C/L38C Group are shown in the remarks. For more details, refer to the documents listed in 6. Reference Documents.

Table 4.9 SFR Differences (1)

R8C/L38C Group	R8C/LA8A Group	Remarks
PD1	PD1	Bits 4 to 7 added
P1	P1	Bits 4 to 7 added
PD7	PD7	Bit 7 deleted
P7	P7	Bit 7 deleted
—	PD5	
—	P5	
—	PD8	
—	P8	
—	PD9	
—	P9	
PD11	—	
P11	—	
PD12	—	
P12	—	
PD13	—	
P13	—	
TRASR	TRJSR	• Register name changed • Function(s) changed in bits 0 and 1 • Bits 4 and 5 added
TRBRCSR	—	
—	TRBSR	
TRCPSR0	TRCPSR0	• Function(s) changed in bit 0 • Bits 2 and 3 added
TRCPSR1	TRCPSR1	• Bit 2 added • Bit 4 deleted
TRDPSR0	—	
TRDPSR1	—	
TRGPSR	—	
U0SR	U0SR	Bits 1 and 5 added Function(s) changed in bits 2 and 3
U1SR	—	
U2SR0	U2SR0	Function(s) changed in bits 0, 1, 4 and 5
U2SR1	U2SR1	Function(s) added to bits 1 and 5
SSUIICSR	SSUIICSR	Bits 4 to 7 added
KISR	—	

The symbol "—" indicates there is no SFR.

Table 4.10 SFR Differences (2)

R8C/L38C Group	R8C/LA8A Group	Remarks
—	P8PUR	
—	P9PUR	
P11PUR	—	
P12PUR	—	
P13PUR	—	
—	P7DRR	
—	P8DRR	
P11DRR	—	
VLT2	VLT2	• Function(s) changed in bits 0 to 3 • Bits 4 to 7 deleted
CM0	CM0	Bit 0 added
CM1	CM1	Function(s) added to bit 0
CM3	CM3	Function(s) added to bits 6 and 7
FRA1	FRC0	Register name changed
FRA2	FRA2	Function(s) changed in bits 0 to 2
FRA3	FRC1	Register name changed
FRA4	—	
—	FR18S0	
FRA5	—	
—	FR18S1	
FRA6	—	
FRA7	—	
POMCR0	POMCR0	• Reset value is different • Bit 1 added
TRD0IC	—	
TRD1IC	—	
TREIC	TRHIC	Register name changed Function(s) changed in bit 3
S1TIC	—	
S1RIC	—	
TRAIC	TRJ0IC	Register name changed
TRBIC	TRB0IC	Register name changed
—	TRB1IC	
—	TRJ1IC	
—	TRJ2IC	
—	LCDIC	
TRGIC	—	
DTCTL	—	
DTCEN0 to DTCEN6	—	
DTCD0 to DTCD23	—	

The symbol "—" indicates there is no SFR.

Table 4.11 SFR Differences (3)

R8C/L38C Group	R8C/LA8A Group	Remarks
TRACR	TRJ0CR	Allocation address is different
TRAIOC	TRJ0IOC	• Allocation address is different • Bit 3 deleted
TRAMR	TRJ0MR	• Allocation address is different • Bit 3 added • Function(s) added to bits 4 to 6
—	TRJ0ISR	
TRAPRE	—	
TRA	—	
—	TRJ0	
—	TRJ1CR	
—	TRJ1IOC	
—	TRJ1MR	
—	TRJ1ISR	
—	TRJ1	
—	TRJ2CR	
—	TRJ2IOC	
—	TRJ2MR	
—	TRJ2ISR	
—	TRJ2	
—	MSTCR1	
TRBCR	TRB0CR	Register name changed
TRBOCR	TRB0OCR	Register name changed
TRBIOC	TRB0IOC	Register name changed
TRBMR	TRB0MR	Register name changed
TRBPRE	TRB0PRE	Register name changed
TRBSC	TRB0SC	Register name changed
TRBPR	TRB0PR	Register name changed
—	TRB1CR	
—	TRB1OCR	
—	TRB1IOC	
—	TRB1MR	
—	TRB1PRE	
—	TRB1SC	
—	TRB1PR	
MSTCR	MSTCR0	• Register name changed • Bits 1, 2, and 7 added • Function(s) changed in bit 4 • Bit 6 deleted
TRCCR1	TRCCR1	Function(s) changed in bits 4 to 6
TRCOER	TRCOER	Function(s) changed in bit 7

The symbol "—" indicates there is no SFR.

Table 4.12 SFR Differences (4)

R8C/L38C Group	R8C/LA8A Group	Remarks
TRDECR	—	
TRDADCR	—	
TRDSTR	—	
TRDMR	—	
TRDPMR	—	
TRDFCR	—	
TRDOER1	—	
TRDOER2	—	
TRDOCR	—	
TRDDF0	—	
TRDDF1	—	
TRDCR0	—	
TRDIORA0	—	
TRDIORC0	—	
TRDSR0	—	
TRDIER0	—	
TRDPOCR0	—	
TRD0	—	
TRDGRA0	—	
TRDGRB0	—	
TRDGRC0	—	
TRDGRD0	—	
TRDCR1	—	
TRDIORA1	—	
TRDIORC1	—	
TRDSR1	—	
TRDIER1	—	
TRDPOCR1	—	
TRD1	—	
TRDGRA1	—	
TRDGRB1	—	
TRDGRC1	—	
TRDGRD1	—	
TRESEC	TRHSEC	• Register name changed • Allocation address is different • Function(s) added to bit 7
TREMIN	TRHMIN	• Register name changed • Allocation address is different • Function(s) changed in bit 7

The symbol "—" indicates there is no SFR.

Table 4.13 SFR Differences (5)

R8C/L38C Group	R8C/LA8A Group	Remarks
TREHR	TRHHR	• Register name changed • Reset value is different • Allocation address is different • Bit 7 deleted
TREWK	TRHWK	• Register name changed • Reset value is different • Allocation address is different • Bit 7 deleted
—	TRHDY	
—	TRHMON	
—	TRHYR	
TRECR1	TRHCR	• Register name changed • Reset value is different • Allocation address is different • Bit 0 added • Function(s) changed in bits 1 to 3 • Symbol names changed in bits 4, 6, and 7
TRECR2	TRHIER	• Register name changed • Bit names and functions changed in bits 0 and 1 in output compare mode • Allocation address is different • Function(s) changed in bits 6 and 7
TRECSR	TRHCSR	• Register name changed • Reset value is different • Allocation address is different • Function(s) changed in bits 0 to 3 • Function(s) added to bits 4 to 6 • Bit 7 added
—	TRHADJ	
—	TRHIFR	
—	TRHAMN	
—	TRHAHR	
—	TRHAWK	
—	TRHPRC	
—	TRHICR	
TRGMR	—	
TRGCNTC	—	
TRGCR	—	
TRGIER	—	
TRGSR	—	
TRGIOR	—	
TRG	—	
TRGGRA	—	
TRGGRB	—	
TRGGRC	—	
TRGGRD	—	

The symbol "—" indicates there is no SFR.

Table 4.14 SFR Differences (6)

R8C/L38C Group	R8C/LA8A Group	Remarks
U1MR	—	
U1BRG	—	
U1TB	—	
U1C0	—	
U1C1	—	
U1RB	—	
LINCR2	—	
LINCR	—	
LINST	—	
ADMOD	ADMOD	Function(s) changed in bits 6 and 7
ADINSEL	ADINSEL	Function(s) changed in bits 6 and 7
ADCON1	ADCON1	Function(s) changed in bit 0
—	ADCON2	
DA0	—	
DA1	—	
DACON	—	
LCR0	LCR0	• Function(s) changed in bits 0 and 1 • Bits 2, 3, and 5 deleted • Function(s) changed in bit 4
LCR1	—	
LCR2	LCR2	Register function(s) changed
LCR3	LCR3	• Function(s) added to bits 0 to 2 • Function(s) changed in bits 6 and 7
—	LCR4	
LSE4	LSE4	Function(s) changed in bit 7
LSE5	LSE5	• Function(s) changed in bits 0 to 6 • Bit 7 deleted
LSE6	—	
LSE7	—	
LRA40L to LRA95L	—	
LRA0H to LRA95H	—	
FST	FST	Bit 3 added
FMR0	FMR0	Bit 0 deleted
FMR1	FMR1	• Reset value is different • Bits 6 and 7 deleted
FMR2	FMR2	Function(s) changed in bits 0 and 1

The symbol "—" indicates there is no SFR.

4.4 Interrupt Vector Differences

Table 4.15 lists differences in the relocatable vector table. For more details, refer to the documents listed in 6. Reference Documents.

Table 4.15 Relocatable Vector Table Differences

Software Interrupt Number	Interrupt Source of R8C/L38C Group	Interrupt Source of R8C/LA8A Group
8	Timer RD0	—
9	Timer RD1	—
10	Timer RE	Timer RH
19	UART1 transmission	—
20	UART1 reception	—
22	Timer RA	Timer RJ0
23	—	Timer RB1
24	Timer RB	Timer RB0
27	—	Timer RJ1
28	—	Timer RJ2
42	—	LCD
43	Timer RG	—

5. Notes

Each product has different oscillation circuit constants of XIN-XOUT, XCIN-XCOUT. Therefore, contact an oscillator manufacturer when selecting an oscillator and oscillation circuit constants so that a stable operation clock can be obtained on the user system and conditions for mass-production. Be careful especially when the voltage and temperature range is wide. The wiring pattern of the feedback resistor, damping resistor, and the load capacity should be considered in advance when designing a circuit.

In addition, although compatibility in characteristics is fully considered when designing each device, actual values such as operating margin, A/D conversion accuracy, noise immunity, noise radiation may be different within the range of electrical characteristics due to different manufacturing processes. Therefore, perform sufficient system evaluations for each individual product before starting mass production.

6. Reference Documents

R8C/L38C Group User's Manual: Hardware Rev.1.00
R8C/LA8A Group User's Manual: Hardware Rev.1.01
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

7. Website and Support

Renesas Electronics website
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Revision History	R8C/L38C and LA8A Groups Differences between R8C/L38C and R8C/LA8A Groups

Rev.	Date	Description	
		Page	Summary
1.00	Feb 18, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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