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R8C/38C Group

Timer RG Phase Counting Mode

1. Abstract

This document describes the setting method and an application example for a two-phase pulse count (count both edges of a two-phase pulse) using the R8C/38C Group's timer RG phase counting mode.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU : R8C/38C Group

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the sample program described in this application note.

3. Application Example

3.1 Program Outline

Two-pulse signals with the phase difference are input to pins TRGCLKA and TRGCLKB, and both edges are counted (increment or decrement).

Settings

- The TRG register is clear disabled.
- The digital filter is not used for pins TRGCLKA and TRGCLKB.
- The timer RG interrupt is disabled.
- Table 3.1 lists count conditions of bits CNTEN0 to CNTEN7.

Figure 3.1 shows an Operating Example and Table 3.2 lists a Pins and Their Functions.

Table 3.1 Increment/Decrement Conditions for the TRG Register

TRGCLKB pin	↑	High	↓	Low	High	↓	Low	↑
TRGCLKA pin	Low	↑	High	↓	↓	Low	↑	High
Bits CNTEN7 to CNTEN0 in the TRGCNTC register	CNTEN7	CNTEN6	CNTEN5	CNTEN4	CNTEN3	CNTEN2	CNTEN1	CNTEN0
Value	1	1	1	1	1	1	1	1
Increment or decrement	+1	+1	+1	+1	-1	-1	-1	-1

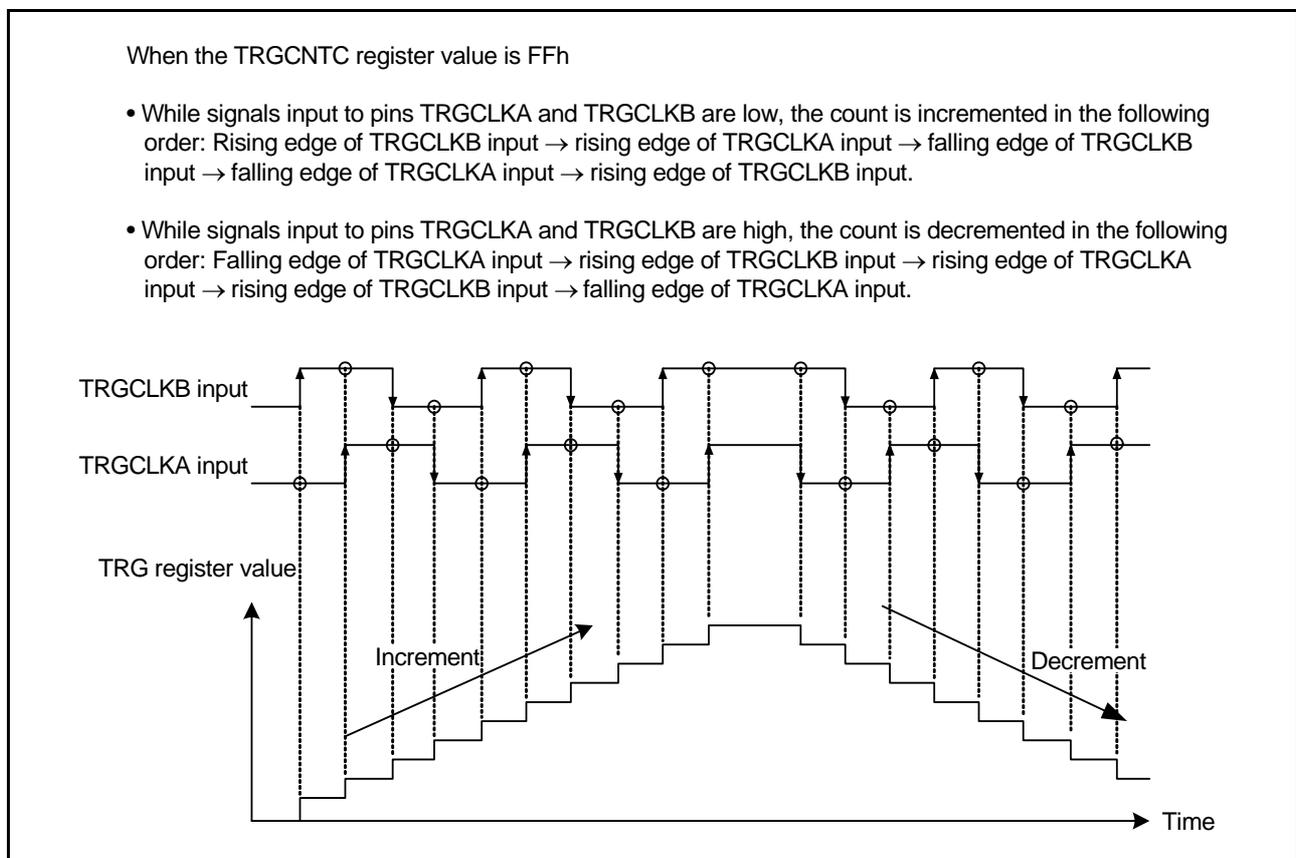


Figure 3.1 Operating Example

Table 3.2 Pins and Their Functions

Pin Name	I/O	Function
P3_0/TRGCLKA	Input	A-phase input
P3_2/TRGCLKB	Input	B-phase input

3.2 Memory

Table 3.3 Memory

Memory	Size	Remarks
ROM	131 bytes	In the rej05b1162_src.c module
RAM	0 bytes	In the rej05b1162_src.c module
Maximum user stack	9 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.

The above applies to the following conditions:

- C compiler: M16C/60, 30, 20, 10, and Tiny, and R8C/Tiny Series Compiler V.5.45 Release 00
- Compile option: -c -finfo -dir "\$(CONFIGDIR)" -R8C

4. Software Outline

This section shows the setting procedures and values to set the example described in section 3. **Application Example.** Refer to the latest **R8C/38C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the hyphen represents reserved bits or bits that have nothing assigned.

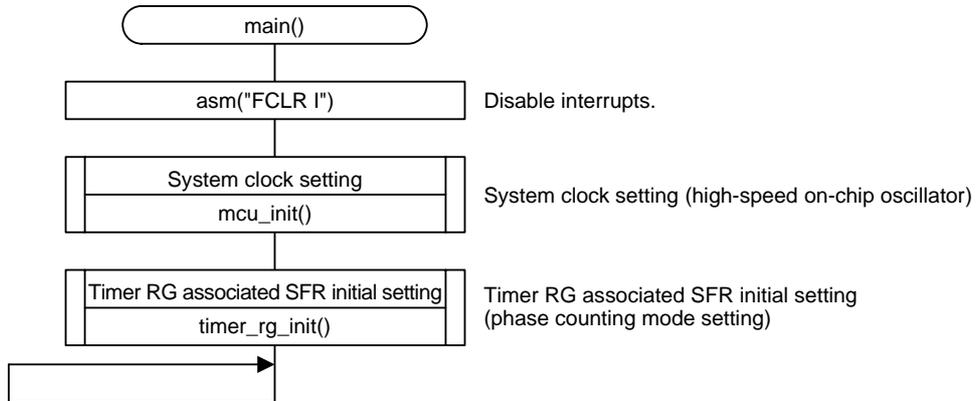
4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

Declaration	void timer_rg_init(void)		
Outline	Timer RG associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The SFR register is initialized to use timer RG in phase counting mode.		

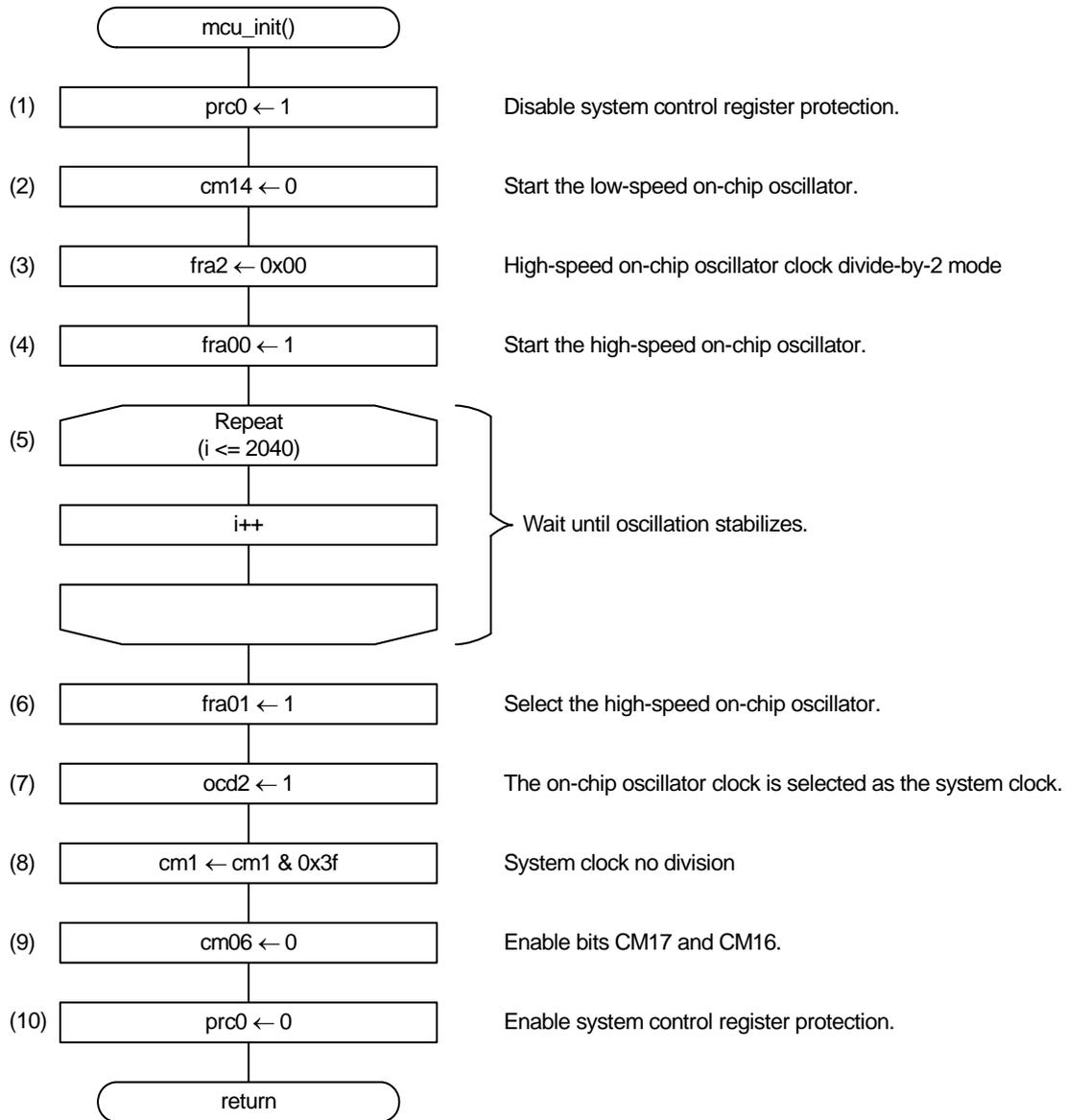
4.2 Main Function

- Flowchart



4.3 System Clock Setting

• Flowchart



• Register Settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division clock for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

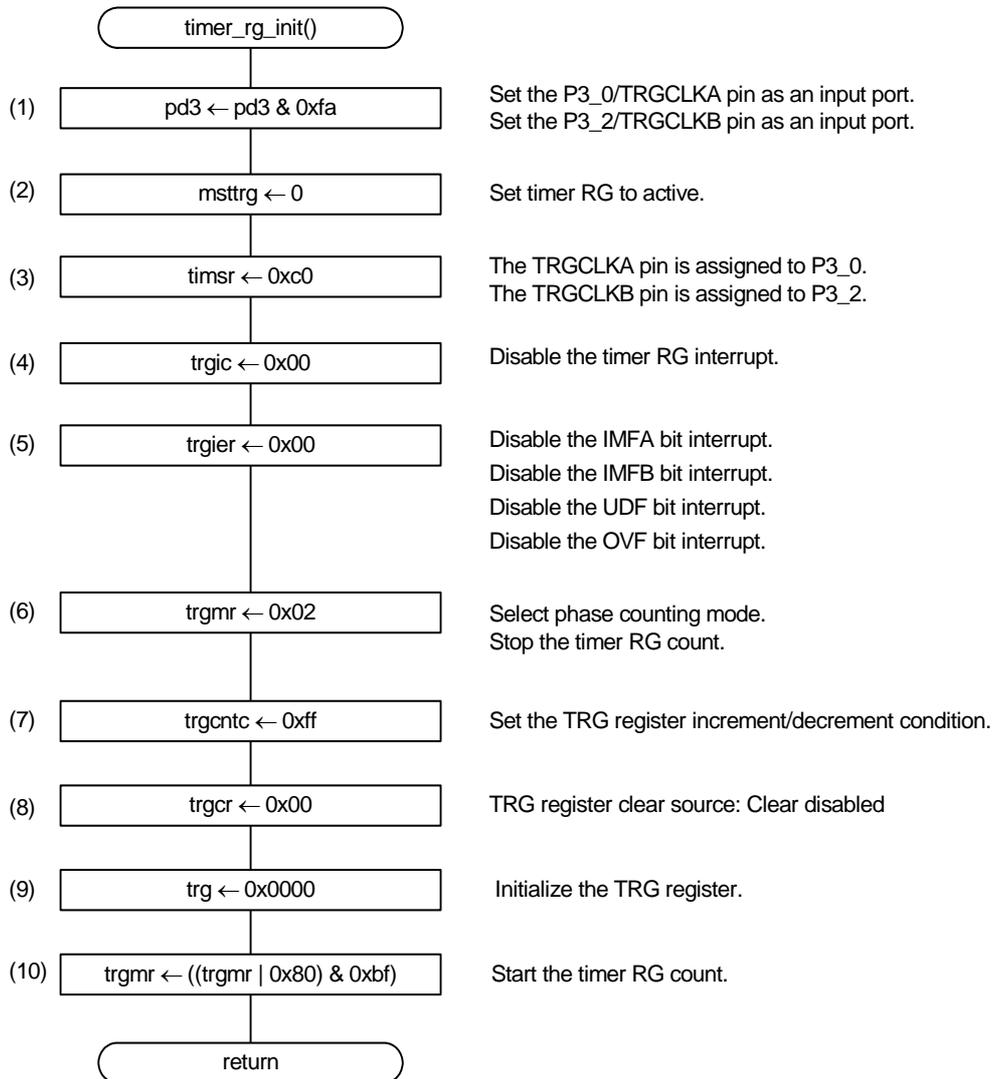
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write Disabled	R/W

4.4 Timer RG Associated SFR Initial Setting

• Flowchart



• Register Settings

(1) Set pins P3_0/TRGCLKA and P3_2/TRGCLKB as input ports.

Port P3 Direction Register (PD3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	x	x	x	x	0	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD3_0	Port P3_0 direction bit	0: Input mode (functions as an input port)	R/W
b2	PD3_2	Port P3_2 direction bit	0: Input mode (functions as an input port)	R/W

(2) Set timer RG to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	x	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	MSTTRG	Timer RG standby bit	0: Active	R/W

(3) Set the timer pin select register.

Timer Pin Select Register (TIMSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	1	x	x	—	x	—	x

Bit	Symbol	Bit Name	Function	R/W
b6	TRGCLKASEL	TRGCLKA pin select bit	1: P3_0 pin assigned	R/W
b7	TRGCLKBSEL	TRGCLKB pin select bit	1: P3_2 pin assigned	R/W

(4) Disable the timer RG interrupt.

Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(5) Disable all interrupt sources to timer RG.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA bit disabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB bit disabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF bit disabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF bit disabled	R/W

(6) Set the TRGMR register.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	—	x	x	x	x	1	x

Bit	Symbol	Bit Name	Function	R/W
b1	MDF	Phase counting mode select bit	1: Phase counting mode	R/W
b7	TSTART	TRG count start bit	0: Count stops	R/W

(7) Set the timer RG count control register.

Timer RG Count Control Register (TRGCNTC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	CNTEN0	Counter enable bit 0	1: Decrement When TRGCLKA input is high and at the rising edge of TRGCLKB input	R/W
b1	CNTEN1	Counter enable bit 1	1: Decrement When TRGCLKB input is low and at the rising edge of TRGCLKA input	R/W
b2	CNTEN2	Counter enable bit 2	1: Decrement When TRGCLKA input is low and at the falling edge of TRGCLKB input	R/W
b3	CNTEN3	Counter enable bit 3	1: Decrement When TRGCLKB input is high and at the falling edge of TRGCLKA input	R/W
b4	CNTEN4	Counter enable bit 4	1: Increment When TRGCLKB input is low and at the falling edge of TRGCLKA input	R/W
b5	CNTEN5	Counter enable bit 5	1: Increment When TRGCLKA input is high and at the falling edge of TRGCLKB input	R/W
b6	CNTEN6	Counter enable bit 6	1: Increment When TRGCLKB input is high and at the rising edge of TRGCLKA input	R/W
b7	CNTEN7	Counter enable bit 7	1: Increment When TRGCLKA input is low and at the rising edge of TRGCLKB input	R/W

(8) Disable the timer RG clear source.

Timer RG Control Register (TRGCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	0	0	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 0: Clear disabled	R/W
b6	CCLR1			R/W

(9) Initialize the timer RG counter to 0000h.

Timer RG Counter (TRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	In phase counting mode, count operation is increment/decrement.	0000h to FFFFh	R/W

(10) Start the timer RG counter.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	—	×	×	×	×	×	

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRG count start bit	1: Count starts	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

Hardware Manual

R8C/38C Group Hardware Manual Rev.0.10

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REVISION HISTORY	R8C/38C Group Timer RG Phase Counting Mode
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