

ISL72991RH

PSpice Simulation Results

Abstract

The ISL72991RH PSpice model is a nominal model of the ISL72991RH low dropout adjustable negative regulator. It simulates the functionality and the typical parametric performance of selected datasheet specification parameters.

The first section of this document provides a brief explanation of using the model to generate a general function test simulation. The simulation shows the functionality of ON/OFF control.

The second section shows PSpice simulation results compared to characterization test results using the ISL72991RHEVAL2Z evaluation board.

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Related Literature

For a full list of related documents, visit our website:

- [ISL72991RH](#) device page

1. PSpice General Functional Test Simulation

The simulation shown in [Figure 4](#) shows the ISL72991RH PSpice model functionality for basic on/off control.

1.1 ISL72991RH.LIB and ISL72991RH.OLB PSpice Files

The PSpice ISL72991RH.LIB and ISL72991RH.OLB files can be downloaded from the Renesas website at the ISL72991RH device pages under the **Download** tab. The file path to the ISL72991RH.OLB sub-circuit [Figure 1](#) must be added to the Cadence parts placement tool. It can then be used in simulation schematics. [Figure 2.](#) shows the folder structure of the ISL72991RH_Rev0.opj file. Individual simulation set-ups are in the [.isl72991rh_rev0.dsn](#) highlighted file.

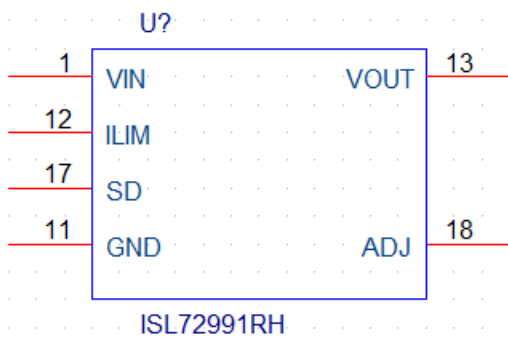


Figure 1. ISL72991RH Sub-Circuit (ISL72991RH.OLB)

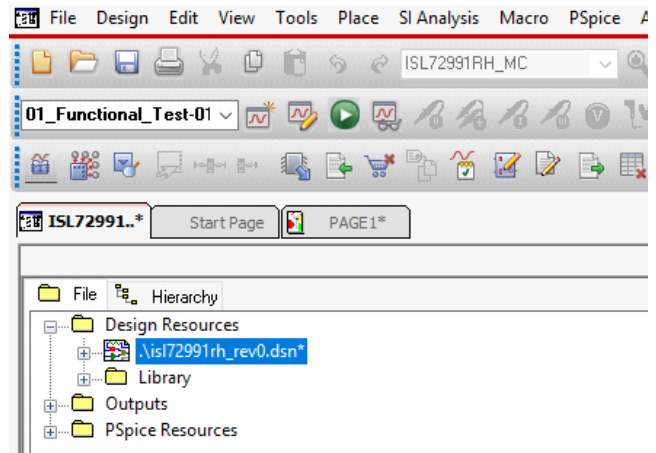


Figure 2. ISL72991RH_Rev0.opj

1.2 Functional Simulation Schematic

Figure 3 shows the PSpice simulation schematic used for the functional turn-off to turn-on simulation test.

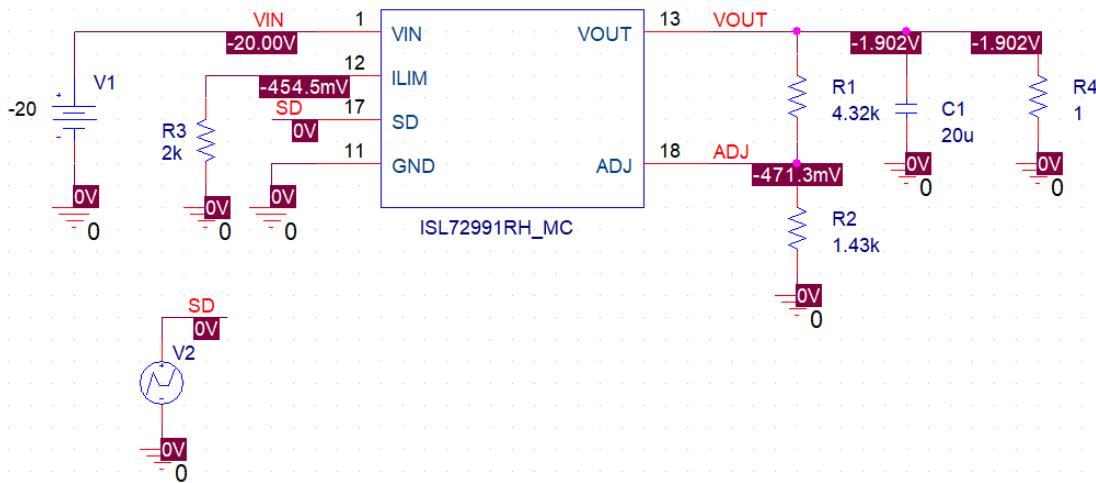


Figure 3. ISL72991RH PSpice General Functional Test Schematic

1.3 Functional Simulation Results

Figure 4 shows the simulation result for the functional test of the ISL72991 using the SD pin input; the SD input (red trace) and output current (green trace) vs time are shown.

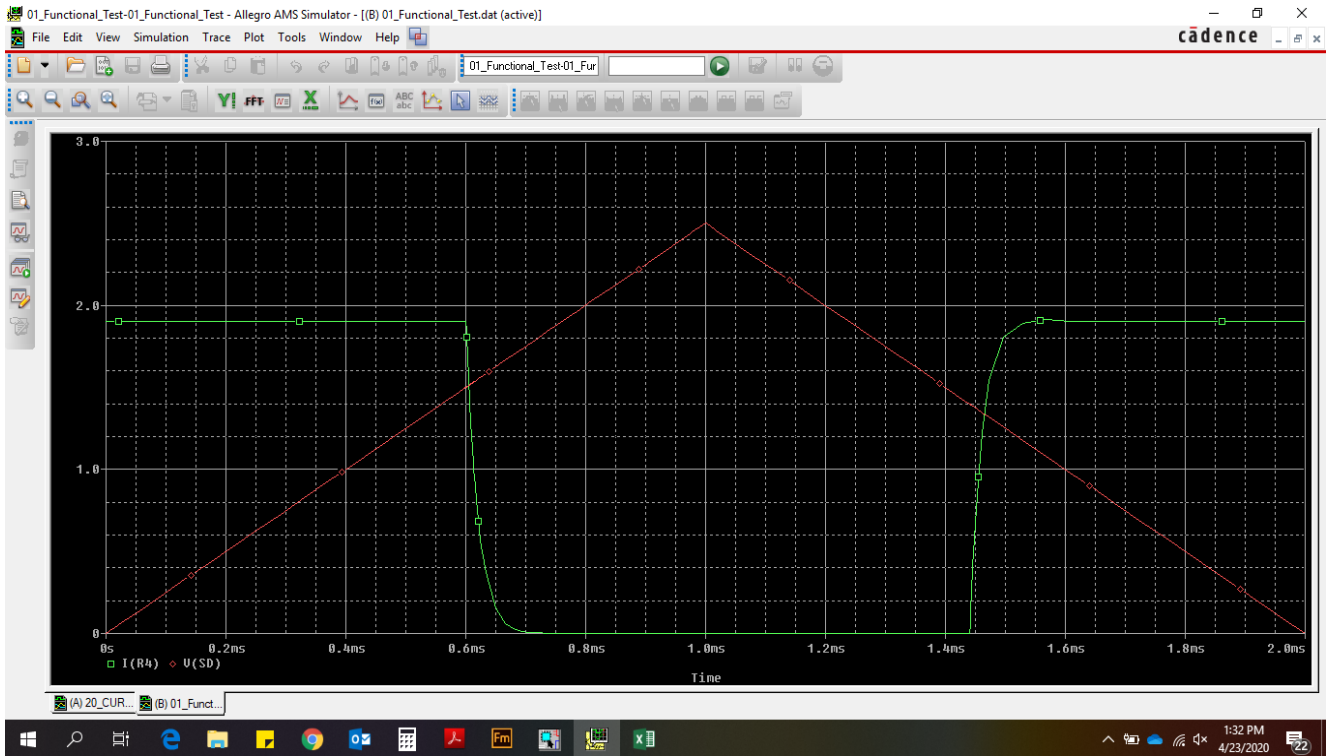


Figure 4. ISL72991RH PSpice General Functional Turn-Off/Turn-On Simulation Results

2. PSpice Simulation Results Versus Characterization Test Results

The ISL72991RH PSpice model was designed to reflect typical parametric performance in the ISL72991RH datasheet. This section provides a comparison between the PSpice simulation results and actual device

characterization test results for a few parameters. The graphs on the left are the PSpice simulation result and the graphs on the right are the device characterization results, for ease of comparison.

2.1 Test Circuits for Functional and Parametric Performance

DC Sweep VIN from -3.5 to -30, Plot VADJ to show what VREF value is set to internally.

PARAMETERS:
VIN = -3.5

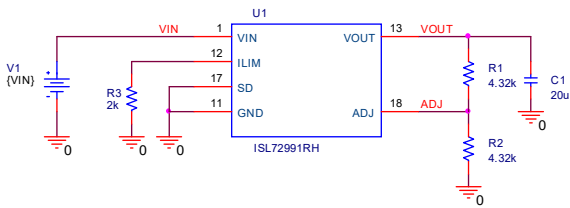


Figure 5. V_{REF} vs $-V_{IN}$ PSpice Circuit

DC Sweep of IOUT from 100mA to 800mA. Plot (VIN-VOUT).

PARAMETERS:
IOUT = 100m

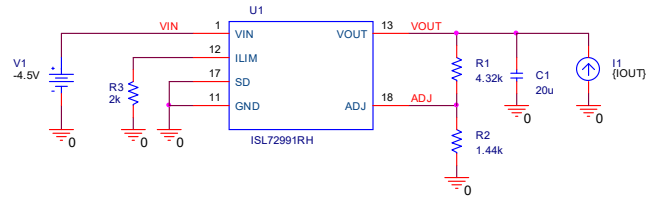


Figure 6. Dropout Voltage vs Output Current PSpice Circuit

DC Simulation. Vary RILIM from 2k to 10k. Observe short circuit current.

PARAMETERS:
RILIM = 2k

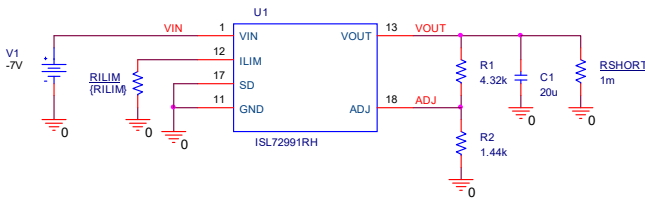


Figure 7. Short-Circuit Current Limiting PSpice Circuit

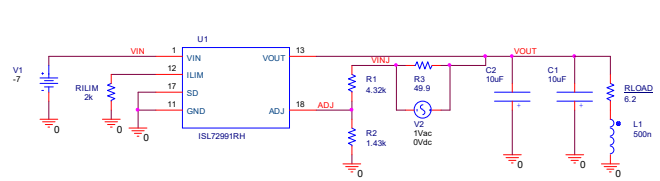


Figure 8. Bode PSpice Circuit

2.2 Functional and Parametric Performance Simulation to Silicon Comparison

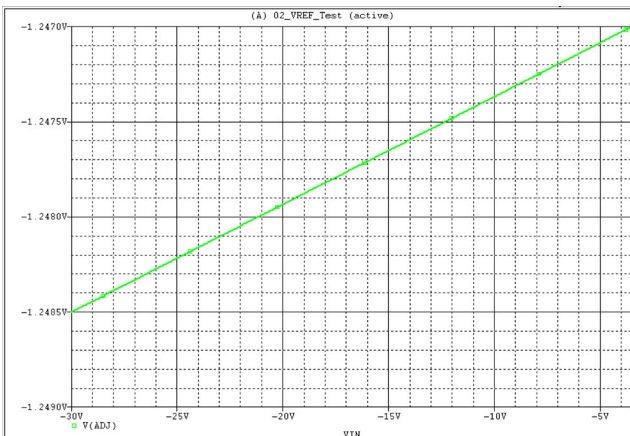


Figure 9. V_{REF} vs $-V_{IN}$ (PSpice Results)

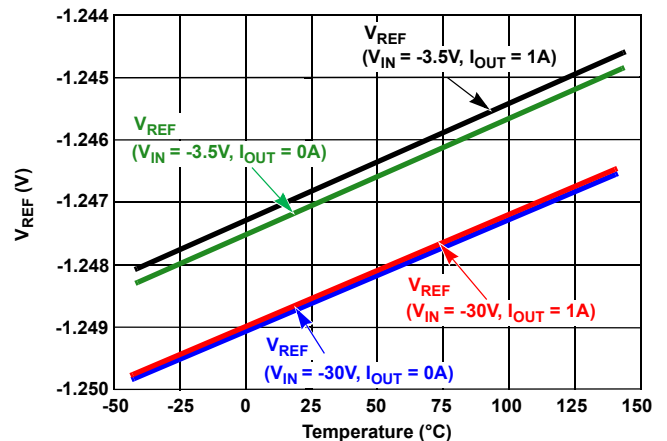


Figure 10. V_{REF} vs V_{IN} and Temperature (Characterization Results)

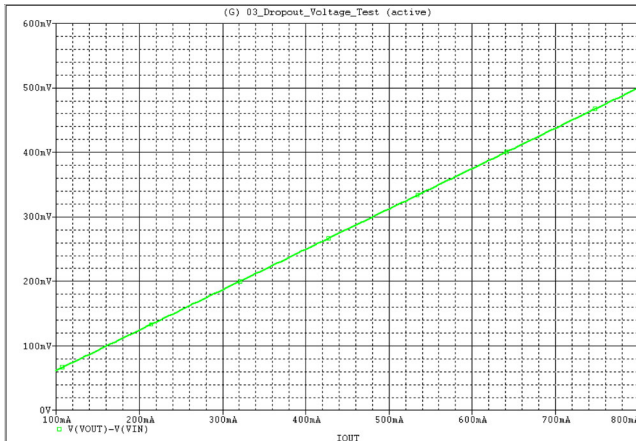


Figure 11. Dropout Voltage vs Output Current (PSpice Results)

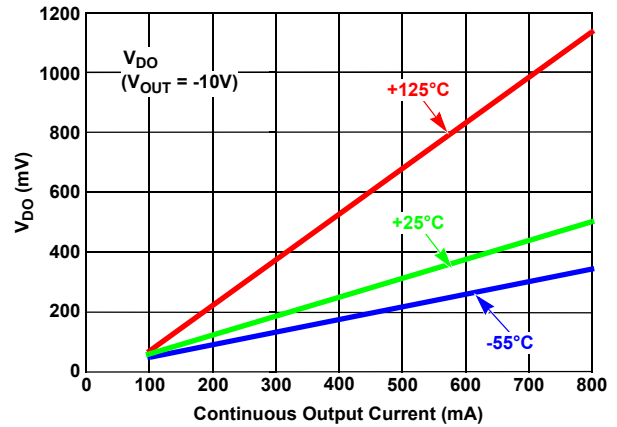


Figure 12. Dropout Voltage vs Output Current (Characterization Results)

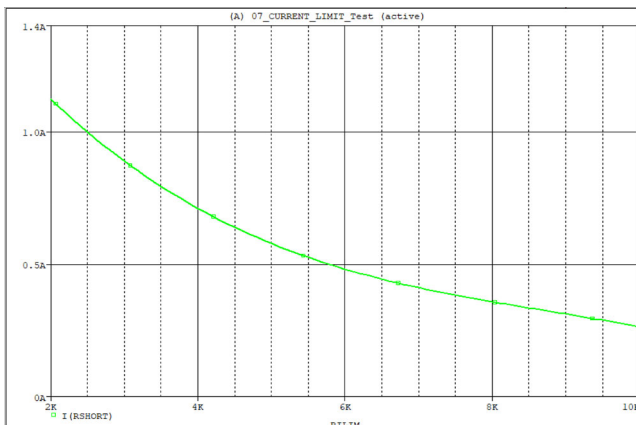


Figure 13. $I_{SC} -7V_{IN}, -5V_{OUT}$ (PSpice Results)

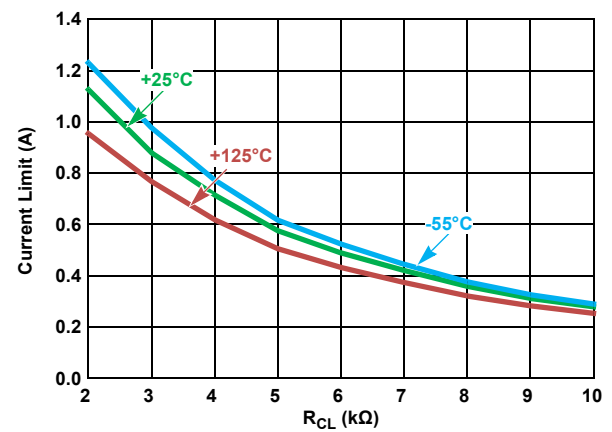


Figure 14. $I_{SC} -7V_{IN}, -5V_{OUT}$ (Characterization Results)

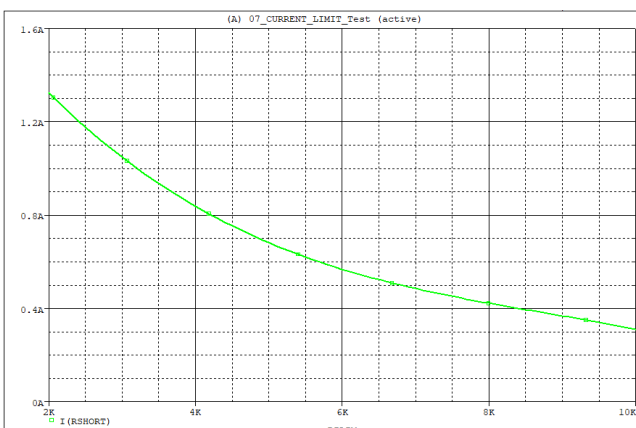


Figure 15. $I_{SC} -12V_{IN}, -5V_{OUT}$ (PSpice Results)

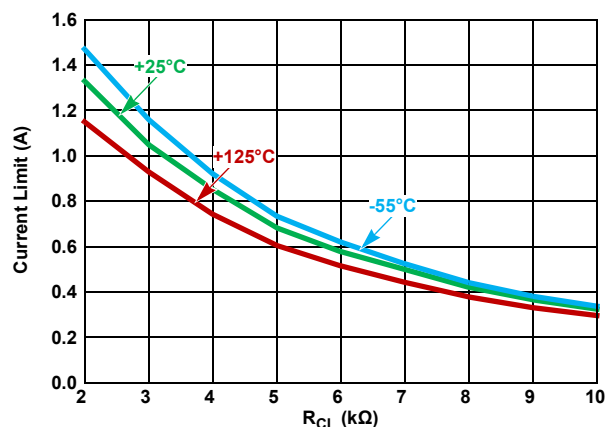


Figure 16. $I_{SC} -12V_{IN}, -5V_{OUT}$ (Characterization Results)

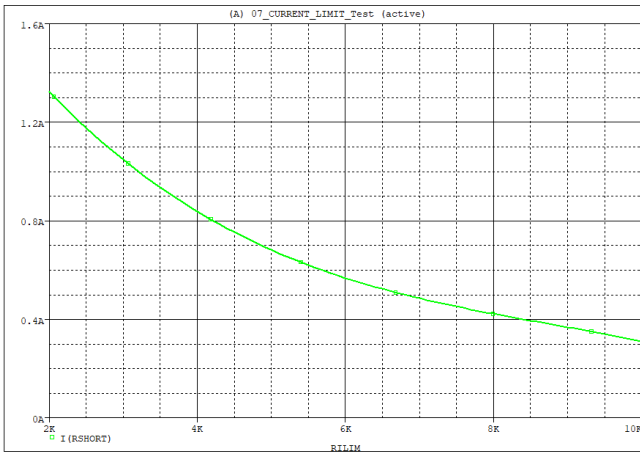


Figure 17. $I_{SC} -12V_{IN}, -10V_{OUT}$ (PSpice Results)

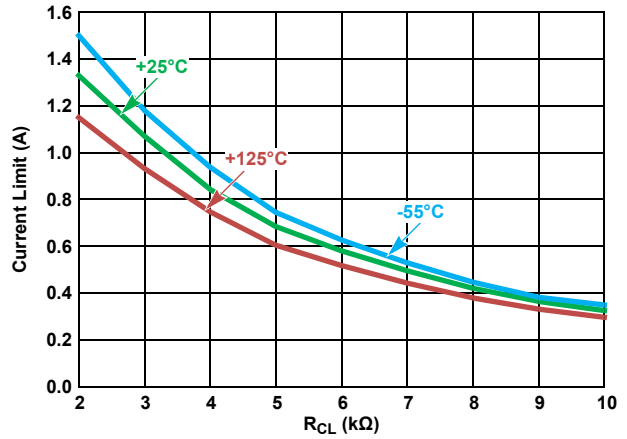


Figure 18. $I_{SC} -12V_{IN}, -10V_{OUT}$ (Characterization Results)

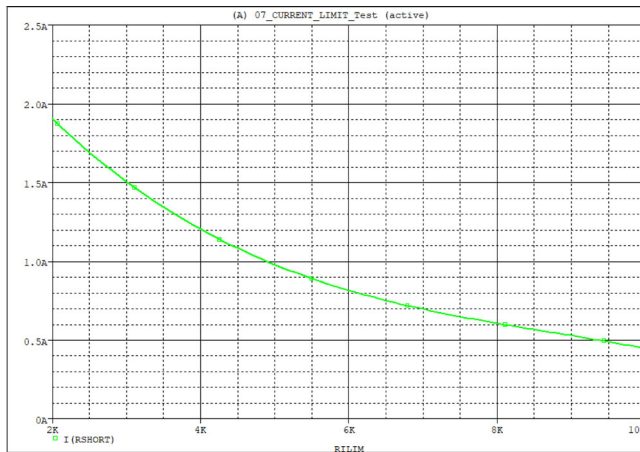


Figure 19. $I_{SC} -20V_{IN}, -10V_{OUT}$ (PSpice Results)

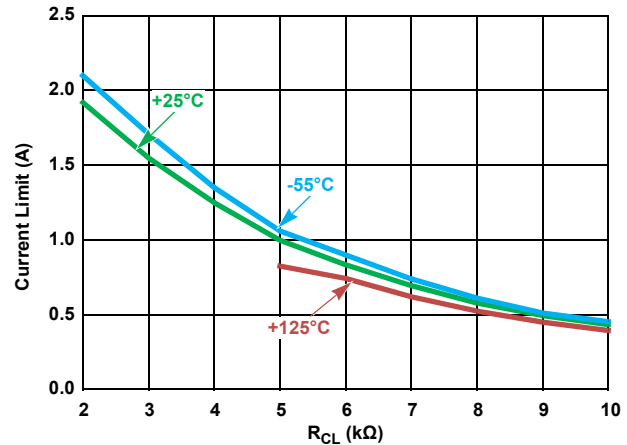


Figure 20. $I_{SC} -20V_{IN}, -10V_{OUT}$ (Characterization Results)

2.3 Bode Plots (Each graph shows simulation and test results)

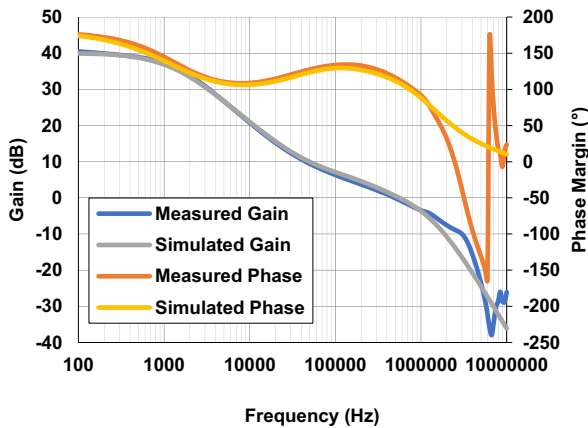


Figure 21. $-7V_{IN}, -5V_{OUT}, R_L = 6.2\Omega$

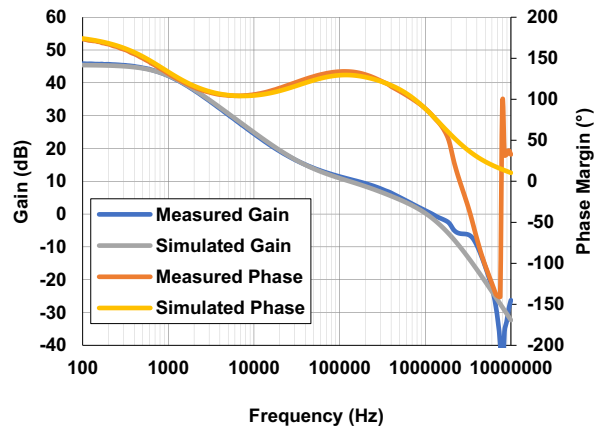


Figure 22. $-7V_{IN}, -5V_{OUT}, R_L = 10.1\Omega$

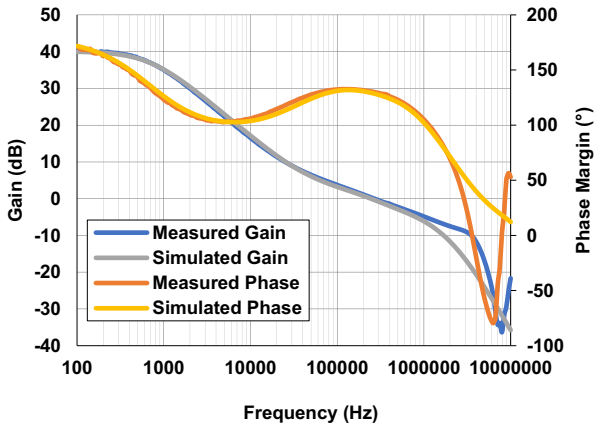


Figure 23. -15V_{IN}, -12V_{OUT}, R_L = 15Ω

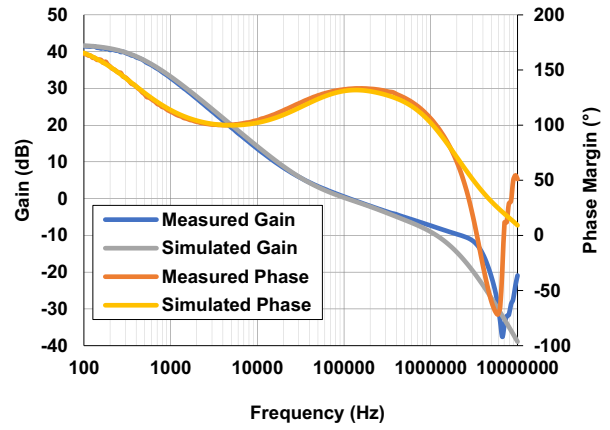


Figure 24. -15V_{IN}, -12V_{OUT}, R_L = 23.5Ω

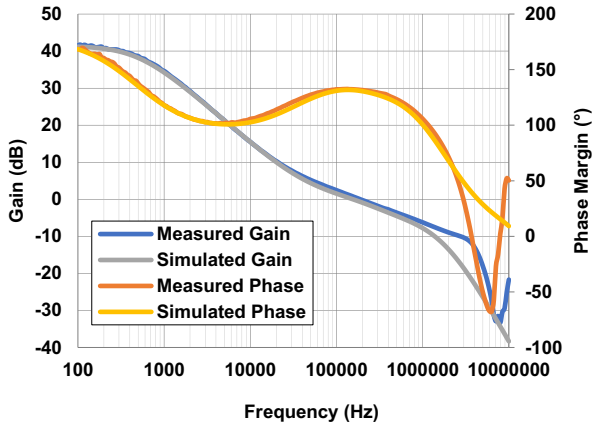


Figure 25. -20V_{IN}, -15V_{OUT}, R_L = 18.9Ω

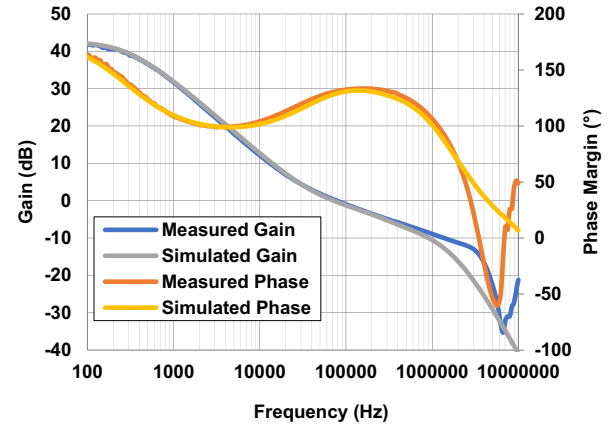


Figure 26. -20V_{IN}, -15V_{OUT}, R_L = 30Ω

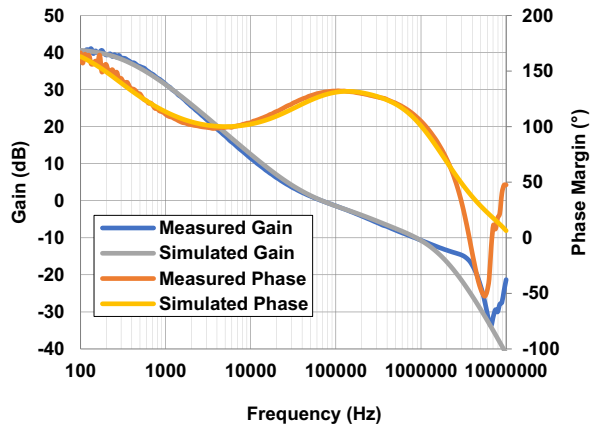


Figure 27. -28V_{IN}, -24V_{OUT}, R_L = 28.9Ω

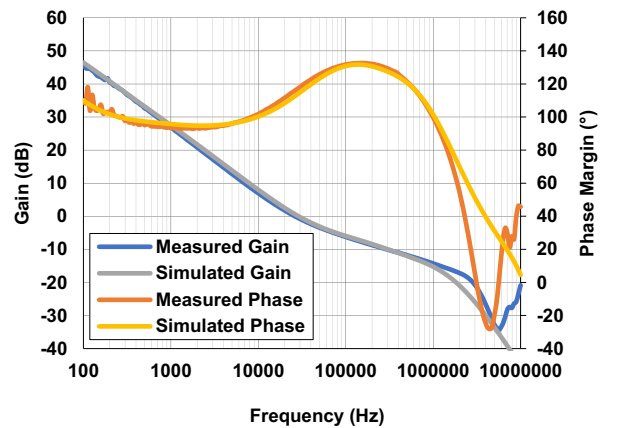


Figure 28. -28V_{IN}, -24V_{OUT}, R_L = 247Ω

2.4 PSRR Performance

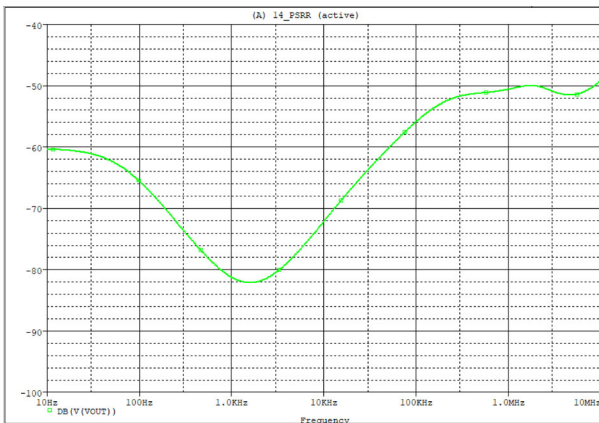


Figure 29. PSRR vs Frequency -20V_{IN}, -18V_{OUT} (PSpice Results)

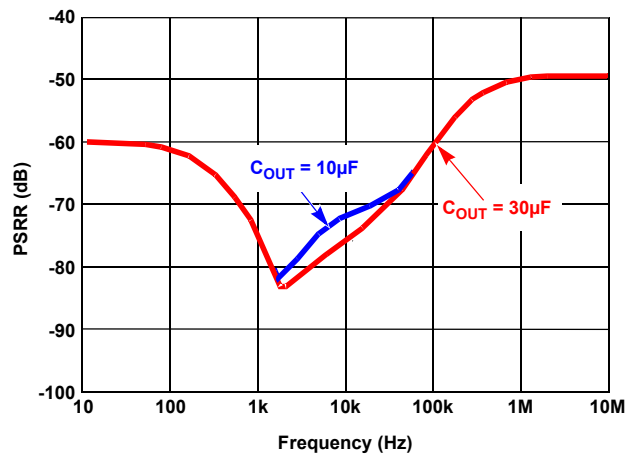


Figure 30. PSRR vs Frequency -20V_{IN}, -18V_{OUT} (Characterization Results)

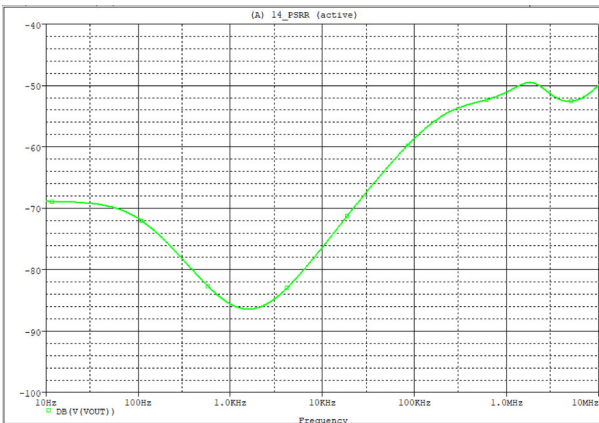


Figure 31. PSRR vs Frequency -7V_{IN}, -5V_{OUT} (PSpice Results)

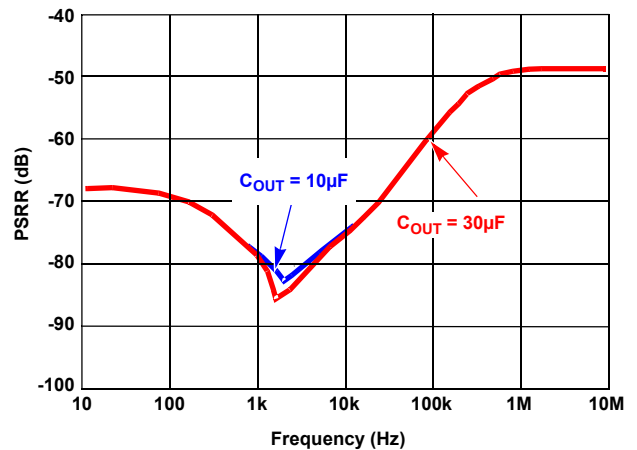


Figure 32. PSRR vs Frequency -7V_{IN}, -5V_{OUT} (Characterization Results)

2.5 Conclusion

The ISL72991RH PSpice model replicates the functionality of the ISL72991RH negative voltage regulator and closely matches the characterization curves in the ISL72991RH datasheet meeting the typical parametric performance of the datasheet specification table.

3. Revision History

Rev.	Date	Description
1.00	May.15.20	Initial release

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