R32C/100 Series

Overview of the Intelligent I/O Functions

Abstract

This document describes an overview of the intelligent I/O functions for the R32C/100 Series.

Note that the values for "i" and "j" in register names, register symbols, pin symbols, etc,. vary for each MCU group. Refer to the corresponding User's Manual: Hardware for values.

Products

R32C/100 Series

Contents

1.   Specifications

The intelligent I/O has been built-in to the R32C/100 Series and is a multifunctional I/O port that has a combined base timer and time measurement circuit, waveform generator, and communication block to perform time measurement, waveform generation, and serial interface function (the serial interface function is not available in the R32C/120, 121, 145, 151, 152, 153, 156, 157, 160, and 161 Groups).
The following briefly describes the intelligent I/O functions.

(1) The base timer is a free-running counter for an internally generated count source.
(2) The time measurement function stores the base timer value in group i time measurement register j each time an external trigger is input.
(3) The waveform generation function generates a waveform when the values of the base timer and group i waveform generation register j match.
(4) Variable character length synchronous serial interface mode is available though the serial interface function.

The intelligent I/O uses time measurement and waveform generation (i.e groups 0 and 1 in the R32C/118A Group), and waveform generation and the serial interface function (i.e. group 2 in the R32C/118A).
Figure 1.1 shows an example of how to use time measurement and waveform generation. Figure 1.2 shows an overview of how to use waveform generation and the serial interface function. When performing time measurement, use the base timer and time measurement circuit. When performing waveform generation, use the base timer and waveform generator. When using serial interface function, use the base timer and waveform generator or the base timer and communication block.
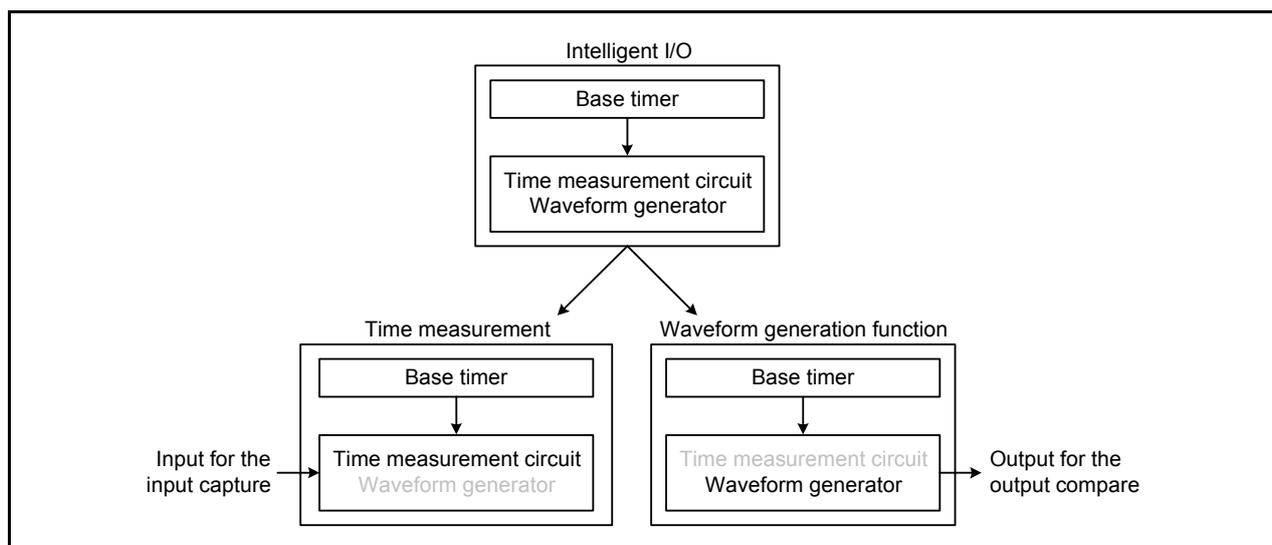
Figure 1.1   Overview of the Intelligent I/O for Groups Embedded With Time Measurement and Waveform Generation
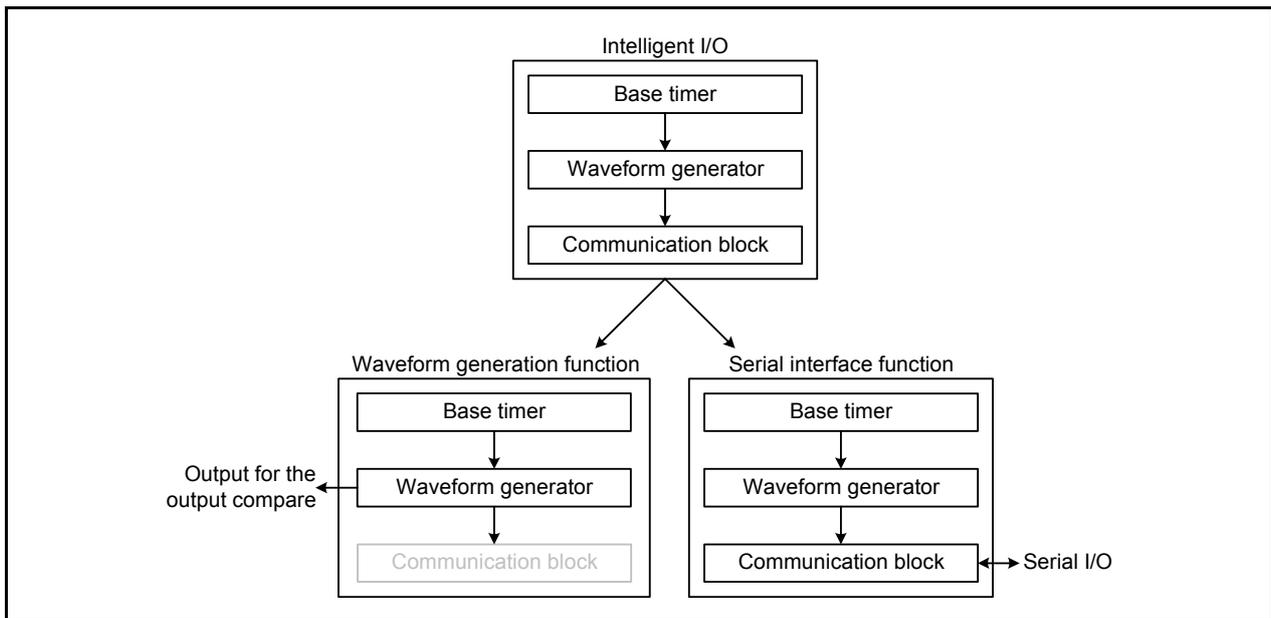
**Figure 1.2   Overview of the Intelligent I/O for Groups Embedded With Waveform Generation and
Serial Interface Function**

2.   Reference Application Notes

Application notes associated with this application note are listed below. Refer to these application notes for
additional information.

• R32C/100 Series Pulse-Width Measurement Using the Digital Debounce Function of Intelligent I/O
  (R01AN0336EJ0100)
• R32C/100 Series PWM Output Using Phase Shift Waveform Output Mode in the Intelligent I/O
  (R01AN0337EJ0100)
• R32C/100 Series Time Measurement Using the Gate Function of Intelligent I/O Groups 0 and 1
  (R01AN0094EJ0100)
• R32C/100 Series Pulse-Width Measurement Using the Time Measurement Function of Intelligent I/O
  Groups 0 and 1 (R01AN0096EJ0100)
• R32C/100 Series Synchronous Serial Interface Mode for Intelligent I/O Group 2 (R01AN0097EJ0100)
• R32C/100 Series How to Use Intelligent I/O Interrupt (REJ05B1416-0100)
• R32C/100 Series Intelligent I/O Single-phase Waveform Output Mode (REJ05B1226-0100)
• R32C/100 Series Intelligent I/O SR Waveform Output Mode (REJ05B1227-0100)

3. Peripheral Functions

3.1 Intelligent I/O Functions by Group

Some MCU groups in the R32C/100 Series have up to four groups of intelligent I/O (group 0 to group 3). The intelligent I/O has a maximum of 32 I/O channels for the time measurement function, and a maximum of 32 I/O channels for the waveform generation function. The serial interface supports variable character length synchronous serial I/O and IEBus.

Table 3.1 lists the functions available in the intelligent I/O and the number of channels.

Table 3.1   Functions Available in the Intelligent I/O

MCU Group		R32C/111			R32C/116, R32C/117, R32C/118			R32C/116A, R32C/117A, R32C/118A		
Intelligent I/O group		0	1	2	0	1	2	0	1	2
Time measurement	Digital filter	8	8	N/A	8	8	N/A	8	8	N/A
	Prescaler	2	2	N/A	2	2	N/A	2	2	N/A
	Gating	2	2	N/A	2	2	N/A	2	2	N/A
Waveform generation	Single-phase waveform output mode	8	8	3	8	8	8	8	8	8
	Inverted waveform output mode	8	8	3	8	8	8	8	8	8
	SR waveform output mode	8	8	3	8	8	8	8	8	8
	Bit modulation PWM output mode	N/A	N/A	3	N/A	N/A	8	N/A	N/A	8
	RTP mode	N/A	N/A	3	N/A	N/A	8	N/A	N/A	8
	Parallel RTP mode	N/A	N/A	3	N/A	N/A	8	N/A	N/A	8
Serial interface	Variable character length synchronous serial I/O mode	N/A	N/A	A	N/A	N/A	A	N/A	N/A	A
	IEBus mode	N/A	N/A	A	N/A	N/A	A	N/A	N/A	A

| MCU Group		R32C/120, R32C/121		R32C/145		R32C/151, R32C/152, R32C/153, R32C/156, R32C/157				R32C/160, R32C/161
Intelligent I/O group		0	1	0	1	0	1	2	3	0
Time measurement	Digital filter	8	8	8	8	8	8	8	8	8
	Prescaler	2	2	2	2	2	2	2	2	2
	Gating	2	2	2	2	2	2	2	2	2
	Digital debounce function	1	1	1	1	1	1	1	1	1
Waveform generation	Single-phase waveform output mode	8	8	8	8	8	8	8	8	8
	Inverted waveform output mode	8	8	8	8	8	8	8	8	8
	SR waveform output mode	8	8	8	8	8	8	8	8	8
	Phase shift waveform output mode	8	8	8	8	8	8	8	8	8

Numbers: Number of channels
A: Function is available
N/A: Function is not available

3.2   Intelligent I/O Configuration

Figure 3.1 and Figure 3.2 show block diagrams of the intelligent I/O. Figure 3.1 shows a block diagram of groups with an embedded time measurement circuit and waveform generation function.
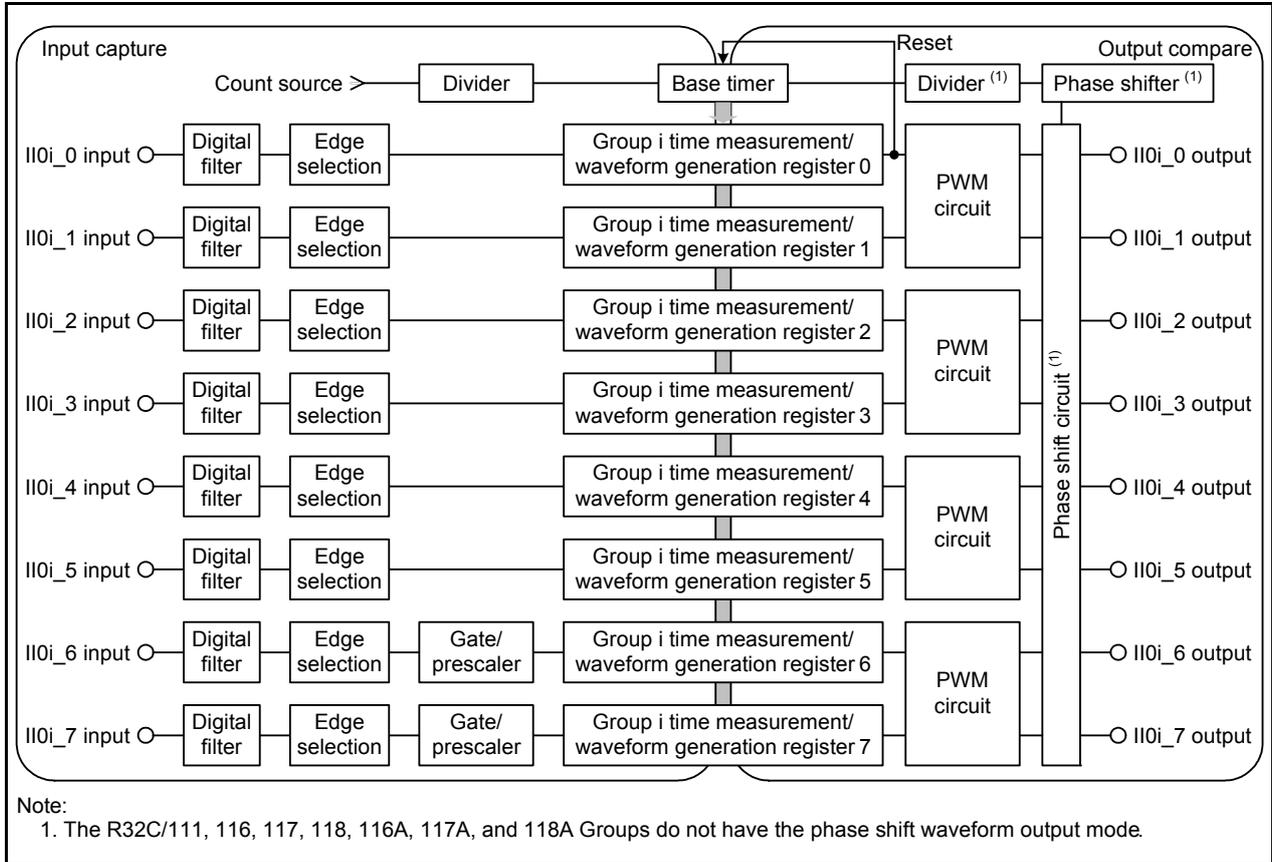
Figure 3.1   Block Diagram of the Intelligent I/O With Embedded Time Measurement Circuit and Waveform Generation Function

Figure 3.2 shows a block diagram of groups with embedded waveform generation function and serial interface function.
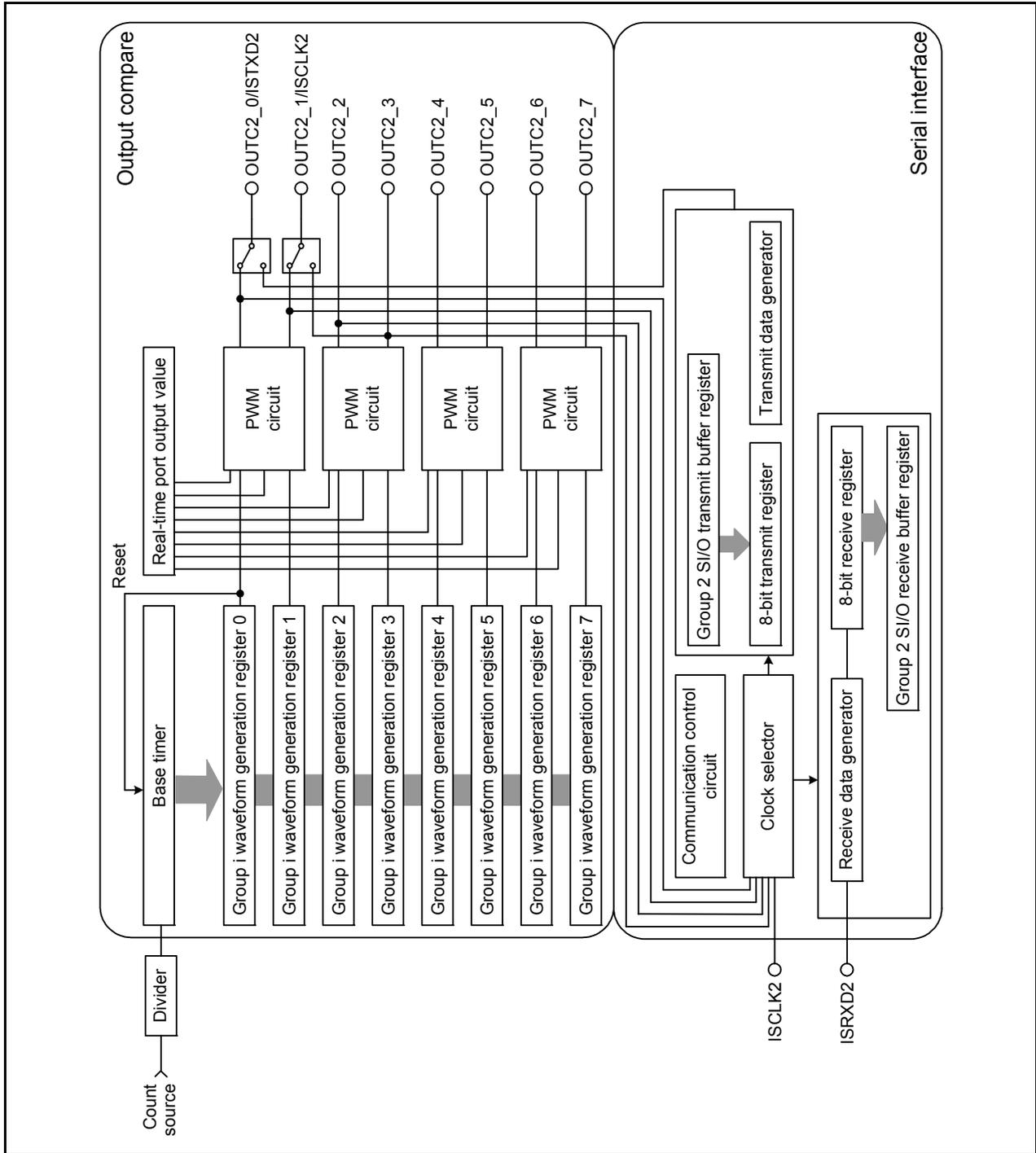
Figure 3.2   Block Diagram of the Intelligent I/O With Embedded Waveform Generation Function and Serial Interface Function

3.3 Base Timer

The base timer is built-in to the intelligent I/O in all groups, and is comprised mainly of the time measurement function and waveform generation function. The base timer is a 16-bit free-running counter. The base timer can select the following as sources for a base timer reset: base timer overflow, value match with group i waveform generation register 0, and low input to an external interrupt pin. The count source and reset source that can be selected differ depending on the group.

Table 3.2 lists the count source and reset source for the base timer by group. For details on the base timer reset due to a value match with group i waveform generation register 0, refer to section 3.5.1.

Table 3.2   Count Source and Reset Source for the Base Timer

MCU Group		R32C/111			R32C/116, R32C/117, R32C/118			R32C/116A, R32C/117A, R32C/118A		
Intelligent I/O group		0	1	2	0	1	2	0	1	2
Count source	f1	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Two-phase pulse input	SE	SE	NS	SE	SE	NS	SE	SE	NS
Reset source	Request from another group	SE	SE	SE	SE	SE	SE	SE	SE	SE
	$\overline{INT0}$ pin	SE	NS	NS	SE (1)	SE (1)	NS	SE (1)	SE (1)	NS
	$\overline{INT1}$ pin	NS	SE	NS			NS			NS
	BTiS, BTS [2]	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Base timer overflow	SE	SE	NS	SE	SE	NS	SE	SE	NS
	Match with group i waveform generation register 0	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Request from serial interface function	NS	NS	SE	NS	NS	SE	NS	NS	SE

MCU Group		R32C/120, R32C/121		R32C/145		R32C/151, R32C/152, R32C/153, R32C/156, R32C/157				R32C/160, R32C/161
Intelligent I/O group		0	1	0	1	0	1	2	3	0
Count source	f1	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Two-phase pulse input	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Timer B0 interrupt	SE	SE	SE	SE	SE	SE	SE	SE	SE
Reset source	Request from another group	SE	SE	SE	SE	SE	SE	SE	SE	NS
	$\overline{INT0}$ pin	SE	NS	SE (1)	SE (1)	SE (1)	SE (1)	SE (1)	SE (1)	SE
	$\overline{INT1}$ pin	NS	SE							NS
	BTS	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Base timer overflow	SE	SE	SE	SE	SE	SE	SE	SE	SE
	Match with group i waveform generation register 0	SE	SE	SE	SE	SE	SE	SE	SE	SE

SE: Selectable
NS: Not selectable
Notes:
1. Either $\overline{INT0}$ or $\overline{INT1}$ is selectable.
2. Reset when bits BTiS and BTS become 0.

3.4   Time Measurement Function

Every time an external trigger is input, the base timer value is stored into group i time measurement register j. When a trigger is input, a time measurement interrupt request is generated.

Figure 3.3 shows a timing diagram when using the time measurement function.
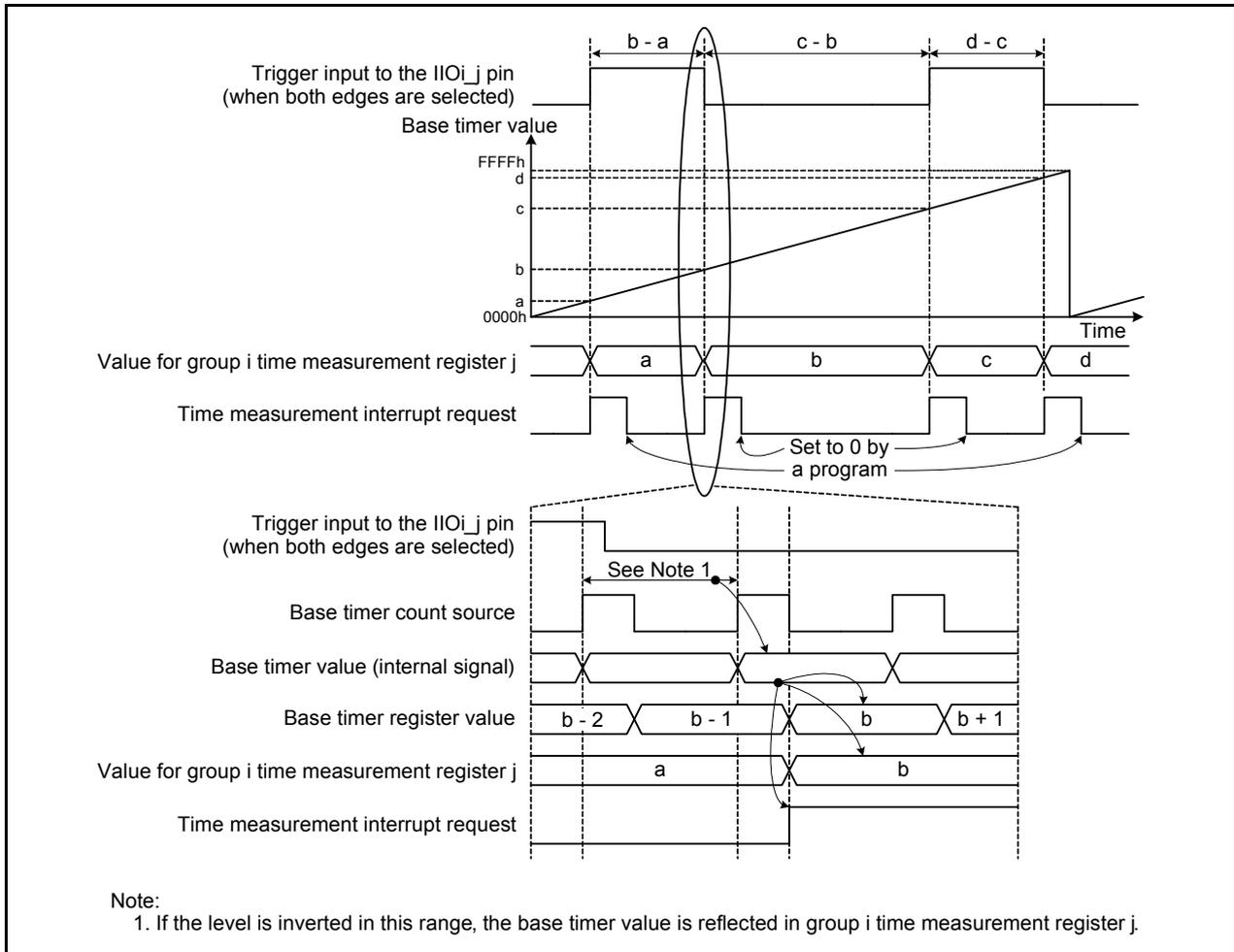
Figure 3.3   Timing Diagram of the Time Measurement Function

The time measurement function uses the following functions to measure signals based on the objective.

- Edge selection
- Digital filter
- Gating
- Prescaler
- Digital debounce function

These functions are described in the sections below.

3.4.1 Edge Selection

For edge selection, polarity of the trigger input can be selected from rising edge, falling edge, or both edges.

3.4.2 Digital Filter

The digital filter determines the trigger input level three times with the clock selected (f1 or base timer count source). Signal levels that match three times pass through the digital filter and become trigger signals. Signals that did not match are considered to be noise and are filtered out. Figure 3.4 shows the timing diagram of the digital filter. Figure 3.4 assumes the trigger input polarity is both edges, and base timer count source (fBTi) is the determination clock for the trigger input level.
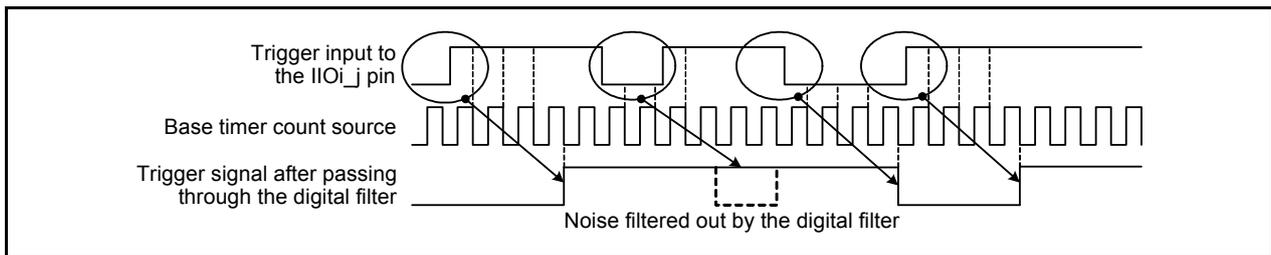
Figure 3.4   Digital Filter Timing Diagram

After a rising edge is input to the IIOi_j pin, the level is determined three times for every fBTi cycle. When the level matches three times, signals that have passed through the digital filter change. By using signals that have passed through the digital filter, time measurement is possible using noise-filtered trigger signals. (When using the digital filter function, the trigger signal is delayed in order to determine the trigger input level, but the delay occurs at all trigger input levels, so time is measured accurately.)

3.4.3   Gating

Gating disables any trigger input to be accepted for a certain period of time after the first trigger is input. Gating can be cleared either by a program, or when group i waveform generation register j matches the base timer value.

Figure 3.5 shows a timing diagram for the gate function.
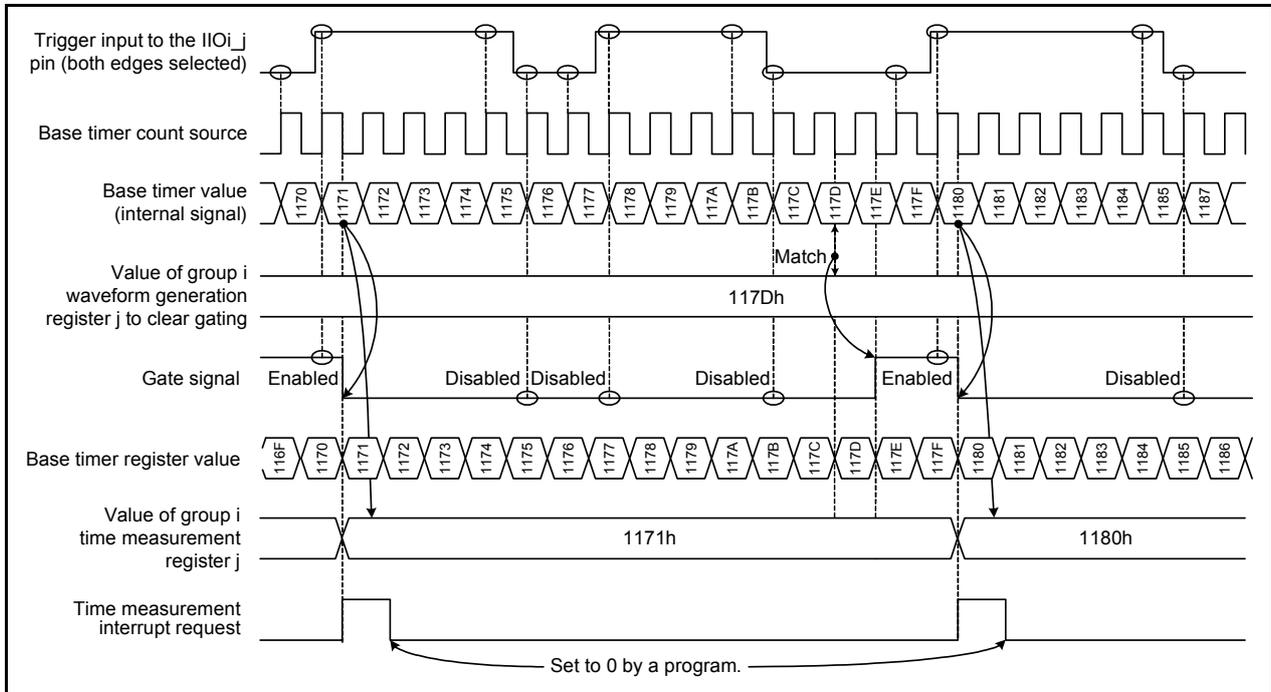
Figure 3.5   Timing Diagram of Gating

In Figure 3.5, the base timer value is stored to group i time measurement register j by a trigger input to the IIOi_j pin, and trigger inputs are not accepted. If the base timer value matches the value written to group i waveform generation register j (117Dh), the trigger inputs are accepted. After trigger input is changed from not accepted to accepted, the base timer value is written to group i time measurement register j at the trigger input timing.

3.4.4   Prescaler

When using the prescaler, the base timer value is stored to group i time measurement register j for the set number of times the trigger is input. The prescaler value is set in an 8-bit register, and can be set to a maximum of 256 times (the number of times is the value set for the prescaler + 1).
Figure 3.6 shows the timing diagram for the prescaler.
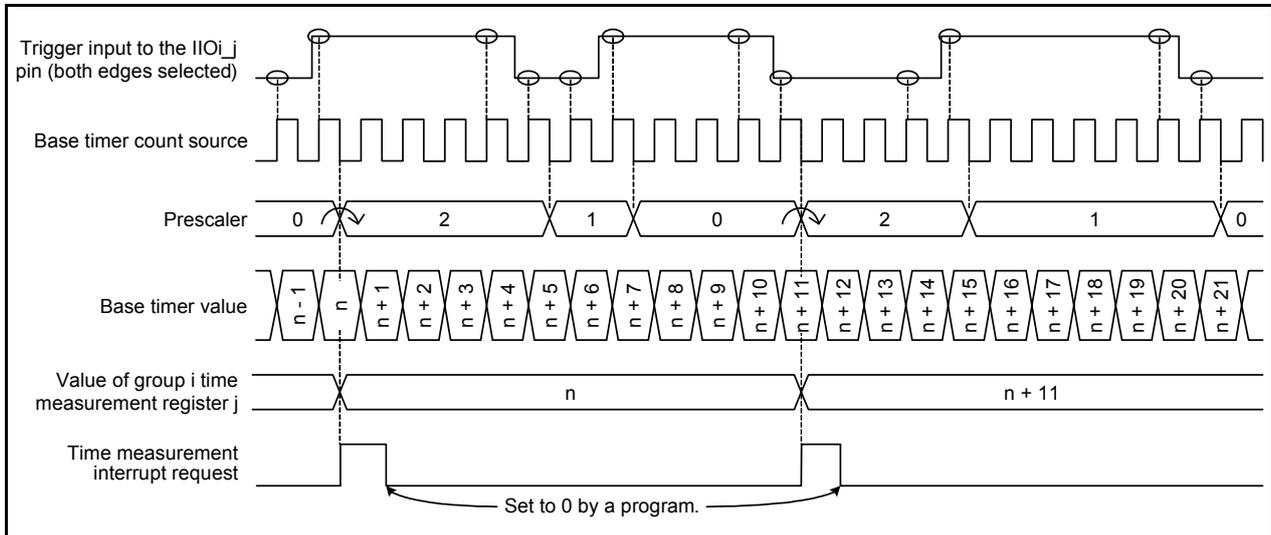
Figure 3.6   Prescaler Timing Diagram

In Figure 3.6, the prescaler value is set to 2. When the base timer value is stored to group i time measurement register j after the first trigger input, the number of trigger inputs is counted, and the base timer value is stored at the third trigger input.

3.4.5   Digital Debounce Function

After a rising or falling edge, when a filter width longer than the filter width set by a program is retained, the signal level is determined.
The counter for the digital debounce circuit decrements the count with a count source of f8. Every time the signal level at the IIOi_7 pin changes, the counter is reloaded and counting resumes. The input signal to the IIOi_7 pin is output from the digital debounce circuit on the first rising edge of f8 after the counter value becomes 00h.

Note that the digital debounce function can only be used with the R32C/120, 121, 145, 151, 152, 153, 156, 157, 160, and 161 Groups.

3.5   Waveform Generation Function

The waveform generation function generates a match signal when the base timer value and group i waveform generation register j value match. The signal generated from this match generates an interrupt request and the output signal changes.

Figure 3.7 shows a timing diagram for the waveform generation function.
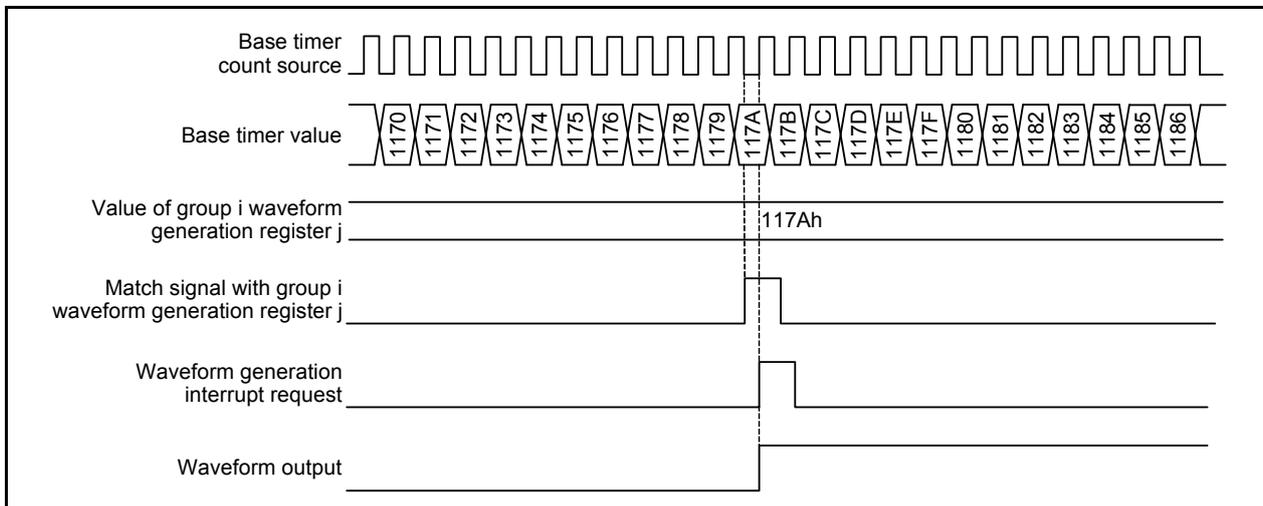
Figure 3.7   Timing Diagram for the Waveform Generation Function

3.5.1   Waveform Generation Modes

The following modes are common to all intelligent I/O groups.

- Single-phase waveform output mode

  In this mode, the output level from the waveform output pin becomes high when the group i waveform generation register j value and base timer value match. When the base timer value becomes 0000h, the output level from the waveform output pin becomes low.

- Inverted waveform output mode

  In this mode, each time the group i waveform generation register j value and base timer value match, the output level from the waveform output pin is inverted.

- SR waveform output mode

  In this mode, the output level from the waveform output pin becomes high when the group i waveform generation register n value and base timer value match (n = 0, 2, 4, 6). The output level from the waveform output pin becomes low when the group i waveform generation register m value and base timer value match, or when the base timer becomes 0000h (m = n + 1).

Figure 3.8 shows the timing diagram for various waveform generation outputs.
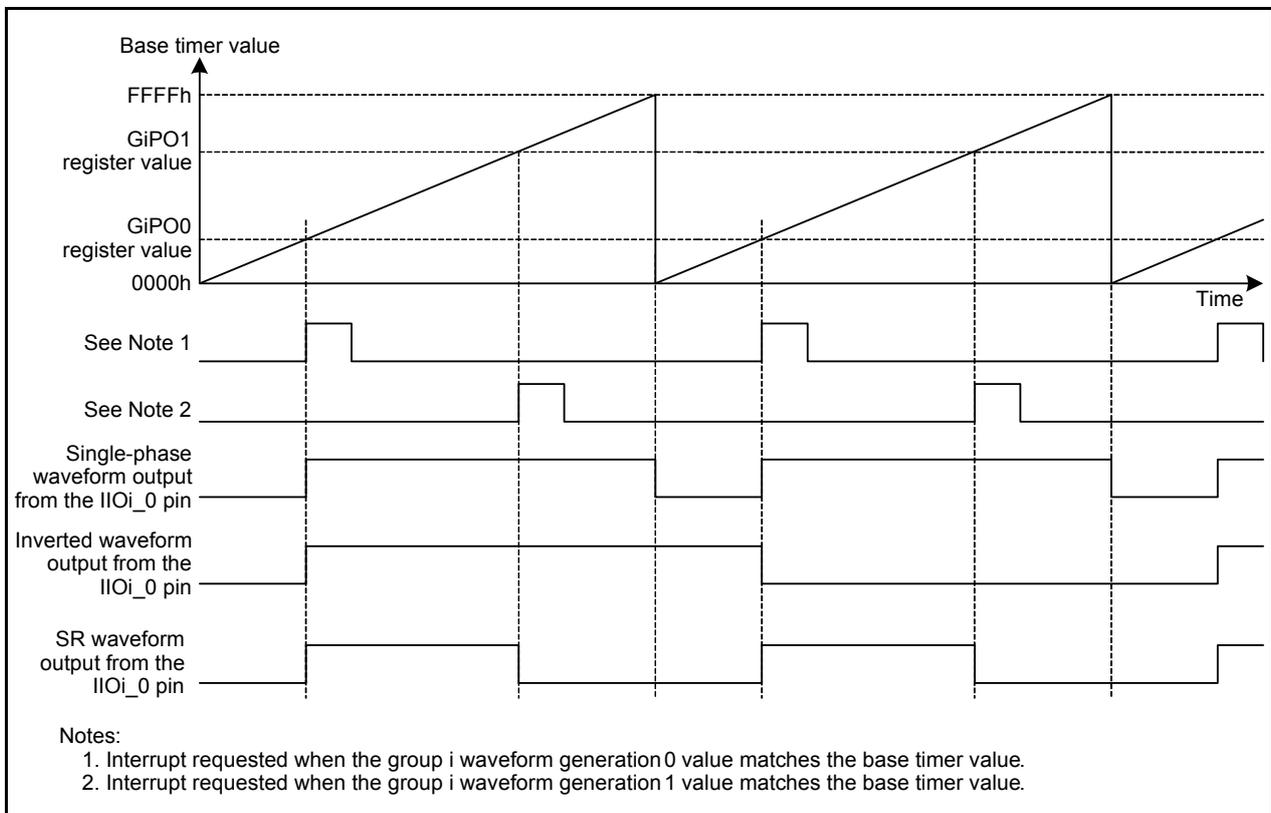
Figure 3.8   Timing Diagram for Various Waveform Generation Outputs

The following functions can be set to all three modes above.
- Default value setting
  This function determines the starting waveform output level.
- Output level inversion
  This function inverts the waveform output level and outputs the inverted signal from the IIOi_j pin (or OUTC2_j pin for group 2).
- Base timer reset function
  With this function, the base timer is reset when the group i waveform generation register 0 value matches the base timer value. Two clocks after these values match, the base timer value becomes 0000h.

Figure 3.9 shows the timing diagram for the base timer reset function.
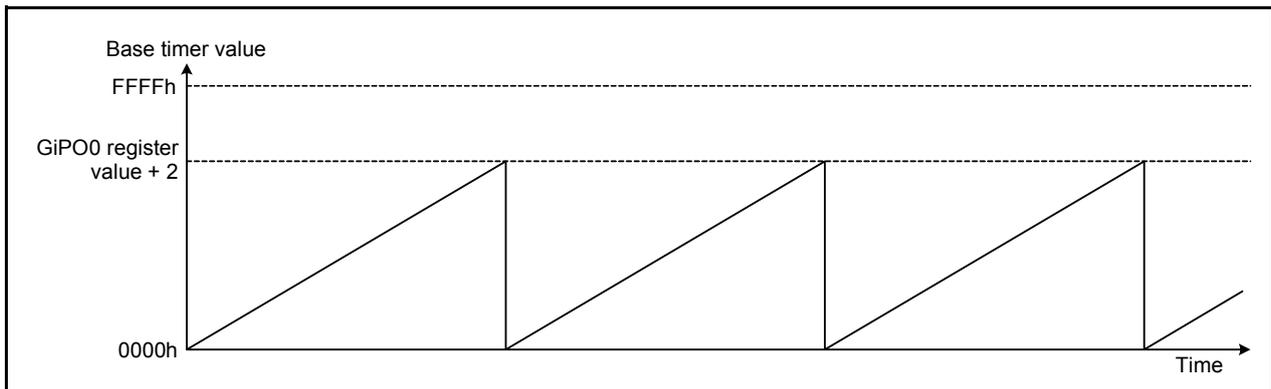
Figure 3.9   Base Timer Reset Timing Diagram

3.5.2   Example of 16-Bit PWM Output

When using the intelligent I/O, a variable 16-bit PWM waveform can be output. This section describes outputting a 16-bit PWM waveform using the waveform generation function. The PWM output is set in group i waveform generation register 0. Select "match with the GiPO0 register" as the source for the base timer reset. Set the low level width of the output waveform in group i waveform generation register j.

Figure 3.10 shows the timing diagram of 16-bit PWM output. In this figure, the base timer is started by setting "x" to group i waveform generation register 0 and "m" to group i waveform generation register j. When the base timer and group i waveform generation register 0 values become equal, the conditions for an interrupt request are satisfied, two clocks elapse before low is output from the IIOi_j pin, and the base timer value becomes 0000h.
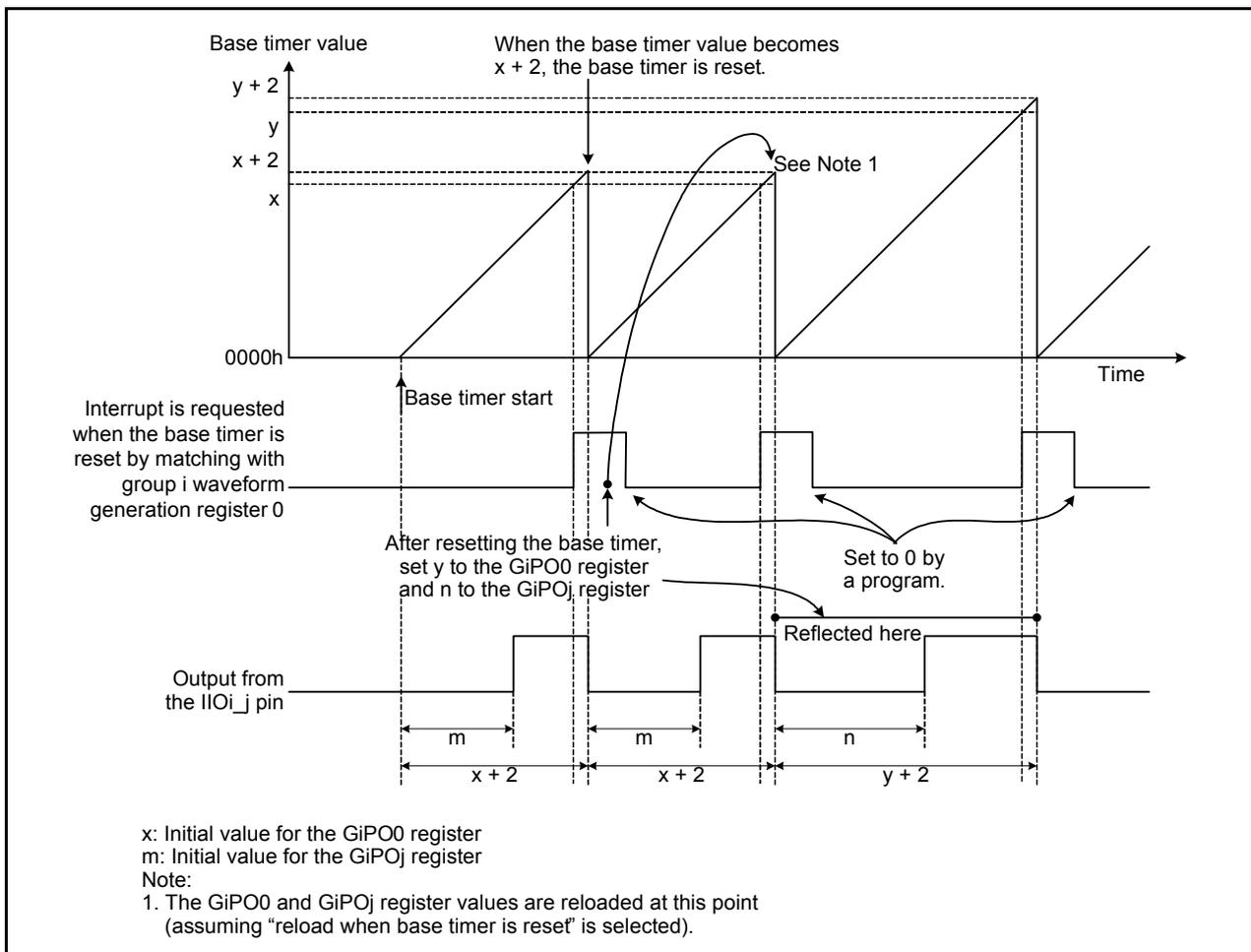
Figure 3.10   Timing Diagram of 16-Bit PWM Output

3.5.3   Bit Modulation PWM Output Mode

When modifying the pulse width of a PWM output using 16-bit resolution, a PWM output that uses a timer requires a cycle of $\dfrac{\text{FFFFh}}{\text{Count source}}$. However, when using bit modulation PWM output mode, a high carrier frequency is feasible while retaining the 16-bit PWM accuracy.

In bit modulation PWM output mode, the carrier frequency is equivalent to a 6-bit PWM, and the PWM accuracy (resolution) is 16 bits.

Figure 3.11 shows a timing diagram of the bit modulation PWM output mode.

The PWM cycle is fixed at $\dfrac{64 \text{ clock cycles}}{\text{fBT2}}$. The 6 upper bits in group i waveform generation register j determine the low width of the PWM. The 10 lower bits determine the number of times in which the low width is extended in one clock cycle.
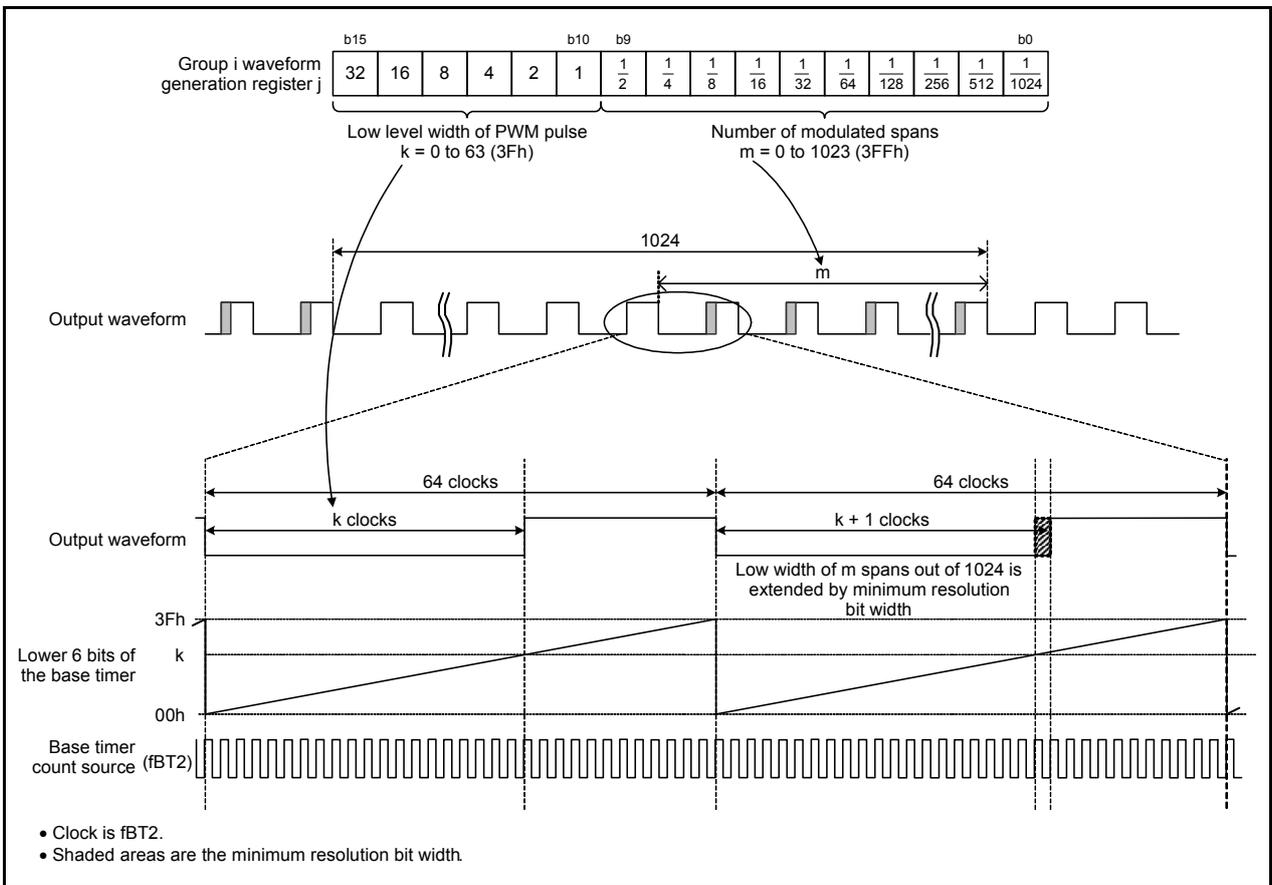
Figure 3.11   Timing Diagram of Bit Modulation PWM Output Mode

Note that the bit modulation PWM output mode can only be used in the R32C/111, 116, 117, 118, 116A, 117A, and 118A Groups.

3.5.4   RTP Output Mode

In real-time port (RTP) output mode, when the group 2 waveform generation register j value matches the base timer value, the value of bit j in the group 2 RTP output buffer register is output from each waveform output pin.

Figure 3.12 shows the outline of RTP output mode, and Figure 3.13 shows the timing diagram of RTP output mode.
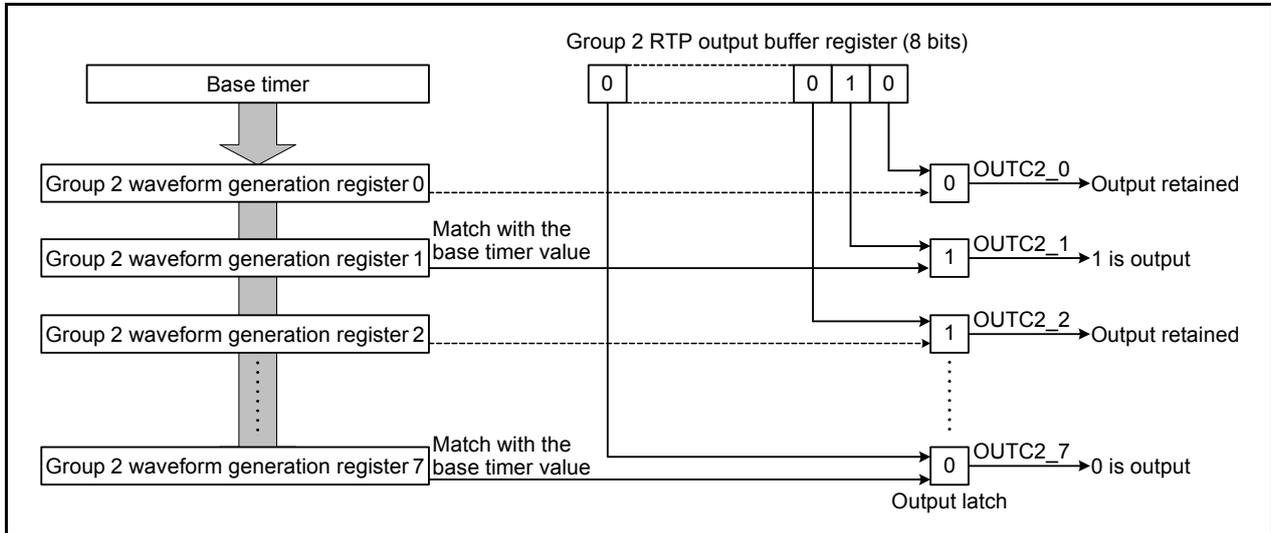
Figure 3.12   Outline of the RTP Output
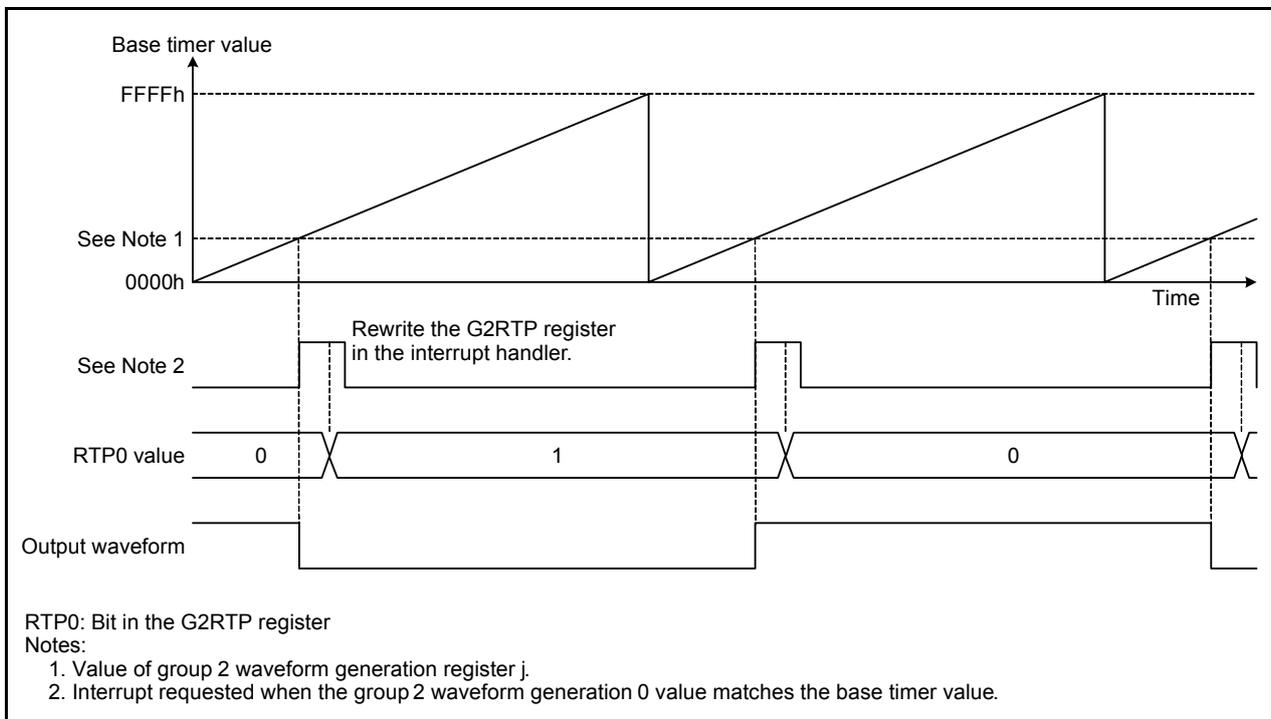
Figure 3.13   Timing Diagram of RTP Output Mode

Note that the RTP output mode can only be used with the R32C/111, 116, 117, 118, 116A, 117A, and 118A Groups.

3.5.5 Parallel RTP Output Mode

In parallel RTP output mode, when the group 2 waveform generation register j value matches the base timer value, the value set to the group 2 RTP output buffer register is output from the corresponding output pins in 1-byte units. In this mode, the pin level can be changed in short intervals. Note that the parallel RTP output mode can only be used with the R32C/111, 116, 117, 118, 116A, 117A, and 118A Groups. Figure 3.14 shows an outline of parallel RTP output mode, and Figure 3.15 shows a timing diagram of the parallel RTP output mode operation.
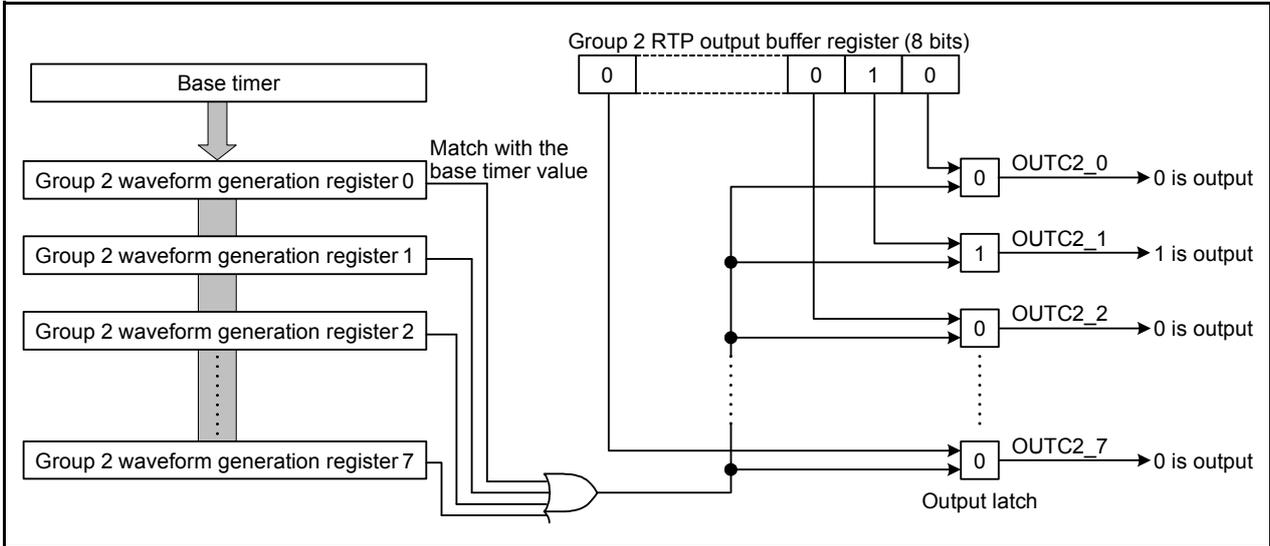
Figure 3.14   Outline of Parallel RTP Output Mode

Notes:
1. Value of group 2 waveform generation register j.
2. Interrupt requested when the group 2 waveform generation register j value matches the base timer value.
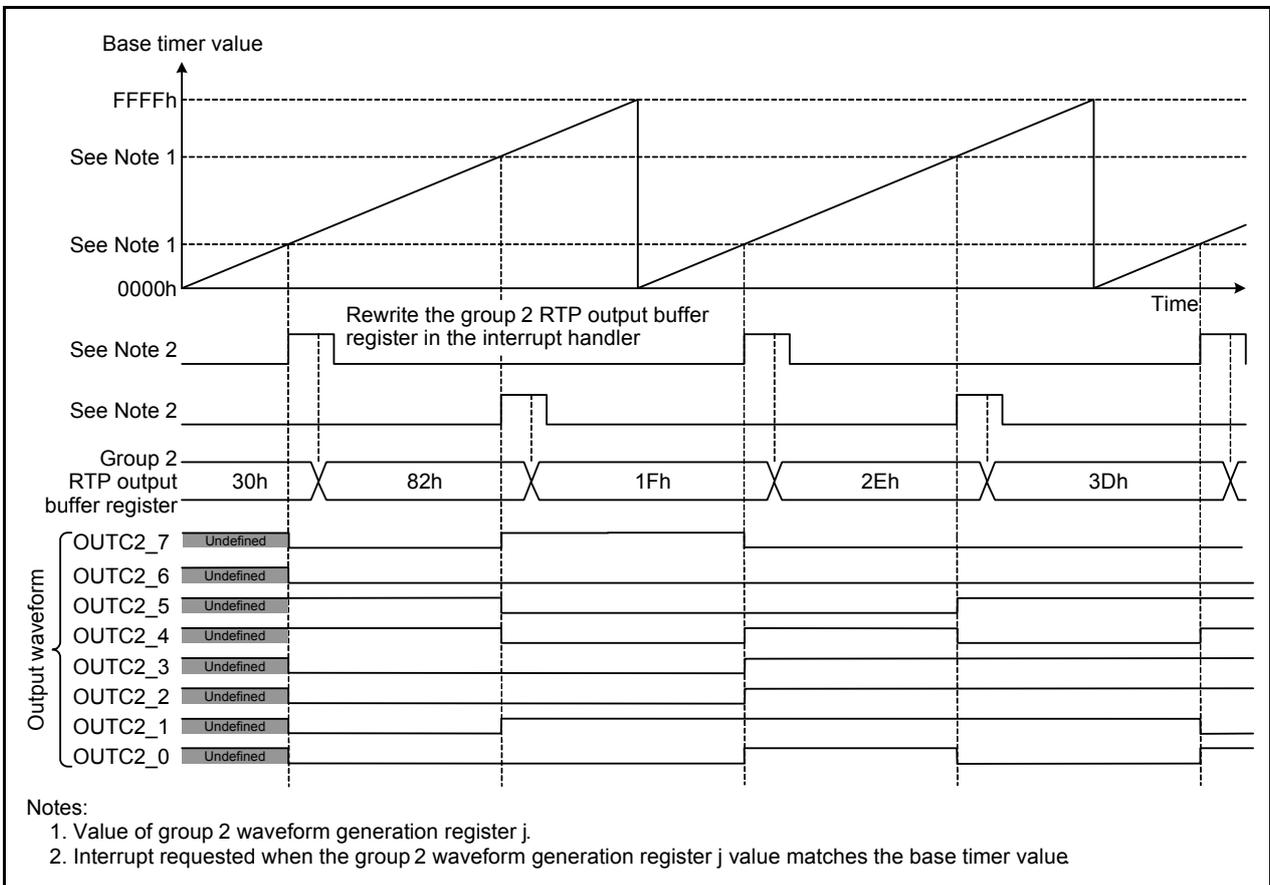
Figure 3.15   Timing Diagram of the Parallel RTP Output Mode Operation

3.5.6   Phase Shift Waveform Output Mode

In phase shift waveform output mode, PWM output is phase-shifted at every channel. This mode enables functions that help reduce switching noise and instantaneous power consumption. When the phase shift waveform output mode is enabled, the phase shifter controls when the output level at the IIOi_j pin becomes high. Each time the phase shift clock is input, each output level of the IIOi_0 pin sequentially becomes high.

Note that the phase shift waveform output mode can only be used with the R32C/120, 121, 145, 151, 152, 153, 157, 160, and 161 Groups.

3.6   Serial Interface Function

This function can only be used with the R32C/111, 116, 117, 118, 116A, 117A, and 118A Groups.

3.6.1   Variable Character Length Synchronous Serial I/O

The serial interface function of the intelligent I/O is comprised of variable character length synchronous serial I/O and the IEBus. When using the variable character length synchronous serial I/O, the transmit and receive clocks are generated by channel 2 waveform generation in inverted waveform output mode. When writing transmit data to the group 2 SI/O transmit buffer register (G2TB), transmit data is output from the ISTXD2 pin in synchronization with the transmit and receive clocks.

Figure 3.16 shows the timing diagram of output while in variable character length synchronous serial I/O mode.
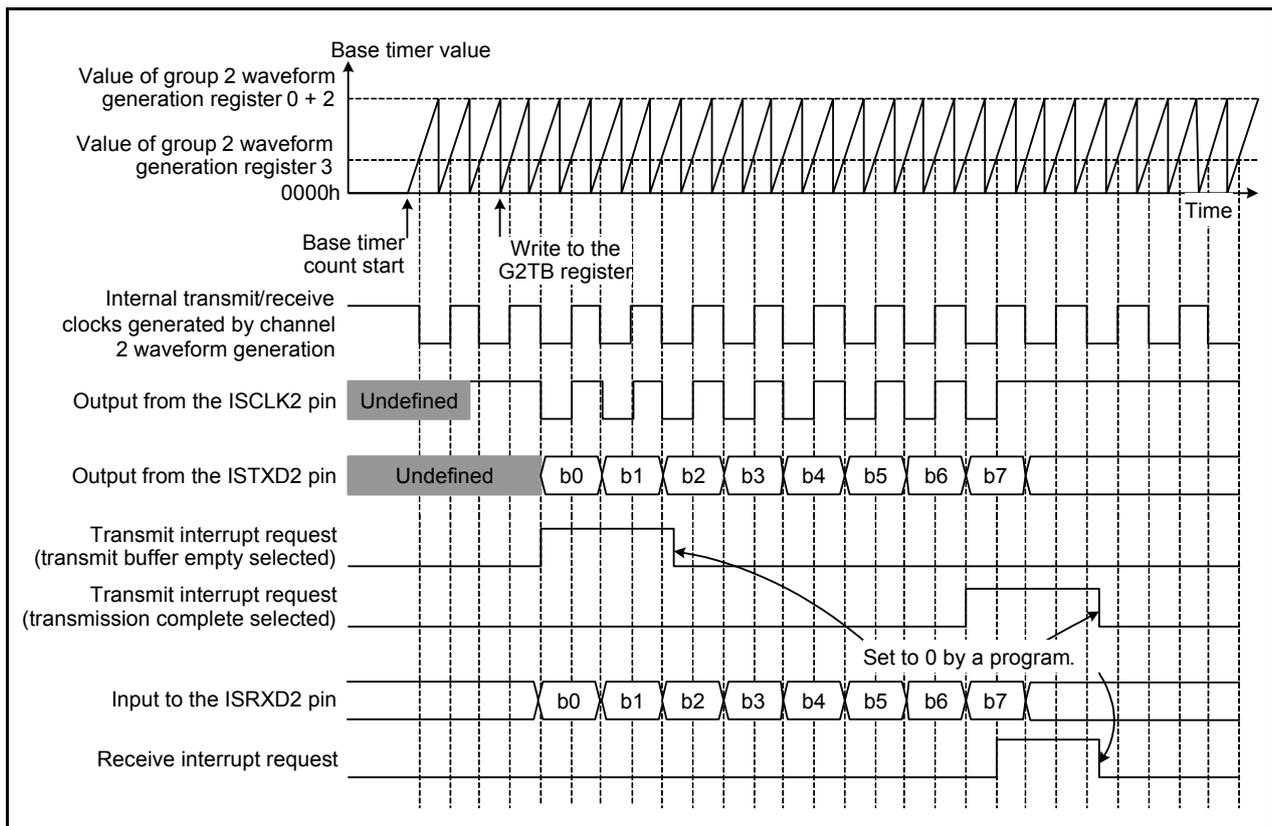
Figure 3.16   Timing Diagram of Output While In Variable Character Length Synchronous Serial I/O Mode

3.6.2   IEBus

The IEBus is an optional function. Contact a Renesas Electronics sales office to use this feature.

4. Reference Documents

R32C/111 Group User's Manual: Hardware Rev.1.20
R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
R32C/116A Group User's Manual: Hardware Rev.1.00
R32C/117A Group User's Manual: Hardware Rev.1.00
R32C/118A Group User's Manual: Hardware Rev.1.00
R32C/120 Group User's Manual: Hardware Rev.1.20
R32C/121 Group User's Manual: Hardware Rev.1.20
R32C/145 Group User's Manual: Hardware Rev.1.10
R32C/151 Group User's Manual: Hardware Rev.1.10
R32C/152 Group User's Manual: Hardware Rev.1.10
R32C/153 Group User's Manual: Hardware Rev.1.10
R32C/156 Group User's Manual: Hardware Rev.1.10
R32C/157 Group User's Manual: Hardware Rev.1.10
R32C/160 Group User's Manual: Hardware Rev.1.02
R32C/161 Group User's Manual: Hardware Rev.1.02
The latest versions can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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Inquiries
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Revision History		R32C/100 Series Overview of the Intelligent I/O Functions		

Rev.	Date	Description		
		Page	Summary	
1.00	Dec. 14, 2012	—	First edition issued	

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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