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April 1st, 2010
Renesas Electronics Corporation

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APPLICATION NOTE

PWM Output of Three Signals with Independently Controllable Duty Cycles

Introduction

Applies the PWM mode of the H8/3687's timer Z block to output three PWM waveforms with the same period but individually controllable duty cycles.

Target Device

H8/300H Tiny Series H8/3687

Contents

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1. Specifications

1. Applies the PWM mode of the H8/3687's timer Z block to output three PWM waveforms with the same period but individually controllable duty cycles.
2. This sample task involves controlling the H8/3687 to produce outputs of the form shown in figure 1.1, that is, three PWM waveforms, each of which has a controllable duty cycle but the same period. This is achieved through control of the high-level pulse width.
3. Any duty cycle from 0 to 100% is specifiable for each of the signals by the settings in the relevant registers.

$$\text{Duty cycle} = \frac{\text{High-level pulse width}}{\text{Period pulse}} \times 100\ (\%)$$

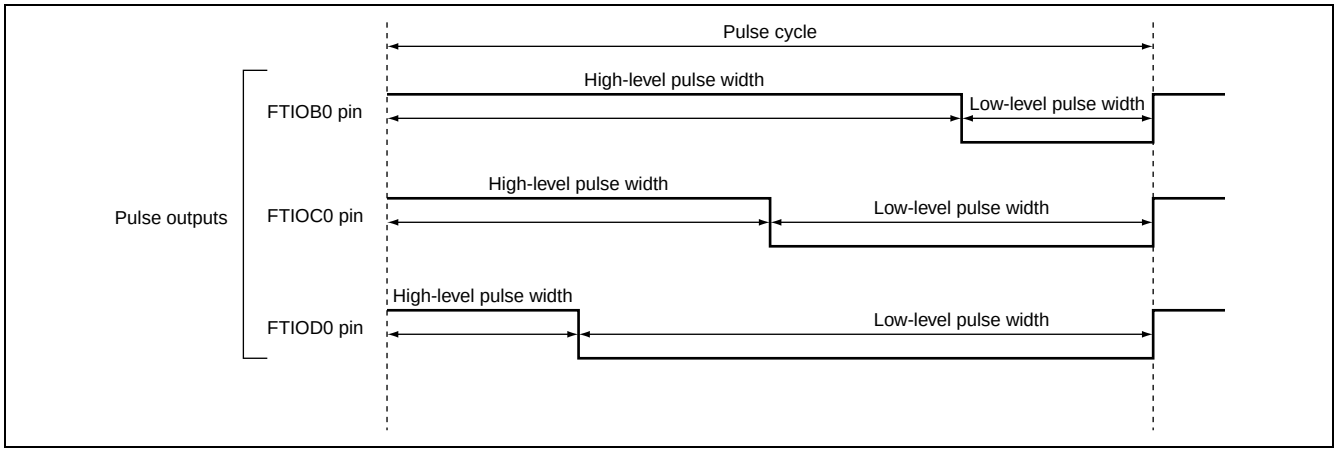


Figure 1.1 Output of Three PWM Signals

2. Functional Descriptions

1. In this sample task, the H8/3687 is controlled to produce three PWM waveforms by using channel 0 of timer Z.
   1) Figure 2.1 is a block diagram of timer Z, which is used in this sample task.
      The sample task uses the following function of timer Z.

— Clearing of the counter in response to a compare-match (counter clearing).

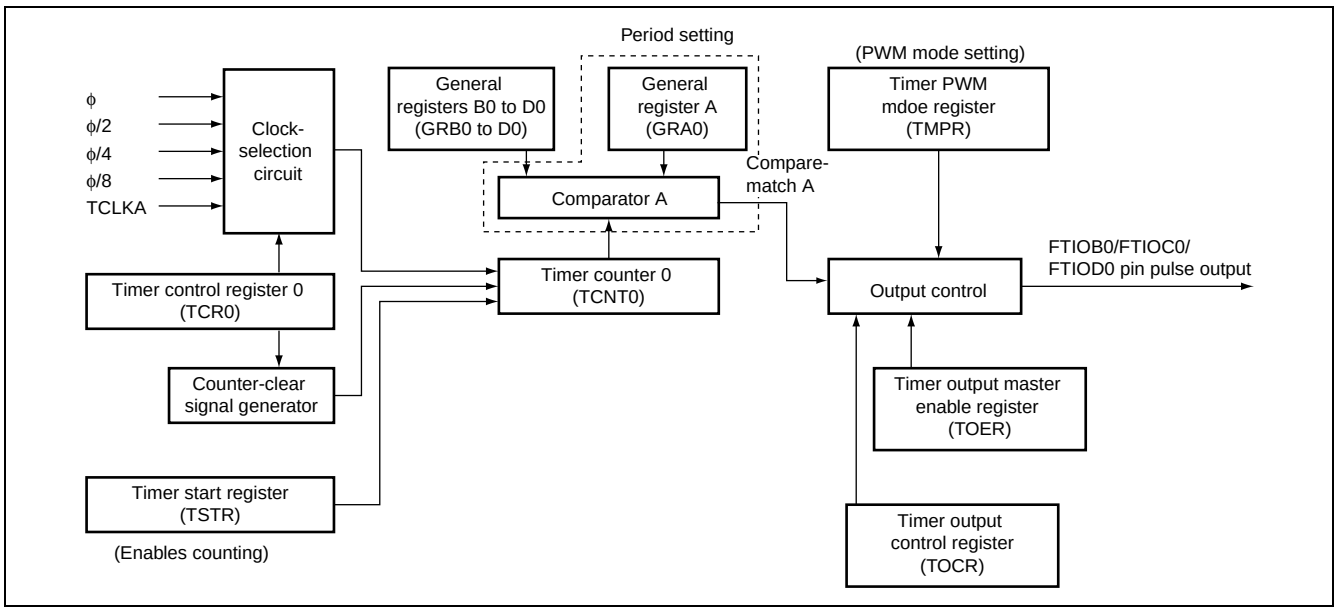


Figure 2.1 Timer Z Channel 0 Block Diagram

2. Table 2.1 shows the function assignments for this task. The three PWM waveforms are output by assigning the timer Z functions to the pins and registers indicated in table 2.1.

Table 2.1 Function Assignments

Pin and Register Name	Assigned Function
FTIOB0	Pulse-output pins
FTIOC0	
FTIOD0	
TSTR	Enables and disables counting by the channel 0 timer.
TCR0	Selects the input clock for the channel 0 timer counter and the condition that drives clearing of the counter.
TMPR	Specifies the PWM mode.
TOCR	Specifies the initial output until the first compare-match occurs.
TOER	Enables and disables the timer output.
GRA0	Specifies the output pulse cycle.
GRB0	Specifies the timing of the level change in the pulse to be output from the FTIOB0 pin.
GRC0	Specifies the timing of the level change in the pulse to be output from the FTIOC0 pin.
GRD0	Specifies the timing of the level change in the pulse to be output from the FTIOD0 pin.
TCNT0	Channel 0 timer counter

3. Description of Operation

Figure 3.1 shows the operational principle. Hardware and software processing by the H8/3687 are applied in the way shown in figure 3.1 to produce three PWM waveforms.

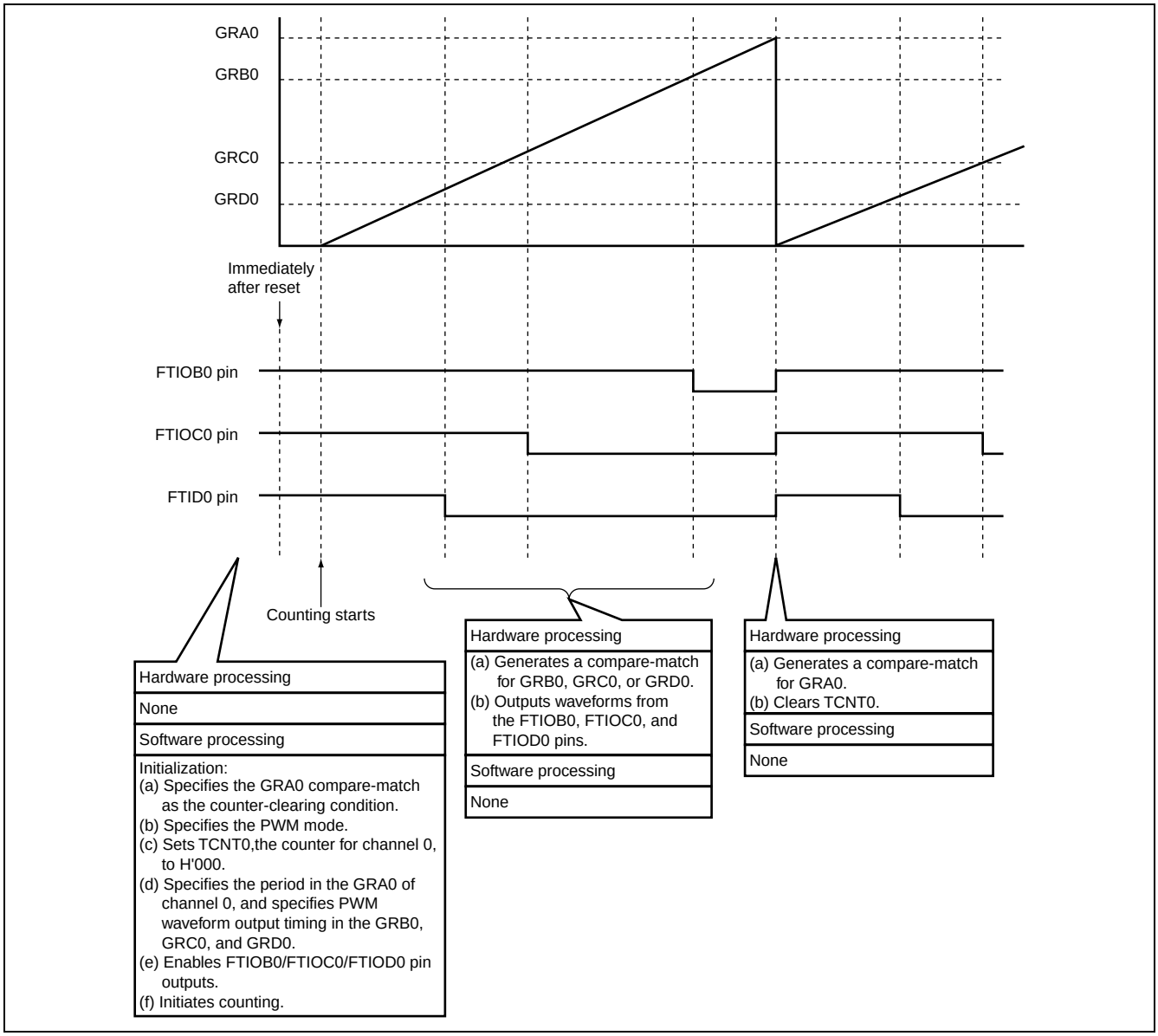


Figure 3.1 Operational Principle for the Output of Three PWM Signals

4. Software Description

4.1 Module

Module Name	Label Name	Assigned Function
Main routine	Main	Specifies the timing of the level changes in the three output pulse waveforms in GRB0, GRC0, and GRD0 and specifies the period for the waveforms in GRA0.

4.2 Arguments

No argument is used in this sample task.

4.3 Internal registers used

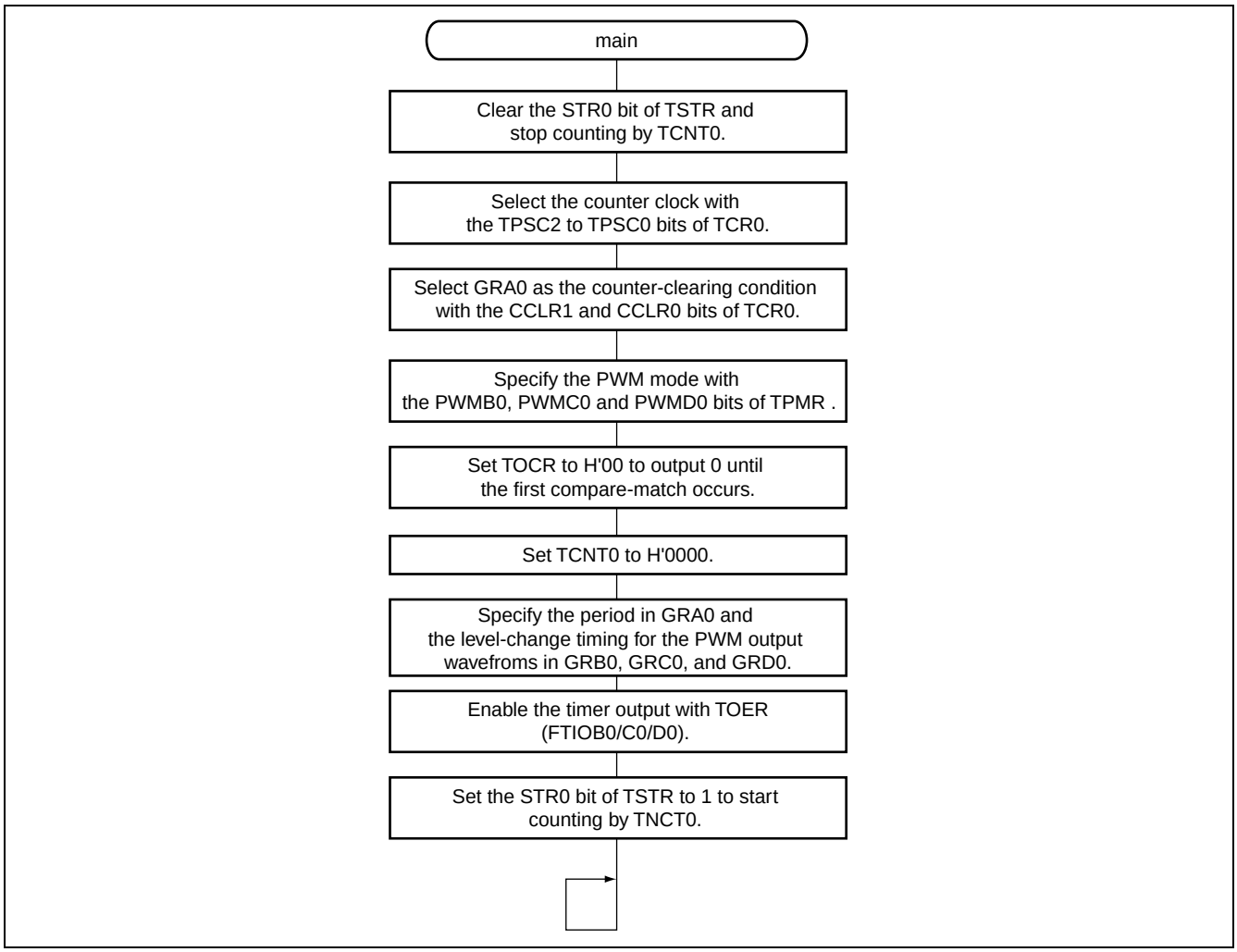
Pin and Register Names	Assigned Function
TSTR	Enables/disables the operation of timer channels 0 and 1.
TCR0	Selects the condition that drives clearing of timer channel 0 and the channel's input clock.
TMPR	Specifies the PWM mode.
TOCR	Specifies the initial output until the first compare-match occurs.
TOER	Enables and disables timer-driven output.
GRA0	Specifies the output pulse cycle.
GRB0	Specifies the timing of the level change in one of the PWM output waveforms.
GRC0	Specifies the timing of the level change in one of the PWM output waveforms.
GRD0	Specifies the timing of the level change in one of the PWM output waveforms.
TCNT0	Channel 0 timer counter

4.4 RAM used

This sample task uses no RAM.

5. Flowchart

1. Main routine



6. Program Listing

```
/************************************************************/
/*                                                          */
/*    H8/300HN Series -H8/3687-                             */
/*    Application Note                                      */
/*                                                          */
/*    PWM Mode                                              */
/*                                                          */
/*    Function                                              */
/*     Timer Z PWM Mode                                     */
/*                                                          */
/*    External Clock : 16 MHz                               */
/*    Internal Clock : 16 MHz                               */
/*    Sub-clock      : 32.768 kHz                           */
/*                                                          */
/************************************************************/
#include    <C:\ch38\include\machine.h>

#include    <C:\ch38\include\machine.h>

/************************************************************/
/*    Symbol Definition                                     */
/************************************************************/

struct BIT {
    unsigned char b7:1;   /* bit7 */
    unsigned char b6:1;   /* bit6 */
    unsigned char b5:1;   /* bit5 */
    unsigned char b4:1;   /* bit4 */
    unsigned char b3:1;   /* bit3 */
    unsigned char b2:1;   /* bit2 */
    unsigned char b1:1;   /* bit1 */
    unsigned char b0:1;   /* bit0 */
};

#define          TCR0    *(volatile unsigned char *)0xF700     /* Timer Control Register 0             */
#define          TIORA0  *(volatile unsigned char *)0xF701     /* Timer I/O Control Register A0        */
#define          TIORC0  *(volatile unsigned char *)0xF702     /* Timer I/O Control Register C0        */
#define          TSR0    *(volatile unsigned char *)0xF703     /* Timer Status Register 0              */
```

```
#define           TSR0_BIT (*(struct BIT *)0xF703)              /* Timer Status Register 0               */
#define           IMIFA_0  TSR0_BIT.b0                          /* Input Capture/Compare match Flag A    */
#define           TIER0    *(volatile unsigned char *)0xF704    /* Timer Interrupt Enable Register 0     */
#define           POCR0    *(volatile unsigned char *)0xF705    /* Port Output Level Control Register    */
#define           TCNT0    *(volatile unsigned short *)0xF706   /* Timer Counter 0                       */
#define           GRA0     *(volatile unsigned short *)0xF708   /* General Register A0                   */
#define           GRB0     *(volatile unsigned short *)0xF70A   /* General Register B0                   */
#define           GRC0     *(volatile unsigned short *)0xF70C   /* General Register C0                   */
#define           GRD0     *(volatile unsigned short *)0xF70E   /* General Register D0                   */

#define           TCR1     *(volatile unsigned char *)0xF710    /* Timer Control Register 1              */
#define           TIORA1   *(volatile unsigned char *)0xF711    /* Timer I/O Control Register A1         */
#define           TIORC1   *(volatile unsigned char *)0xF712    /* Timer I/O Control Register C1         */
#define           TSR1     *(volatile unsigned char *)0xF713    /* Timer Status Register 1               */
#define           TIER1    *(volatile unsigned char *)0xF714    /* Timer Interrupt Enable Register 0     */
#define           POCR1    *(volatile unsigned char *)0xF715    /* Port Output Level Control Register    */
#define           TCNT1    *(volatile unsigned short *)0xF716   /* Timer Counter 1                       */
#define           GRA1     *(volatile unsigned short *)0xF718   /* General Register A1                   */
#define           GRB1     *(volatile unsigned short *)0xF71A   /* General Register B1                   */
#define           GRC1     *(volatile unsigned short *)0xF71C   /* General Register C1                   */
#define           GRD1     *(volatile unsigned short *)0xF71E   /* General Register D1                   */

#define           TSTR     *(volatile unsigned char *)0xF720    /* Timer Start Register                  */
#define           TMDR     *(volatile unsigned char *)0xF721    /* Timer Mode Register                   */
#define           TPMR     *(volatile unsigned char *)0xF722    /* Timer PWM Mode Register               */
#define           TFCR     *(volatile unsigned char *)0xF723    /* Timer Function Control Register       */
/************************************************************/
/* Function definition                                      */
/************************************************************/
extern    void    INIT ( void );                               /* SP Set                                */
void      main     ( void );

extern void _INITSCT();

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                                 /* VECTOR SECTION SET                    */
void (*const VEC_TBL1[])(void) = {                            /* 0x00 - 0x0f                           */
    INIT                                                      /* 00 Reset                              */
```

```
};

#pragma    section                                          /* P                                    */
/******************************************************************/
/*    Main Program                                          */
/******************************************************************/
void main ( void )
{
    _INITSCT();

    set_imask_ccr(1);                                     /* Disable interrupts                   */

    TSTR = 0xFC;                                          /* Stop the timer                       */
    TOCR = 0x00;                                          /* PWM initial output "0"               */
    TPMR = 0x8F;                                          /* FTIOB0, FTIOC0, FTIOD0 PWM Mode      */

    TCR0 = 0x20;                                          /* GRA Compare-match Clear Mode         */
    POCR0 = 0xFF;                                         /* FTIOB0, FTIOC0, FTIOD0 active high   */

    GRA0 = 0x320;                                         /* Cycle 50 us                          */
    GRB0 = 0x230;                                         /* Duty cycle 30%                       */
    GRC0 = 0x230;                                         /* Duty cycle 30%                       */
    GRD0 = 0x230;                                         /* Duty cycle 30%                       */

    TOER = 0xF1;                                          /* Enable output on FTIOB0, FTIOC0, FTIOD0*/

    TSTR = 0xFD;                                          /* Start TCNT0                          */

    set_imask_ccr(0);                                     /* Enable interrupts                    */

    while(1)    {
       ;
       }
}
```

INIT (Program Listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
  ;
      .SECTION    P,CODE
  _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
  ;
      .END
```

Link address specification

Section Name	Address
CV1	H'0000
P	H'0100
B	H'F780