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H8/300H Super Low Power Series

Pulse-Frequency Measurement Using the Event-Counter Function of Timer C

Introduction

Event counter function of timer C is used to measure pulse-frequency input from timer C event input (TMIC) pin.

Target Device

H8/38099

Contents

1. Specifications

1. Event counter function of timer C is used to measure pulse-frequency input from timer C event input (TMIC) pin.
2. Number of times of rising edge detection for pulse which is input from the TMIC input pin is counted for one second, and the counted numbers are stored in RAM.
3. A one-second time-interval is measured by the clock operation of the realtime clock (RTC).
4. Connecting the UD pin to GND makes the Timer C counter (TCC) function as an up-counter.

2. Description of Functions Used

2.1 Block Diagram of Timer C

Figure 1 shows the block diagram of the timer C event counter function.

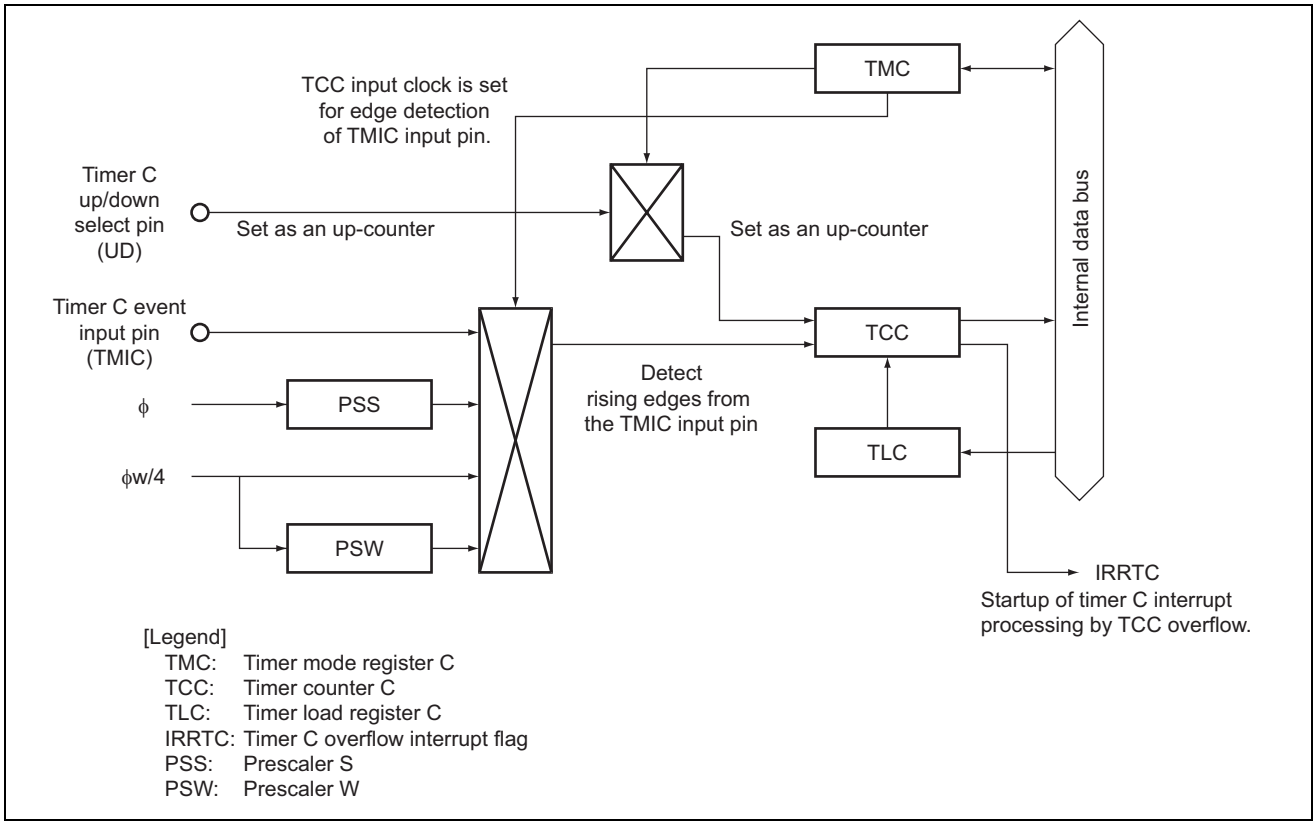


Figure 1 Block Diagram of Timer C Function

2.2 Functions Used

2.2.1 Description of Functions

In this sample task, event counter function of timer C is used to measure pulse-frequency input from TMIC input pin. Details on the functions are described below. For details on individual registers will be explained in section 4.3, “Internal Registers”.

- Timer Mode Register C (TMC)
  Timer Mode Register C (TMC) is an 8-bit read/write register used to select the auto-reload function, control selection of counting up or down of Timer Counter C (TCC), and select input clock. That is, it determines whether selection of counting up or down by TCC is controlled by hardware (through the signal level on the UD pin) or, if not, whether TCC functions as an up-counter or down-counter. On a reset, TMC is initialized to H'10.

- Timer Counter C (TCC)
  Timer Counter C (TCC) is an 8-bit read-only up/down counter, which is incremented or decremented by internal clock or external event input. The clock to be input can be selected from a total of 10 types, six of which are derived from the system clock divided by 8192, 2048, 512, 64, 16 and 4, three of which are derived from the sub-clock divided by 1024, 256 and 4, and one of which is the external clock. In this sample task, the edge detection of the TMIC input pin is selected as the TCC input clock.

- Timer C Interrupt Request Flag (IRRTC)
  Timer C Interrupt Request Flag (IRRTC) is set to 1 by a TCC overflow event. If, on the provision that IRRTC has been set to 1, Timer C Interrupt Enable (IENTC) of the Interrupt Enable Register 2 (IENR2) is set to 1, and the I bit of the Condition Code register (CCR) is cleared to 0, the Timer C interrupt sequence will start on reception of the Timer C interrupt.

- Timer C Event Input Pin (TMIC)
  Timer C Event Input Pin (TMIC) functions as the input pin for the pulse stream that will be subject to the frequency measurements.

2.2.2 Description of the method of frequency measurement using the event counter function of Timer C

The following describes how the event counter function of timer C is used to measure frequency in this sample task.

- In the user RAM area, set cnt1 to count the number of timer C interrupts, and set cnt2 to save the counter value of timer counter C when one second elapses.
- When 256 rising-edge input pulse events have been applied to the TMIC input pin, TCC overflows and a Timer C interrupt is generated.
- The counter set by cnt1 is incremented during the Timer C interrupt sequence.
- The count value in TCC is read out and stored in cnt2 after an interval of one second has elapsed, at which point the TCC increment sequence by the signal applied from the TMIC input pin is stopped.
- The frequency of the pulse applied to the TMIC input pin can be found by using the following expression:

  Input Pulse Frequency (Hz)
  = (Timer C Interrupt Event Count) x 256 + (Count Value in TCC after one second elapses)
  = (Value in cnt1) x 256 + (Value in cnt2)

- Since cnt1 is an 8-bit counter, the maximum frequency of the input pulse that can be measured is 65.535 kHz.
- Frequency measurements are stopped at the instant when cnt1 changes from H'FF to H'00, and the sequence is finished by writing H'00 to cnt1 and cnt2.

2.2.3 Description of Realtime Clock (RTC)

The following describes the realtime clock (RTC).

- RTC Control Register 1 (RTCCR1)
  RTC Control Register 1 (RTCCR1) controls start/stop and reset of the clock timer.
- RTC Control Register 2 (RTCCR2)
  RTC Control Register 2 (RTCCR2) controls RTC periodic interrupt of one second. Enabling interrupt of one second sets the corresponding flag to 1 in the RTC interrupt flag register (RTCFLG) when an interrupt occurs.
- Clock Source Select Register (RTCCSR)
  Clock Source Select Register (RTCCSR) selects clock source. In this sample task, the 32.768-kHz clock signal for RTC operation is selected as the clock source.
- RTC Interrupt Flag Register (RTCFLG)
  RTC Interrupt Flag Register (RTCFLG) sets the corresponding flag when an interrupt occurs. Even when an interrupt is accepted, the corresponding flag is not cleared automatically. To clear the flag, 0 should be written to the flag.

2.2.4 Watchdog Timer Function

H8/38099 incorporates a watchdog timer (WDT) that is turned on by default after a reset. The WDT is an 8-bit timer that can generate an internal reset signal when the timer counter overflows because a system crash has prevented the CPU from writing to it. In this sample task, the WDT function is not used, so it is turned off.

- Timer Control/Status Register WD1 (TCSRWD1)
  Timer Control/Status Register WD1 (TCSRWD1) performs TCSRWD1 and TCWD write control. TCSRWD1 also controls the watchdog timer operation and indicates the operating state. TCSRWD1 must be rewritten by using the MOV instruction. Bit-manipulation instructions cannot be used to change the setting.

2.3 Assignment of Functions

Table 1 lists the assignment of functions applicable to this sample task. The functions are assigned as indicated in table 1. Frequency measurement is performed by the event counter function.

Table 1 Assignment of Functions

Function	Assignment of Functions
TCC	This is an 8-bit up/down-counter to which edge detection for the TMIC input pin is input.
TMC	This is a register for selecting the auto-reload function and input clock, and performing up/down-counter control.
TLC	This sets the value for reloading when TCC overflows to H'00.
IRRTC	This reflects the presence/absence of a Timer C interrupt request.
IENTC	This enables a Timer C interrupt request.
RTCCR1	This controls start/stop and reset of the clock timer.
RTCCSR	This selects the 32.768 kHz clock signal for RTC operation as the clock source.
SEIFG	This reflects the presence/absence of a one-second periodic interrupt request.
1SEIE	This enables a one-second periodic interrupt request. (The function 1SEIE is changed to R1SEIE to be used for the source program of this application note.)
IENRTC	This enables a RTC interrupt request.
PMRE	This selects the TMIC-input and UD pin functions.
TMIC	This is the input pin of the pulse subject to frequency measurement.
UD	This is connected to GND, setting TCC as an up-counter.
TCSRWD1	This stops the watchdog timer.

3. Principle of Operation

Figure 2 illustrates the principle of operation described by way of waveform diagram. As shown in figure 2, pulse-frequency measurements by means of the Timer C event counter function are facilitated by both hardware and software operations.

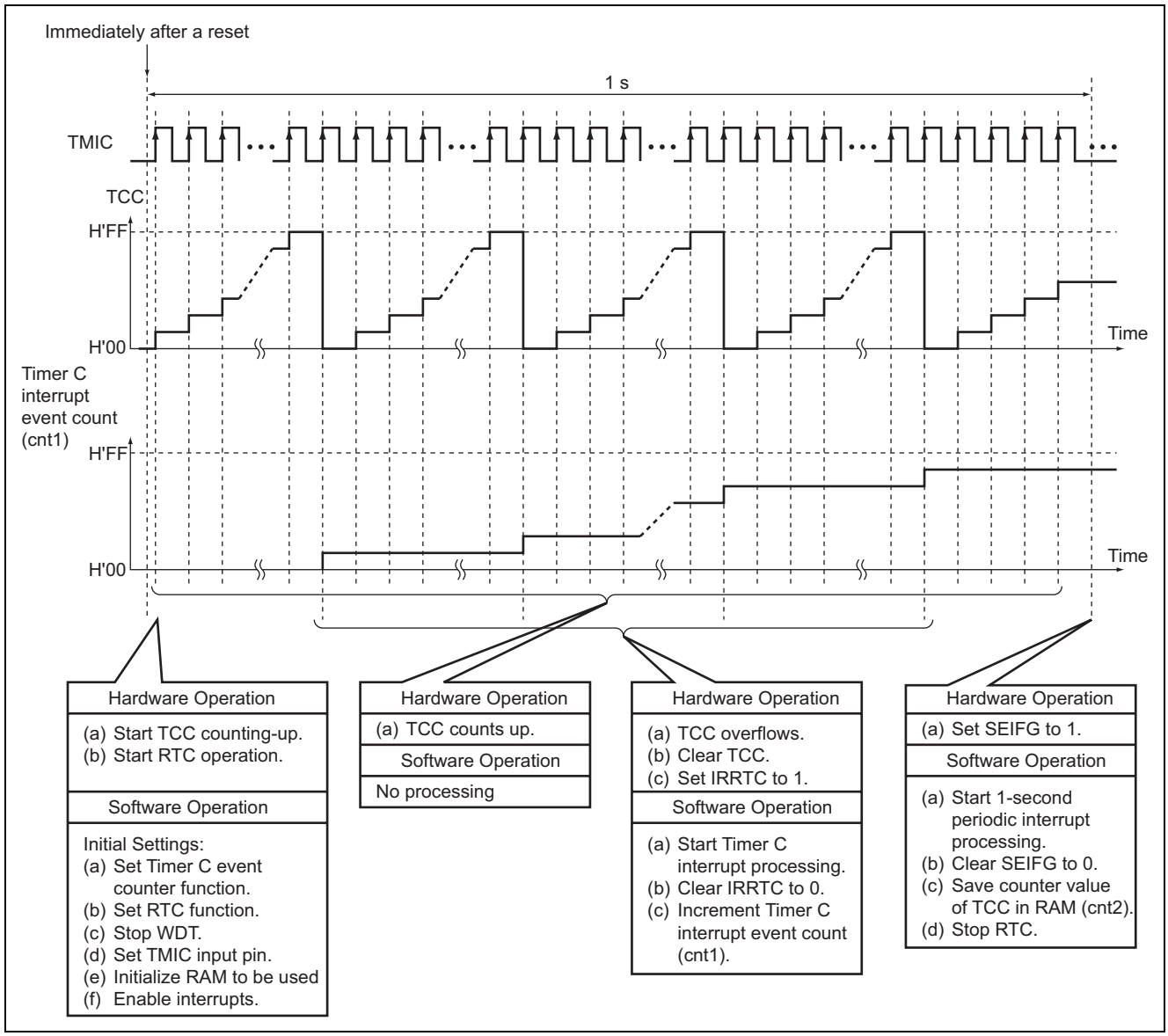


Figure 2 Principle of Operation in Frequency Measurement by the Timer C Event Counter Function

4. Description of Software

4.1 Modules

The modules applicable to this sample task are listed in table 2.

Table 2 Description of Modules

Module Name	Label Name	Function
Main Routine	main	The main routine sets timer C to the event counter function, sets the realtime clock and the WDT functions and the RAM locations, selects the TMIC-input and UD pin functions, and enables interrupts.
Count up	tcint	The Timer C interrupt handler increments cnt1 and processes cnt1 overflows.
RTC Interrupt	rtcint	The rtcint routine disables interrupts when the RTC one-second interrupt indicates that one second has elapsed, and saves the value counted by TCC in cnt2.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers

The following tables list the internal registers used in this sample task.

- Timer Mode Register C (TMC) Address: H'FFFFB4

Bit	Bit Name	Setting Value	R/W	Description
7	TMC7	0	R/W	Auto-Reload Function Select Selects whether timer C is used as an interval timer or auto-reload timer. 0: Interval timer function 1: Auto-reload function
6	TMC6	1	R/W	Counter Up/Down Control Selects whether selection of counting up or down by TCC is controlled by hardware (through the signal level on the UD pin) or, if not, whether TCC functions as an up-counter or down-counter. 00: TCC is an up-counter 01: TCC is a down-counter 1x: Hardware control through the signal level on the UD pin UD pin input high: Down-counter UD pin input low: Up-counter
5	TMC5	0	R/W	
4	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
3	TMC3	1	R/W	Clock Select TMC3 to TMC0 select the clock input for TCC. For the counting of external events, either the rising or falling edge can be selected. x000: Internal clock counting on ϕ/8192 x001: Internal clock counting on ϕ/2048 x010: Internal clock counting on ϕ/512 x011: Internal clock counting on ϕ/64 x100: Internal clock counting on ϕ/16 0101: Internal clock counting on ϕ/4 0110: Internal clock counting on ϕ_W/1024 1101: Internal clock counting on ϕ_W/256 1110: Internal clock counting on ϕ_W/4 0111: Counting falling edges of external events (TMIC)* 1111: Counting rising edges of external events (TMIC)*
2	TMC2	0	R/W	
1	TMC1	0	R/W	
0	TMC0	0	R/W	

Legend:
x: Don't care

Note: * The TMIC bit in the port mode register E (PMRE) must be set to 1 before the TMC3 to TMC0 bits are set to B'x111.

- Timer Counter C (TCC) Address: H'FFFFB5

Bit	Bit Name	Setting Value	R/W	Description
7	TCC7	—	R	TCC is an 8-bit read-only up/down-counter, which is incremented or decremented by internal clock or external event input. The clock source for input to this counter is selected by bits TMC3 to TMC0 in the timer mode register C (TMC). TCC values can be read by the CPU at any time. When TCC overflows from H'FF to H'00 or to the value set in TLC, or underflows from H'00 to H'FF or to the value set in TLC, the IRRTC bit in IRR2 is set to 1. TCC is allocated to the same address as TLC. Upon reset, TCC is initialized to H'00.
6	TCC6	—	R	
5	TCC5	—	R	
4	TCC4	—	R	
3	TCC3	—	R	
2	TCC2	—	R	
1	TCC1	—	R	
0	TCC0	—	R	

- Timer Load Register C (TLC) Address: H'FFFFB5

Bit	Bit Name	Setting Value	R/W	Description
7	TLC7	0	W	TLC is an 8-bit write-only register for setting the reload value of timer counter C (TCC). When a reload value is set in TLC, the same value is loaded into timer counter C as well, and TCC starts counting up/down from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded into TCC. Accordingly, overflow/underflow period can be set within the range of 1 to 256 input clocks. The same address is allocated to TLC as to TCC. Upon reset, TLC is initialized to H'00.
6	TLC6	0	W	
5	TLC5	0	W	
4	TLC4	0	W	
3	TLC3	0	W	
2	TLC2	0	W	
1	TLC1	0	W	
0	TLC0	0	W	

- Interrupt Enable Register 1 (IENR1) Address: H'FFFFF3

Bit	Bit Name	Setting Value	R/W	Description
7	IENRTC	1	R/W	RTC Interrupt Request Enable The RTC interrupt request is enabled when this bit is set to 1.

- Interrupt Enable Register 2 (IENR2) Address: H'FFFFF4

Bit	Bit Name	Setting Value	R/W	Description
1	IENTC	1	R/W	Timer C Interrupt Request Enable The timer C interrupt request is enabled when this bit is set to 1.

- Interrupt Request Register 2 (IRR2) Address: H'FFFFF7

Bit	Bit Name	Setting Value	R/W	Description
1	IRRTC	1	R/W	Timer C Interrupt Request Flag [Setting condition] • The timer C overflow or underflow occurs. [Clearing condition] • Writing of 0 to this bit.

- RTC Control Register 1 (RTCCR1) Address: H'FFF06C

Bit	Bit Name	Setting Value	R/W	Description
7	RUN	1	R/W	RTC Operation Start 0: Stops RTC operation 1: Starts RTC operation
4	RST	0	R/W	Reset 0: Normal operation 1: Resets registers and control circuits except RTCCSR and this bit. This bit must always be cleared to 0 after it is set to 1.

- RTC Control Register 2 (RTCCR2) Address: H'FFF06D

Bit	Bit Name	Setting Value	R/W	Description
2	1SEIE*	1	R/W	One-Second Periodic Interrupt Enable 0: Disables a one-second periodic interrupt 1: Enables a one-second periodic interrupt

Note: * The function 1SEIE is changed to R1SEIE to be used for the source program of this application note.

- RTC Clock Source Select Register (RTCCSR) Address: H'FFF06F

Bit	Bit Name	Setting Value	R/W	Description
7	—	— /(0)	R	Reserved This bit cannot be modified.
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	Select a clock output from the TMOW pin when setting the TMOW bit in PMR3 to 1.
4	SUB32K	0	R/W	000: ϕ/4 010: ϕ/8 100: ϕ/16 110: ϕ/32 xx1: ϕ_W
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: ϕ/8 Free running counter operation
1	RCS1	0	R/W	0001: ϕ/32 Free running counter operation
0	RCS0	0	R/W	0010: ϕ/128 Free running counter operation 0011: ϕ/256 Free running counter operation 0100: ϕ/512 Free running counter operation 0101: ϕ/2048 Free running counter operation 0110: ϕ/4096 Free running counter operation 0111: ϕ/8192 Free running counter operation 1000: 32.768 kHz RTC operation 1001 to 1111: Setting prohibited

Legend:
x: Don't care

- RTC Interrupt Flag Register (RTCFLG) Address: H'FFF067

Bit	Bit Name	Setting Value	R/W	Description
2	SEIFG	0	R/W*	[Setting condition] • A one-second periodic interrupt occurs [Clearing condition] • 0 is written to SEIFG when SEIFG = 1

Note: * Only 0 can be written here, to clear the flag.

- Port Mode Register E (PMRE) Address: H'FFF03B

Bit	Bit Name	Setting Value	R/W	Description
4	TMIC	1	R/W	PE7/TMIC Pin Function Switch 0: PE7 I/O pin 1: TMIC input pin
2	UD	1	R/W	PE6/UD Pin Function Switch 0: PE6 I/O pin 1: UD input pin

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFFFB1

Bit	Bit Name	Setting Value	R/W	Description
7	B6WI	1	R/W	Bit 6 Write Inhibit The TCWE bit can be written only when the write value of the B6WI bit is 0. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable TCWD can be written when the TCWE bit is set to 1. When writing data to this bit, the write value for bit 7 must be 0.
5	B4WI	*	R/W	Bit 4 Write Inhibit The TCSRWE bit can be written only when the write value of the B4WI bit is 0. This bit is always read as 1.
4	TCSRWE	*	R/W	Timer Control/Status Register WD Write Enable The WDON and WRST bits can be written when the TCSRWE bit is set to 1. When writing data to this bit, the write value for bit 5 must be 0.
3	B2WI	*	R/W	Bit 2 Write Inhibit The WDON bit can be written only when the write value of the B2WI bit is 0. This bit is always read as 1.
2	WDON	*	R/W	Watchdog Timer On TCWD starts counting up when this bit is set to 1 and halts when the WDON bit is cleared to 0. [Setting condition] • A reset is made. • When 1 is written to the WDON bit and 0 to the B2WI bit while the TCSRWE bit is 1. [Clearing condition] • When 0 is written to the WDON bit and 0 to the B2WI bit while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Inhibit The WRST bit can be written only when the write value of the B0WI bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When TCWD overflows and an internal reset signal is generated [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the WRST bit and 0 to the B0WI bit while the TCSRWE bit is 1

Note: * These bits are manipulated so as to stop the watchdog timer. See the flowchart for the main routine.

4.4 RAM Usage

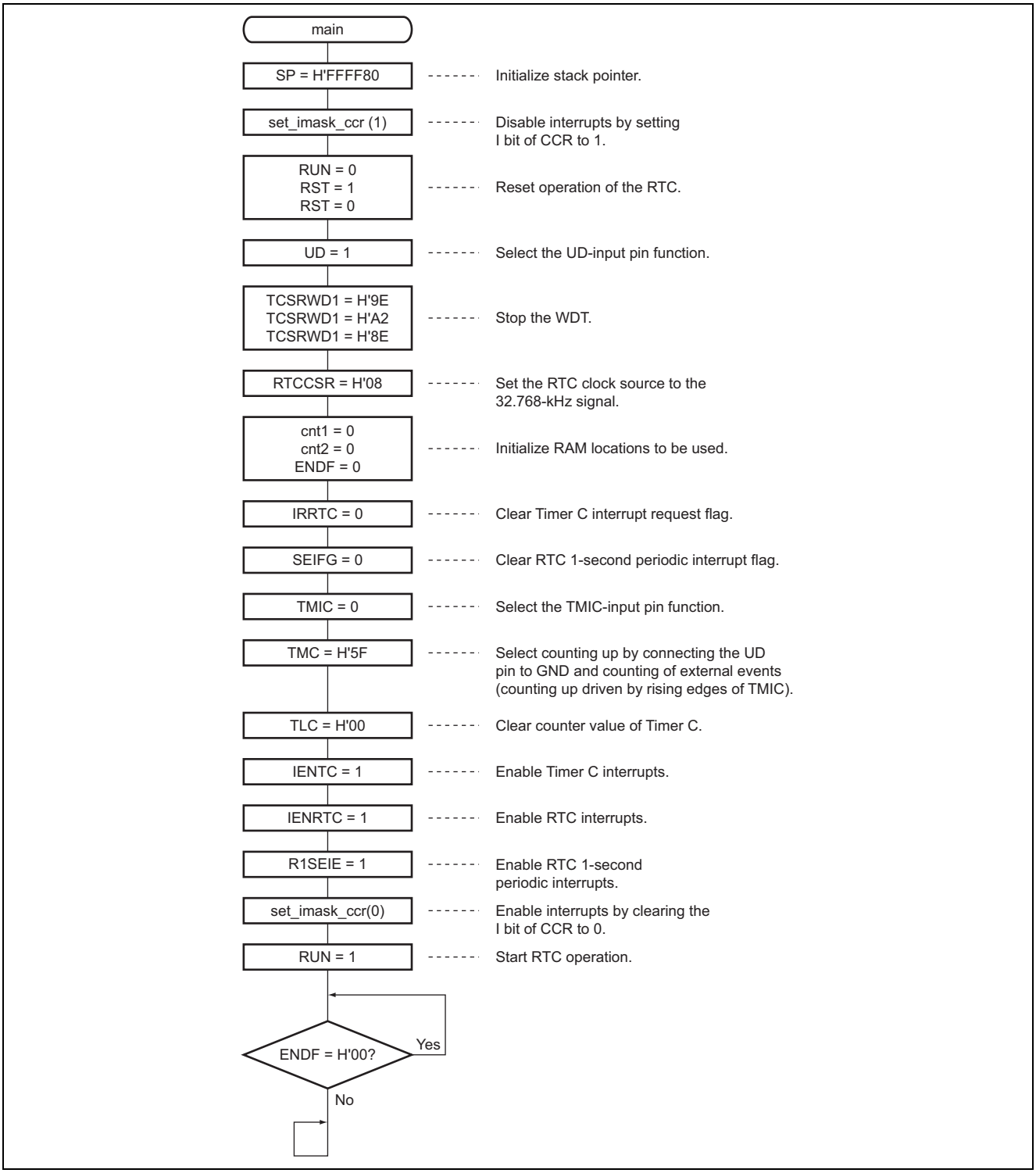
Table 3 lists and describes the RAM usage in this sample task.

Table 3 RAM Usage

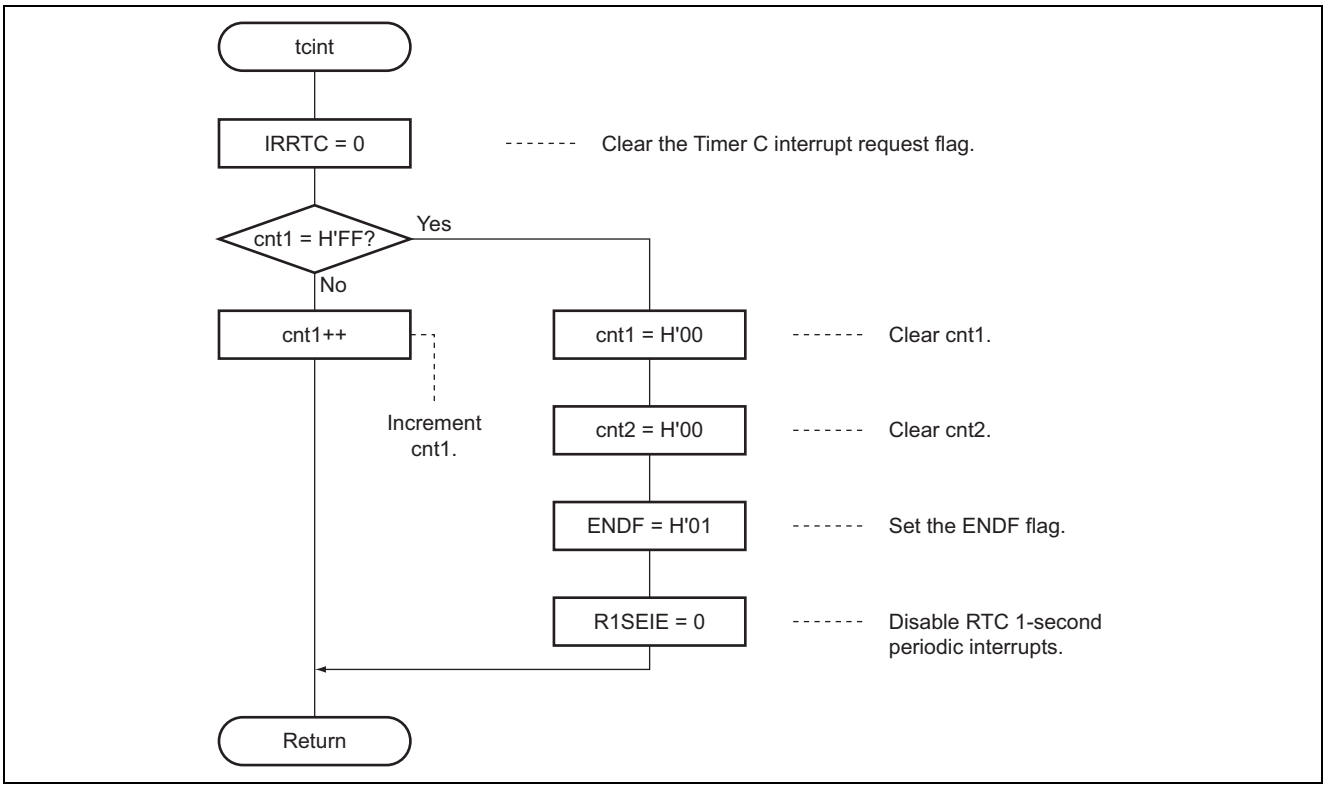
Type	Label Name	Description	Used in
unsigned char	cnt1	Counts how many times TCC-overflow interrupts are processed.	main
unsigned char	cnt2	Holds the counter value of TCC when one second elapses.	main, rtcint
unsigned char	ENDF	Flag used to determine whether or not input pulse frequency measurement is complete When measurement period is less than one second, and cnt1 < H'FF: ENDF = H'00. When one second of processing has elapsed, or cnt1 = H'FF: ENDF = H'01.	main, rtcint, tcint

5. Flowcharts

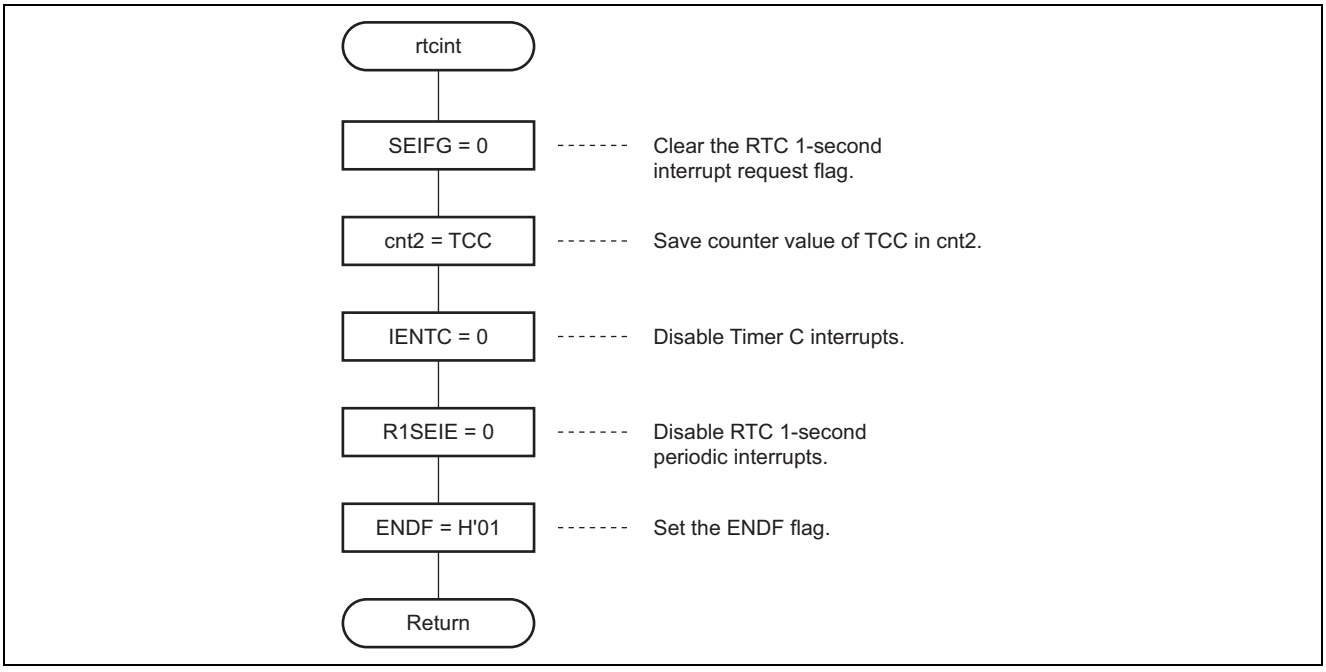
5.1 Function main



5.2 Function tcint



5.3 Function rtcint



6. Link Address Specifications

Section Name	Address
CV1	H'000000
CV2	H'000054
CV3	H'0000D4
P	H'000800
B	H'FFF380

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