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April 1st, 2010
Renesas Electronics Corporation

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M16C/62P Group

Procedure for Successive Serial I/O Transmission/Reception Using the DMAC

1. Abstract

This application note presents the procedure for successive serial I/O transmission/reception using the DMAC and an example on how to use it.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/62P Group

This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/62P microcomputers. However, some functions may have been modified.
Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Explanation of the Example Procedure

The example procedure selects serial I/O transmission (or reception) for the cause of request to the DMAC, and writes the next data to the transmit buffer (or reads from the receive buffer) at high speed in synchronism with the I/O transmission. This operation is performed successively as many times as the number of DMAC transfers needed.

3.1. Example Connection

Figure 1 shows an example device connection for successive transmission/reception.

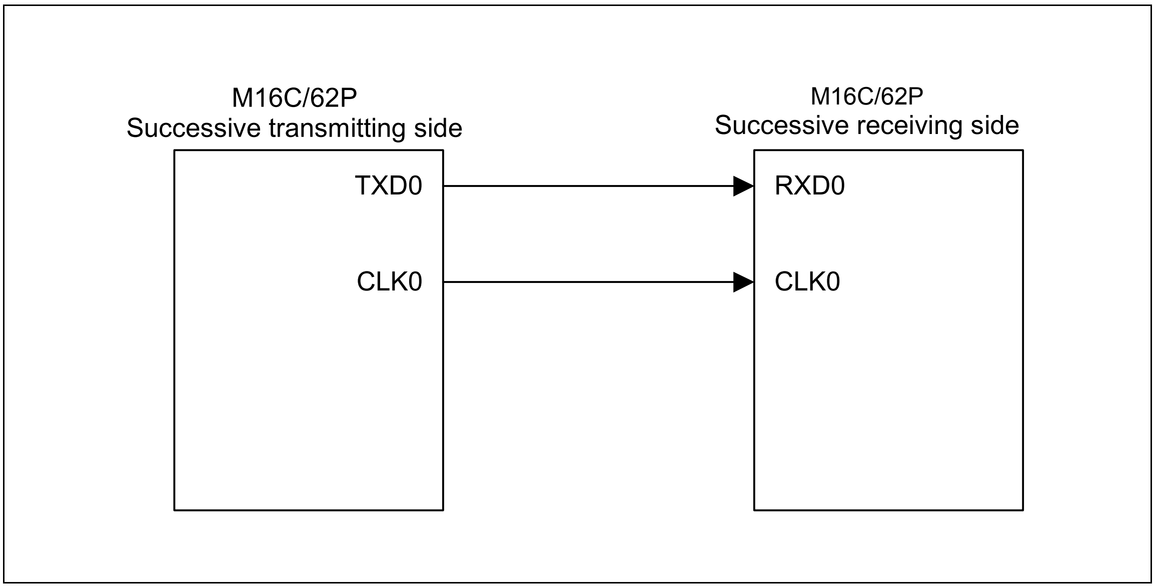


Figure 1. Example Connection for Successive Transmission/Reception

3.2. Setting Up Successive Transmission

The following shows how to set up the device for the case where 8 bytes of data are successively transmitted.

Usage Example:

- System
  VCC1=VCC2=5.0V, XIN=16MHz
- DMAC Setting
  DMA Request Factors=UART0 transfer, Single transfer, Transfer unit = 8 bits, Transfer source address direction=Forward direction, Transfer destination address direction=fixed (U0TB register)
- Serial I/O Setting
  Clock synchronous serial I/O mode, BRG count source = f1SIO, Bit Rates=62500bps (BRG=127), Transmit Interrupt Cause=Transmit buffer empty

Operation:
Specify UART0 transmission for the cause of request to the DMAC and after writing the first byte to the UART0 transmit buffer, transmit the remaining 7 bytes of data successively using a UART0 transmit interrupt request as a trigger. Figure 2 shows successive transmission/reception timing.

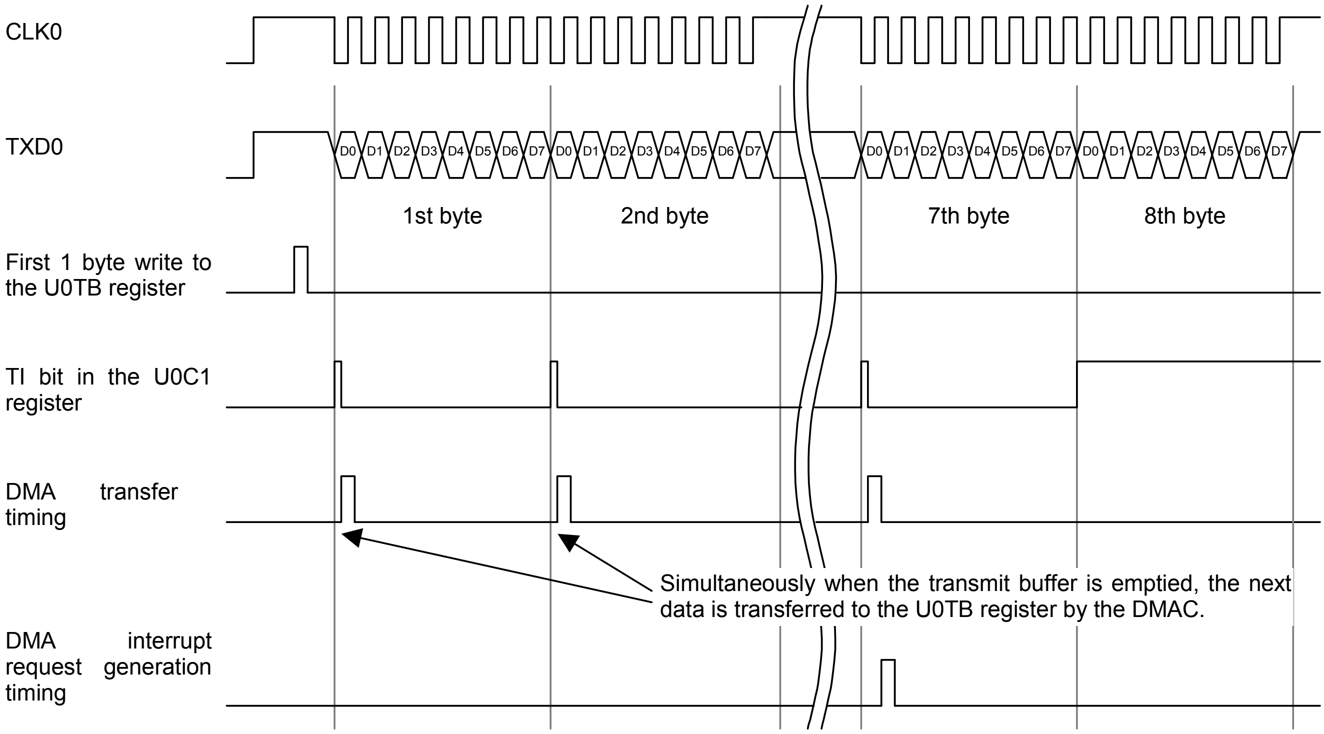
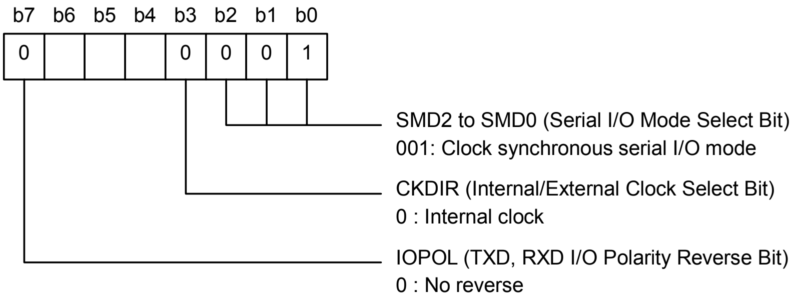

CLK0
TXD0
D0
D1
D2
D3
D4
D5
D6
D7
1st byte
2nd byte
7th byte
8th byte
First 1 byte write to the U0TB register
TI bit in the U0C1 register
DMA transfer timing
Simultaneously when the transmit buffer is emptied, the next data is transferred to the U0TB register by the DMAC.
DMA interrupt request generation timing

Figure 2. Successive Transmission/reception Timing

(1) Setting up the serial I/O

- Set up the U0MR register (UART0 transmit/receive mode register).



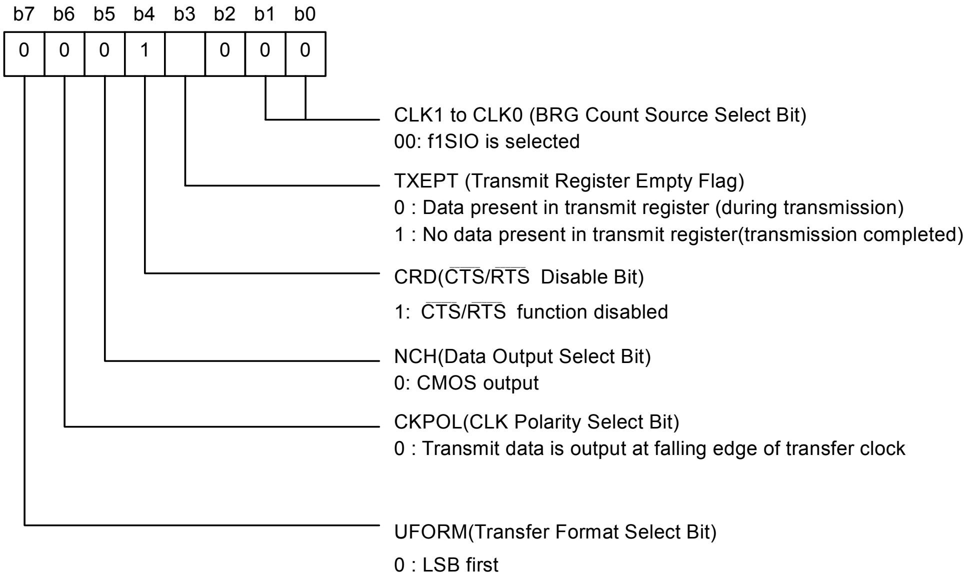
b7	b6	b5	b4	b3	b2	b1	b0
0				0	0	0	1

SMD2 to SMD0 (Serial I/O Mode Select Bit)
001: Clock synchronous serial I/O mode

CKDIR (Internal/External Clock Select Bit)
0 : Internal clock

IOPOL (TXD, RXD I/O Polarity Reverse Bit)
0 : No reverse

- Set up the U0C0 register (UART0 transmit/receive control register 0)



b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	1		0	0	0

CLK1 to CLK0 (BRG Count Source Select Bit)
00: f1SIO is selected

TXEPT (Transmit Register Empty Flag)
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register(transmission completed)

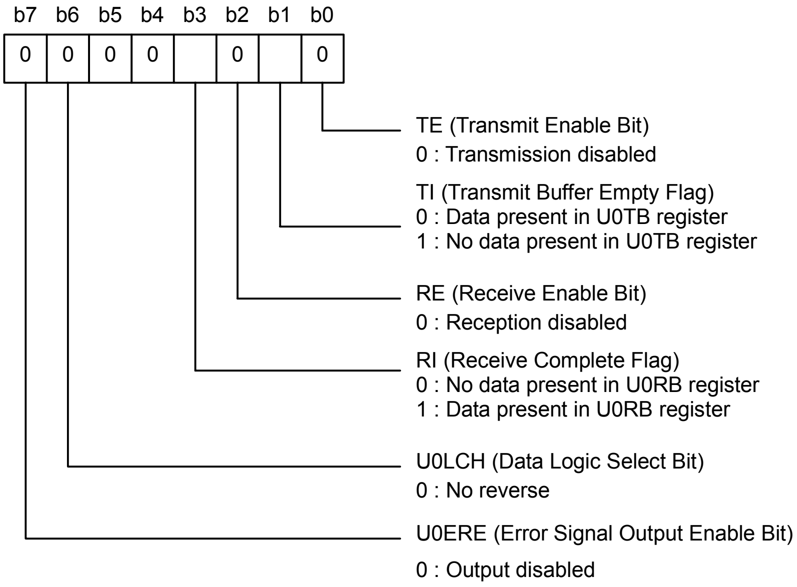
CRD($\overline{\text{CTS}}$/$\overline{\text{RTS}}$ Disable Bit)
1: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled

NCH(Data Output Select Bit)
0: CMOS output

CKPOL(CLK Polarity Select Bit)
0 : Transmit data is output at falling edge of transfer clock

UFORM(Transfer Format Select Bit)
0 : LSB first

- Set up the U0C1 register (UART0 transmit/receive control register 1)



b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0		0

TE (Transmit Enable Bit)
0 : Transmission disabled

TI (Transmit Buffer Empty Flag)
0 : Data present in U0TB register
1 : No data present in U0TB register

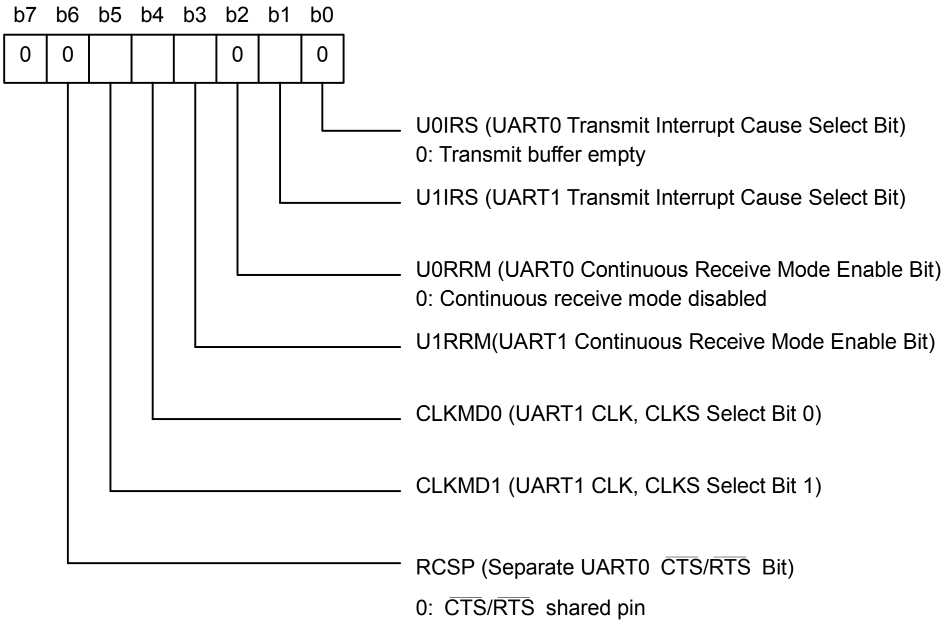
RE (Receive Enable Bit)
0 : Reception disabled

RI (Receive Complete Flag)
0 : No data present in U0RB register
1 : Data present in U0RB register

U0LCH (Data Logic Select Bit)
0 : No reverse

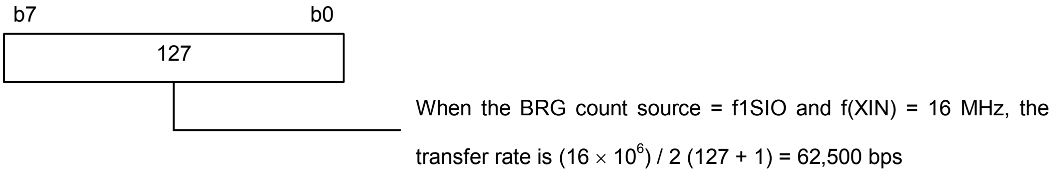
U0ERE (Error Signal Output Enable Bit)
0 : Output disabled

- Set up the UCON register (UART transmit/receive control register 2)

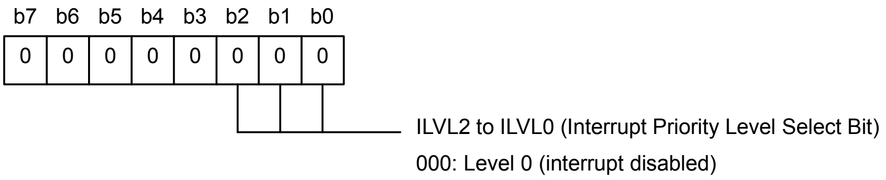

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0
U0IRS (UART0 Transmit Interrupt Cause Select Bit)
0: Transmit buffer empty
U1IRS (UART1 Transmit Interrupt Cause Select Bit)
U0RRM (UART0 Continuous Receive Mode Enable Bit)
0: Continuous receive mode disabled
U1RRM(UART1 Continuous Receive Mode Enable Bit)
CLKMD0 (UART1 CLK, CLKS Select Bit 0)
CLKMD1 (UART1 CLK, CLKS Select Bit 1)
RCSP (Separate UART0 $\overline{CTS}$/$\overline{RTS}$ Bit)
0: $\overline{CTS}$/$\overline{RTS}$ shared pin

- Set the U0SMR register (UART0 special mode register), U0SMR2 register (UART0 special mode register 2), U0SMR3 register (UART0 special mode register 3), and U0SMR4 register (UART0 special mode register 4) to “00h”.

- Set up the U0BRG register (UART0 bit rate generation register)

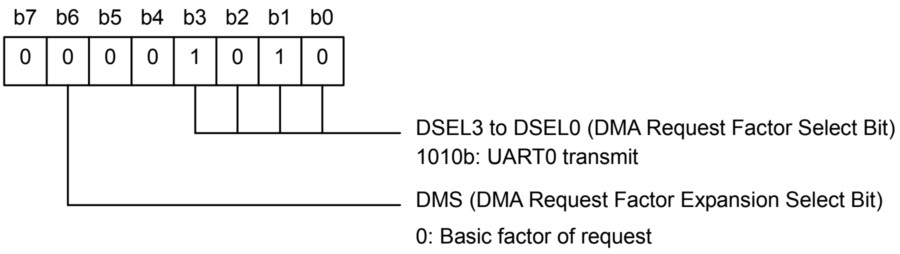

b7 b0
127
When the BRG count source = f1SIO and f(XIN) = 16 MHz, the
transfer rate is (16 × 10^6) / 2 (127 + 1) = 62,500 bps

- Set up the S0TIC register (UART0 transmit interrupt control register)


b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0 0
ILVL2 to ILVL0 (Interrupt Priority Level Select Bit)
000: Level 0 (interrupt disabled)

(2) Setting up the DMAC

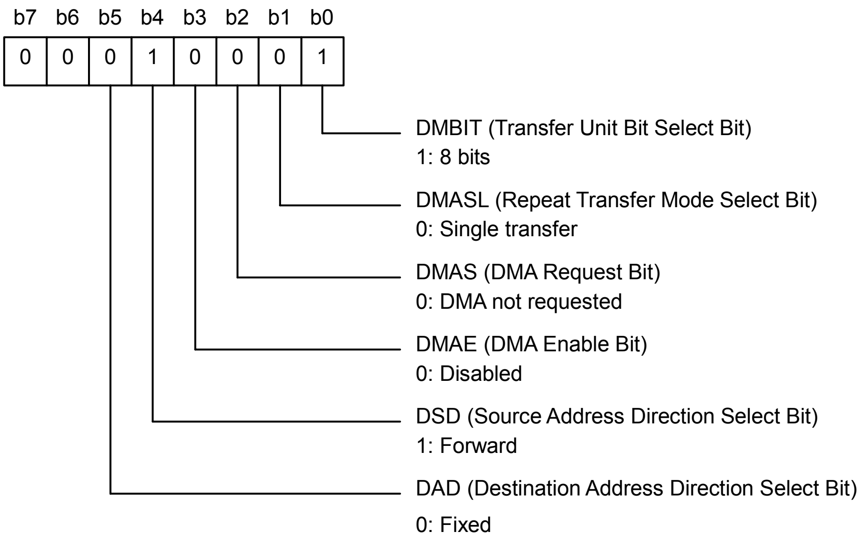
- Set up the DM0SL register (DMA0 request cause select register)



DSEL3 to DSEL0 (DMA Request Factor Select Bit)
1010b: UART0 transmit

DMS (DMA Request Factor Expansion Select Bit)
0: Basic factor of request

- Set up the DM0CON register (DMA0 control register)



DMBIT (Transfer Unit Bit Select Bit)
1: 8 bits

DMASL (Repeat Transfer Mode Select Bit)
0: Single transfer

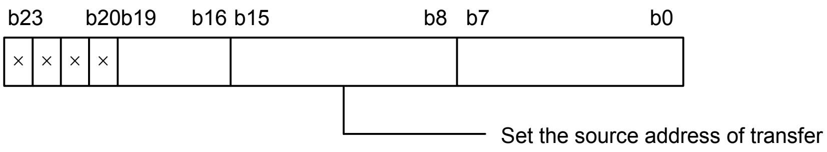
DMAS (DMA Request Bit)
0: DMA not requested

DMAE (DMA Enable Bit)
0: Disabled

DSD (Source Address Direction Select Bit)
1: Forward

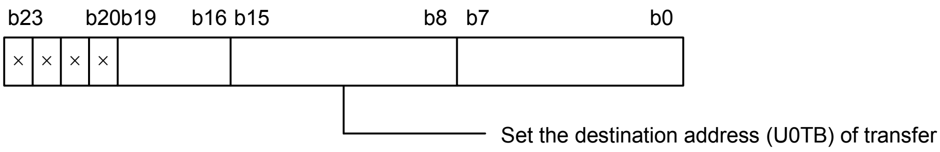
DAD (Destination Address Direction Select Bit)
0: Fixed

- Set up the SAR0 register (DMA0 source pointer)



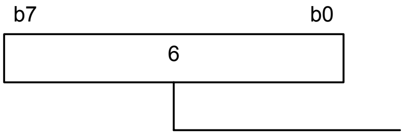
Set the source address of transfer

- Set up the DAR0 register (DMA0 destination pointer)



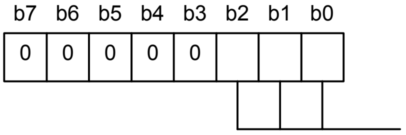
Set the destination address (U0TB) of transfer

- Set up the TCR0 register (DMA0 transfer counter)



Since the first byte of 8-byte successive transmission is written and then transferred to the U0TB register directly (not transferred by the DMAC), set the value “6” here so that 7 bytes will be transferred by DMA.

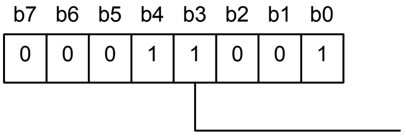
- Set up the DM0IC register (DMA0 interrupt control register)



ILVL2 to ILVL0 (Interrupt Priority Level Select Bit)
Set the interrupt priority level

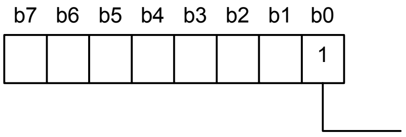
(3) Enables interrupt (I flag =“1”)

(4) Set up the DM0CON register (DMA0 control register) back again (to enable DMA)



DMAE (DMA Enable Bit)
1: Enable

(5) Enables transmit
Set the TE bit in the U0C1 register to “1” (transmit enable)



TE (Transmit Enable Bit)
1: Transmission enabled

(6) Starting successive transmissions
Write the first byte of successive transmit data to the U0TB register. Thereafter, the other bytes of data are successively transmitted by means of the DMAC transfer initiated by a UART0 transmit interrupt request until the count set in the DMA transfer counter expires.

(7) DMAC transfer complete interrupt processing
Set the DMAC transfer complete flag.

3.3. Setting Up Successive Reception

The following shows how to set up the device for the case where 8 bytes of data are successively received.

Usage Example:

- System
  VCC1=VCC2=5.0V, XIN=16MHz
- DMAC Setting
  DMA Request Factors=UART0 reception, Single transfer, Transfer unit = 16 bits (including an error flag), Transfer source address direction=fixed (U0RB register), Transfer destination address direction=Forward direction
- Serial I/O Setting
  Clock synchronous serial I/O mode, External clock (Note 1), Continuous receive mode enabled

Operation:
Specify UART0 reception for the cause of request to the DMAC and after a dummy read of the UART0 receive buffer, receive the data successively using a UART0 receive interrupt as a trigger. Figure 3 shows successive reception timing.

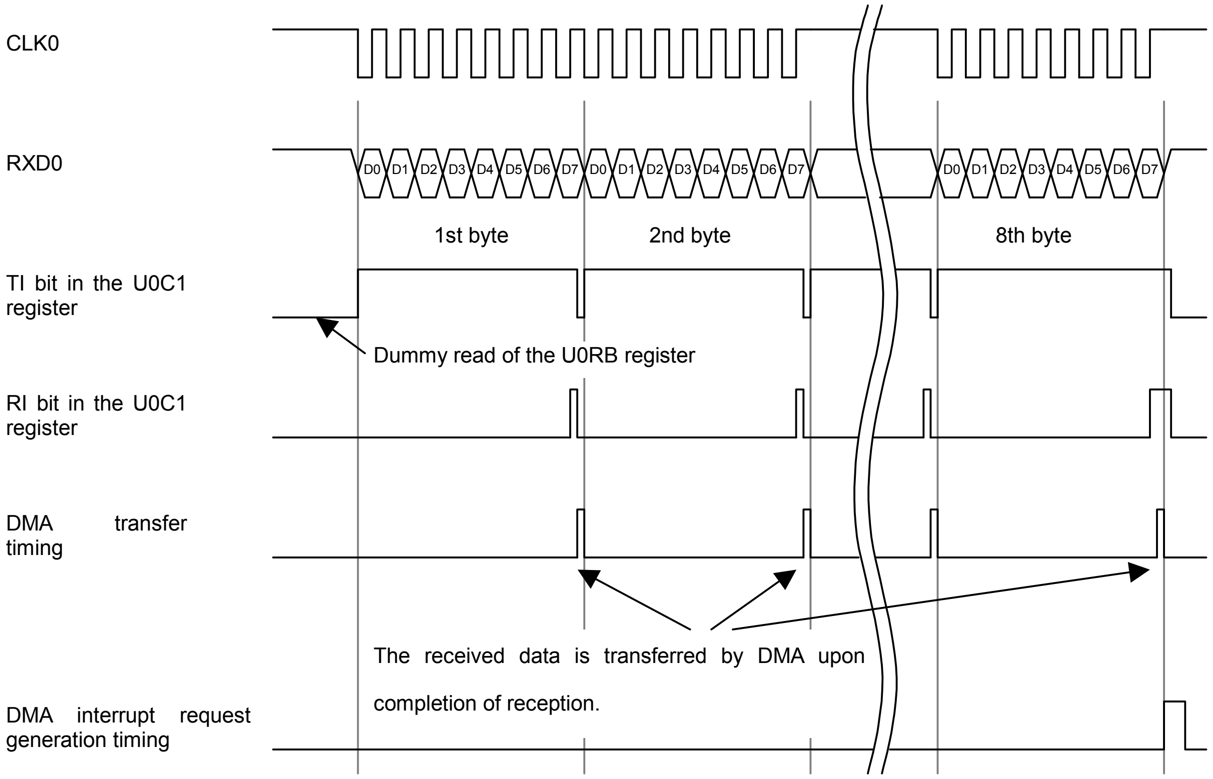
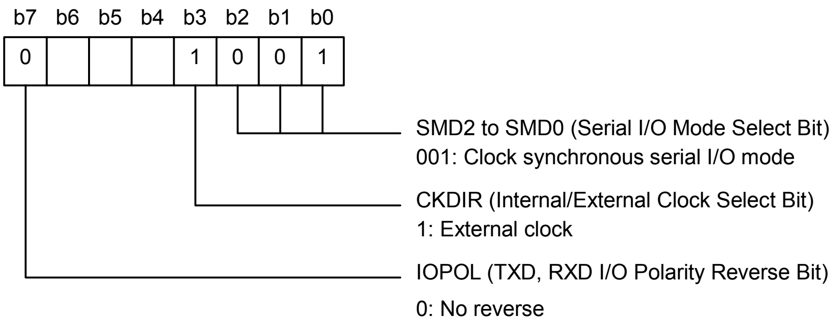

CLK0
RXD0
D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3 D4 D5 D6 D7
1st byte
2nd byte
8th byte
TI bit in the U0C1 register
Dummy read of the U0RB register
RI bit in the U0C1 register
DMA transfer timing
The received data is transferred by DMA upon completion of reception.
DMA interrupt request generation timing

Figure 3. Successive Reception Timing

Note 1:
When the input at the CLK0 pin before data reception is high (or low if the CKPOL bit in the U0C0 register = 1), the conditions described below must be met:
・TE bit in the U0C1 register = 1 (transmission enabled)
・RE bit in the U0C1 register = 1 (reception enabled)
・U0RB register is read

(1) Setting up Serial I/O

- Set up the U0MR register (UART0 transmit/receive mode register



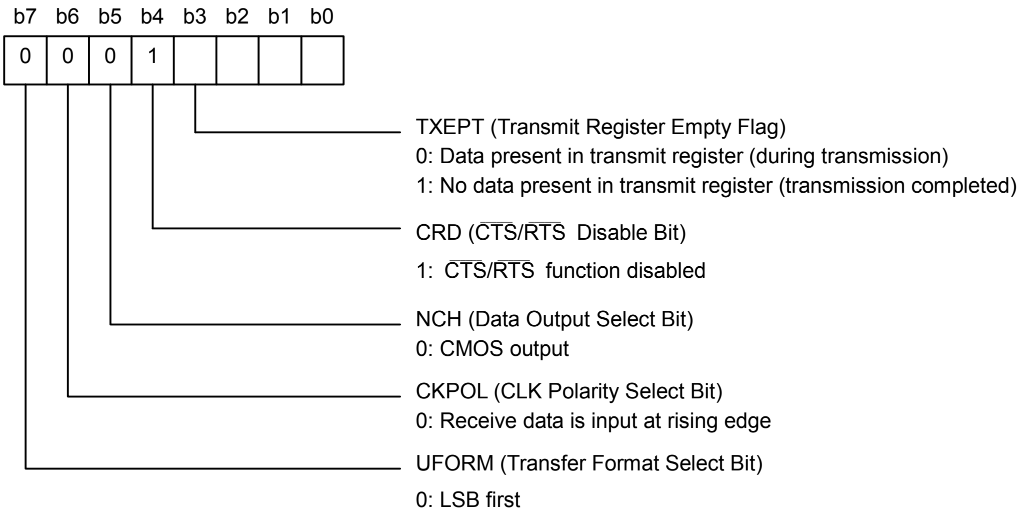
b7	b6	b5	b4	b3	b2	b1	b0
0				1	0	0	1

SMD2 to SMD0 (Serial I/O Mode Select Bit)
001: Clock synchronous serial I/O mode

CKDIR (Internal/External Clock Select Bit)
1: External clock

IOPOL (TXD, RXD I/O Polarity Reverse Bit)
0: No reverse

- Set up the U0C0 register ((UART0 transmit/receive control register 0)



b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	1				

TXEPT (Transmit Register Empty Flag)
0: Data present in transmit register (during transmission)
1: No data present in transmit register (transmission completed)

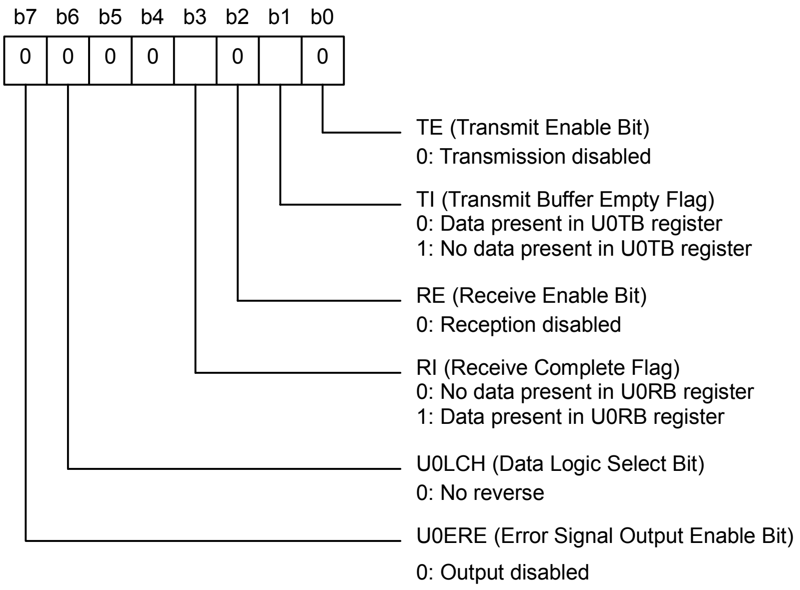
CRD ($\overline{\text{CTS}}$/$\overline{\text{RTS}}$ Disable Bit)
1: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled

NCH (Data Output Select Bit)
0: CMOS output

CKPOL (CLK Polarity Select Bit)
0: Receive data is input at rising edge

UFORM (Transfer Format Select Bit)
0: LSB first

- Set up the U0C1 register (UART0 transmit/receive control register 1)



b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0		0

TE (Transmit Enable Bit)
0: Transmission disabled

TI (Transmit Buffer Empty Flag)
0: Data present in U0TB register
1: No data present in U0TB register

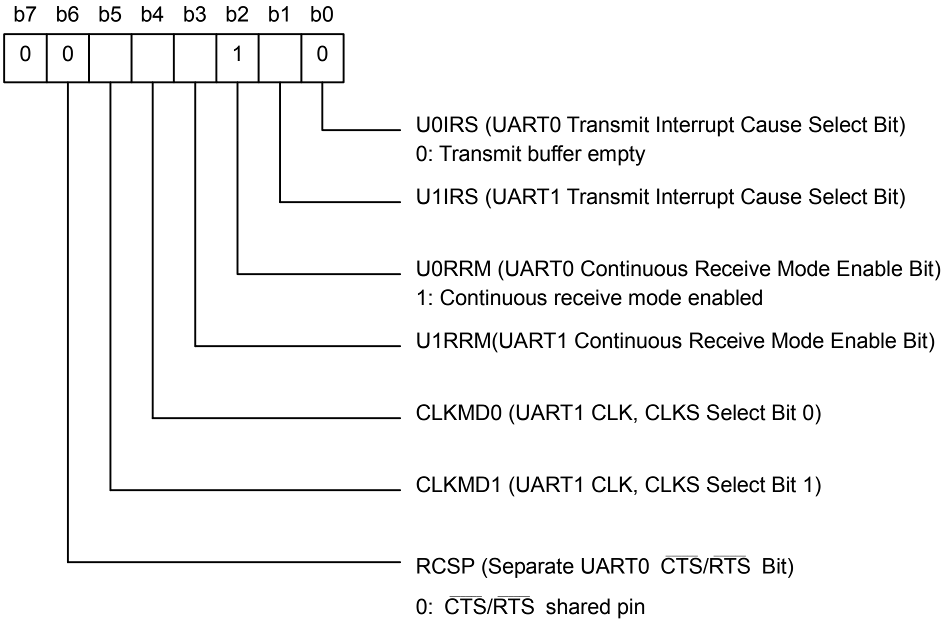
RE (Receive Enable Bit)
0: Reception disabled

RI (Receive Complete Flag)
0: No data present in U0RB register
1: Data present in U0RB register

U0LCH (Data Logic Select Bit)
0: No reverse

U0ERE (Error Signal Output Enable Bit)
0: Output disabled

- Set up the UCON register (UART transmit/receive control register 2)



U0IRS (UART0 Transmit Interrupt Cause Select Bit)
0: Transmit buffer empty

U1IRS (UART1 Transmit Interrupt Cause Select Bit)

U0RRM (UART0 Continuous Receive Mode Enable Bit)
1: Continuous receive mode enabled

U1RRM(UART1 Continuous Receive Mode Enable Bit)

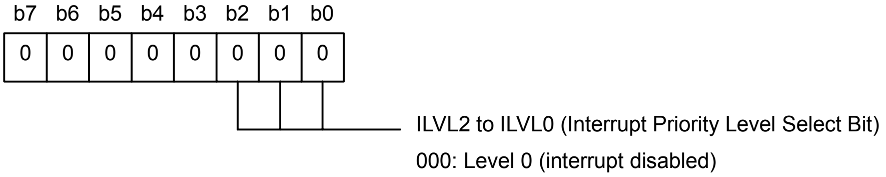
CLKMD0 (UART1 CLK, CLKS Select Bit 0)

CLKMD1 (UART1 CLK, CLKS Select Bit 1)

RCSP (Separate UART0 $\overline{CTS}$/$\overline{RTS}$ Bit)
0: $\overline{CTS}$/$\overline{RTS}$ shared pin

- Set the U0SMR register (UART0 special mode register), U0SMR2 register (UART0 special mode register 2), U0SMR3 register (UART0 special mode register 3), and U0SMR4 register (UART0 special mode register 4) to "00h".

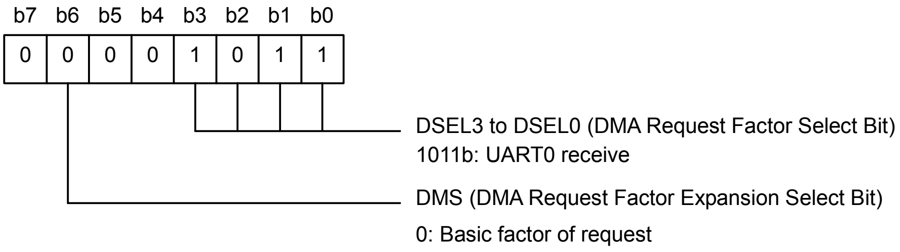
- Set up the S0RIC register (UART0 receive interrupt control register)



ILVL2 to ILVL0 (Interrupt Priority Level Select Bit)
000: Level 0 (interrupt disabled)

(2) Setting up the DMAC

- Set up the DM0SL register (DMA0 request cause select register)

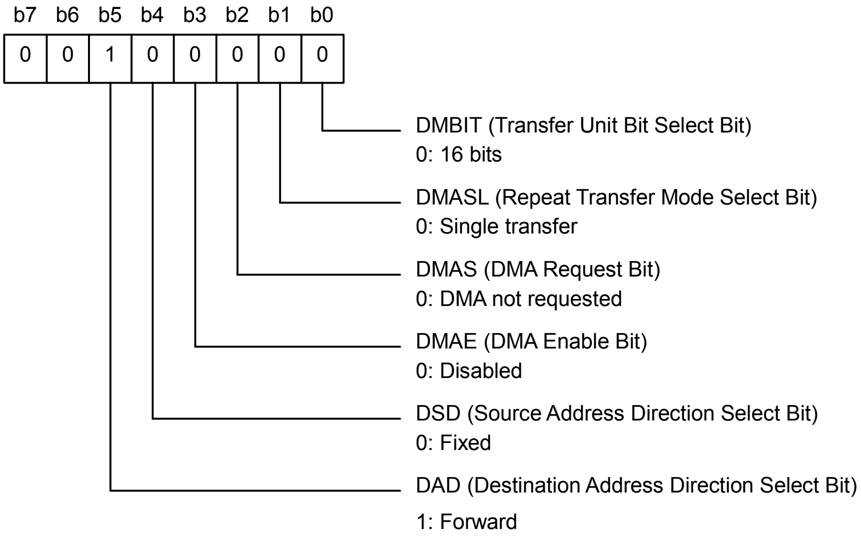


b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	1	0	1	1

DSEL3 to DSEL0 (DMA Request Factor Select Bit)
1011b: UART0 receive

DMS (DMA Request Factor Expansion Select Bit)
0: Basic factor of request

- Set up the DM0CON register (DMA0 control register)



b7	b6	b5	b4	b3	b2	b1	b0
0	0	1	0	0	0	0	0

DMBIT (Transfer Unit Bit Select Bit)
0: 16 bits

DMASL (Repeat Transfer Mode Select Bit)
0: Single transfer

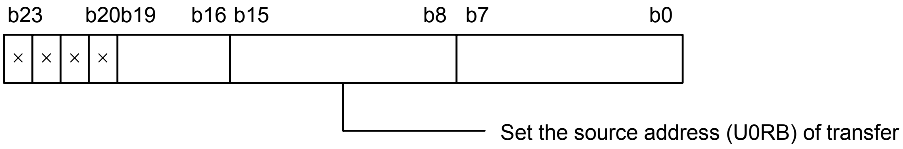
DMAS (DMA Request Bit)
0: DMA not requested

DMAE (DMA Enable Bit)
0: Disabled

DSD (Source Address Direction Select Bit)
0: Fixed

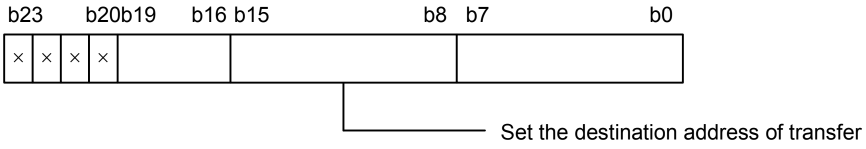
DAD (Destination Address Direction Select Bit)
1: Forward

- Set up the SAR0 register (DMA0 source pointer)



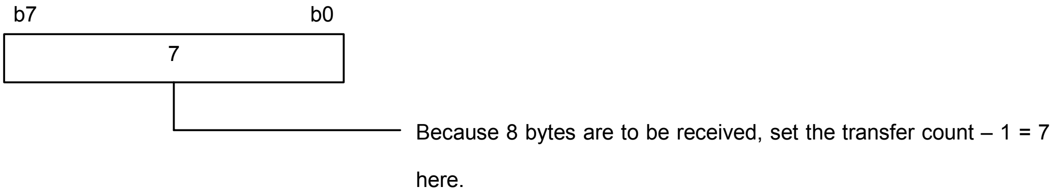
Set the source address (U0RB) of transfer

- Set up the DAR0 register (DMA0 destination pointer)



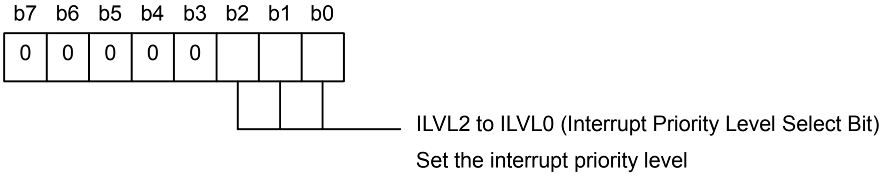
Set the destination address of transfer

- Set up the TCR0 register (DMA0 transfer counter)



Because 8 bytes are to be received, set the transfer count – 1 = 7 here.

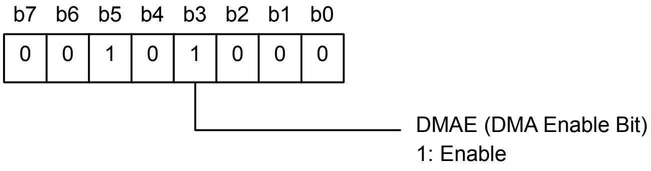
- Set up the DM0IC register (DMA0 interrupt control register)



ILVL2 to ILVL0 (Interrupt Priority Level Select Bit)
Set the interrupt priority level

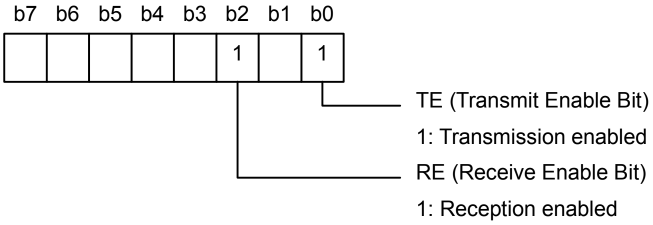
(3) Enables interrupt (I flag =“1”)

(4) Set up the DM0CON register (DMA0 control register) back again (to enable DMA)



DMAE (DMA Enable Bit)
1: Enable

(5) Enables transmit/receive
Set the TE and RE bits in the U0C1 register both to “1”, to enable transmission and reception.



TE (Transmit Enable Bit)
1: Transmission enabled
RE (Receive Enable Bit)
1: Reception enabled

(6) Starting successive reception
Access the U0RB register for dummy read to initiate successive reception.

(7) DMAC transfer complete interrupt processing
Check the received data for errors and, if necessary, reinitialize the serial I/O as error processing.

4. Example of a Sample Program

4.1. Example of a Successive Transmission Program

The following shows an example program for successively transmitting 8 bytes of data using the DMAC. Here, settings are made assuming the DMAC and serial I/O specifications shown below.

- DMAC Specification
  DMA Request Factors=UART0 transfer, Single transfer, Transfer unit = 8 bits, Transfer source address direction=Forward direction, Transfer destination address direction=fixed (U0TB register)
- Serial I/O Specification
  Clock synchronous serial I/O mode, CTS/RTS function disable, BRG count source = f1SIO, Bit Rates=62500bps (XIN=16MHz), Transmit Interrupt Cause=Transmit buffer empty

```
/***********************************************************************/
/*                                                          */
/*  M16C/62 Group Program Collection                             */
/*                                                          */
/*  FILE NAME : rjj05b0543_snd.c                                 */
/*  CPU       : M16C/62P Group                                 */
/*  FUNCTION  : The sample program of the serial I/O continuation     */
/*             transmission using DMAC.                         */
/*  HISTORY   : 2004.11.01 Ver 1.00                             */
/*                                                          */
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/*  All right reserved.                                        */
/*                                                          */
/***********************************************************************/

/****************************************/
/*    include file                     */
/****************************************/
#include "sfr62p.h"        // Special Function Register Header File

/****************************************/
/*    Function declaration              */
/****************************************/
void sio_init(void);       // Serial-I/O initialize routine
void dma_init(void);       // DMAC initialize routine
void dma0_int(void);       // DMA0 interrupt routine

/****************************************/
/*    Global variable declaration       */
/****************************************/
                        // Transfer data area.
const unsigned char    snd_data[8] =
       {0x01, 0x03, 0x07, 0x0f, 0x1f, 0x3f, 0x7f, 0xff};
unsigned short  dma_flg;   // DMA transmit complate flag. 1=complate.

/****************************************/
/*    Main Program                     */
/****************************************/
void main(void)
{

   sio_init();           // Serial-I/O initialization.

   dma_init();           // DMAC initialization.

   asm("fset i");         // Interrupt enabled

   dm0con |= 0x08;        // Set DM0CON register.
                        //  <DMAE>  : DMA enable
   te_u0c1 = 1;          // U0C1 register re-setup.
                       //  <TE>     : transmit enabled

   u0tb = snd_data[0];

   while(1);

}

/*****************************************/
/*  DMAC initialize routine           */
/*****************************************/
void dma_init(void)
{
   dm0sl = 0x0a;         // Set DM0SL register.
                       //  <DSEL3-0> : UART0 transmit
                       //  <DMS>     : Basic cause

   dm0con = 0x11;        // Set DM0CON register.
                       //  <DMBIT> : 8bit
                       //  <DMASL> : Single transfer
                       //  <DMAE>  : DMA disable
                       //  <DSD>   : Src  address direction=Forward
                       //  <DAD>   : Dest address direction=Fix

                       // Set DMA0 Source pointer address.
   sar0_addr.byte.low  = (char)(&snd_data[1]);
   sar0_addr.byte.mid  = (char)((unsigned long)(&snd_data[1]) >> 8);
   sar0_addr.byte.high = (char)((unsigned long)(&snd_data[1]) >> 16);

                       // Set DMA0 Destination pointer address.
   dar0_addr.byte.low  = (char)(&u0tb);
   dar0_addr.byte.mid  = (char)((unsigned long)(&u0tb) >> 8);
   dar0_addr.byte.high = (char)((unsigned long)(&u0tb) >> 16);

                       // Set DMA0 transfer counter.
   tcr0 = 6;

   dm0ic = 4;           // Set DMA0 interrupt priority-level = 4.

}

/*****************************************/
/*  Serial-I/O initialize routine      */
/*****************************************/
void sio_init(void)
{
   u0mr = 0x01;          // Set U0MR register.
                       //  <SMOD2-0> : Clock-synchronous
                       //  <CKDIR>   : Internal-clock
                       //  <IOPOL>   : No reverse

   u0c0 = 0x18;          // Set U0C0 register.
                       //  <CLK1-0>  : f1SIO
                       //  <CRD>     : CTS/RTS function disabled
                       //  <NCH>     :
                       //  <CKPOL>   : transfer data is output at falling edge
                       //  <UFORM>   : LSB first

   u0c1 = 0x00;          // Set U0C1 register.
                       //  <TE>     : transmit disabled
                       //  <RE>     : receive disabled
                       //  <U0LCH>   : No reverse
                       //  <U0ERE>   : Error signal output disable

   ucon = 0x00;          // Set UCON register.
                       //  <U0IRS> : Transmit interrupt cause = Buffer empty
                       //  <RCSP>  : CTS/RTS shared pin
```

```
    u0smr  = 0x00;          // Set U0SMR register.
    u0smr2 = 0x00;          // Set U0SMR2 register.
    u0smr3 = 0x00;          // Set U0SMR3 register.
                         //  <NODC> : CLK0 is CMOS output
    u0smr4 = 0x00;          // Set U0SMR4 register.

    u0brg = 127;            // Set U0BRG register.
                         //   62500bps(XIN=16MHz)

    s0tic = 0;              // Set UART0 transmit interrupt priority-level = 0.

}

/*****************************************/
/*  DMA0 interrupt routine             */
/*****************************************/
#pragma INTERRUPT/B dma0_int
// "/B" = Instead of saving the registers to the stack,
//       you can switch to the alternate registers.

void dma0_int(void)
{
    dma_flg = 1;            // DMA transmit complate set.
    p10  = 0xff;            // Transmit complate display.
    pd10 = 0xff;

}
```

4.2. Example of a Successive Reception Program

The following shows an example program for successively receiving 8 bytes of data using the DMAC. Here, settings are made assuming the DMAC and serial I/O specifications shown below.

- DMAC Specification
  DMA Request Factors=UART0 reception, Single transfer, Transfer unit = 16 bits (including an error flag), Transfer source address direction=fixed (U0RB register), Transfer destination address direction=Forward direction
- Serial I/O Specification
  Clock synchronous serial I/O mode, External clock, CTS/RTS function disabled, Continuous receive mode enabled

```
/***********************************************************************/
/*                                                          */
/*  M16C/62 Group Program Collection                             */
/*                                                          */
/*  FILE NAME : rjj05b0543_rcv.c                                */
/*  CPU      : M16C/62P Group                                 */
/*  FUNCTION  : The sample program of the serial I/O continuation     */
/*            reception using DMAC.                            */
/*  HISTORY   : 2004.11.01 Ver 1.00                             */
/*                                                          */
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/*                                                          */
/***********************************************************************/

/****************************************/
/*    include file                 */
/****************************************/
#include "sfr62p.h"           // Special Function Register Header File

/****************************************/
/*    Function declaration           */
/****************************************/
void sio_init(void);          // Serial-I/O initialize routine
void dma_init(void);          // DMAC initialize routine
void dma0_int(void);          // DMA0 interrupt routine

/****************************************/
/*    Global variable declaration      */
/****************************************/
unsigned short  rcv_data[8];    // Repeat receive data area
unsigned short  dummy_buf;     // Dummy receive data area

/****************************************/
/*    Main Program                 */
/****************************************/
void main(void)
{

    sio_init();           // Serial-I/O initialization.

    dma_init();           // DMAC initialization.

    asm("fset i");         // Interrupt enabled

    dm0con |= 0x08;        // Set DM0CON register.
                       //  <DMAE>  : DMA enable

    u0c1 |= 0x05;          // U0C1 register re-setup.
                       //  <TE>      : transmit disabled
                       //  <RE>     : receive enabled
   dummy_buf = u0rb;      // Data reception is started after dummy reception..

   while(1);

}

/****************************************/
/*  DMAC initialize routine      */
/****************************************/
void dma_init(void)
{
   dm0sl = 0x0b;         // Set DM0SL register.
                       //  <DSEL3-0> : UART0 receive
                       //  <DMS>    : Basic cause

   dm0con = 0x20;         // Set DM0CON register.
                       //  <DMBIT> : 16bit
                       //  <DMASL> : SIngle transfer
                       //  <DMAE>  : DMA disable
                       //  <DSD>   : Src  address direction=Fix
                       //  <DAD>   : Dest address direction=Forward

                       // Set DMA0 Source pointer address.
   sar0_addr.byte.low  = (char)(&u0rb);
   sar0_addr.byte.mid  = (char)((unsigned long)(&u0rb) >> 8);
   sar0_addr.byte.high = (char)((unsigned long)(&u0rb) >> 16);

                       // Set DMA0 Destination pointer address.
   dar0_addr.byte.low  = (char)(&rcv_data);
   dar0_addr.byte.mid  = (char)((unsigned long)(&rcv_data) >> 8);
   dar0_addr.byte.high = (char)((unsigned long)(&rcv_data) >> 16);

                       // Set DMA0 transfer counter.
   tcr0 = 7;

   dm0ic = 4;            // Set DMA0 interrupt priority-level = 4.

}

/****************************************/
/*  Serial-I/O initialize routine      */
/****************************************/
void sio_init(void)
{
   u0mr = 0x09;          // Set U0MR register.
                       //  <SMOD2-0> : Clock-synchronous
                       //  <CKDIR>   : External-clock
                       //  <IOPOL>   : No reverse

   u0c0 = 0x1c;          // Set U0C0 register.
                       //  <CLK1-0>  :
                       //  <CRD>    : CTS/RTS function disabled
                       //  <NCH>    :
                       //  <CKPOL>   : receive data is input at rising edge
                       //  <UFORM>   : LSB first

   u0c1 = 0x00;          // Set U0C1 register.
                       //  <TE>     : transmit disabled
                       //  <RE>     : receive disabled
                       //  <U0LCH>   : No reverse
                       //  <U0ERE>   : Error signal output disable

   ucon = 0x04;          // Set UCON register.
                       //  <U0RRM> : Continuous receive mode enabled
                       //  <RCSP>  : CTS/RTS shared pin

   u0smr  = 0x00;        // Set U0SMR register.
   u0smr2 = 0x00;         // Set U0SMR2 register.
   u0smr3 = 0x00;         // Set U0SMR3 register.
```

```
    u0smr4 = 0x00;          // Set U0SMR4 register.

    s0ric = 0;             // Set UART0 receive interrupt priority-level = 0.

}

/****************************************/
/*  DMA0 interrupt routine            */
/****************************************/
#pragma INTERRUPT/B dma0_int
// "/B" = Instead of saving the registers to the stack,
//       you can switch to the alternate registers.

void dma0_int(void)
{
                          // Receive data display.
    pd0 = 0xff;             // P0 is an output port.
    pd1 = 0xff;             // P1 is an output port.
    pd2 = 0xff;             // P2 is an output port.
    pd3 = 0xff;             // P3 is an output port.
    pd4 = 0xff;             // P4 is an output port.
    pd5 = 0xff;             // P5 is an output port.
    pd6 = 0xff;             // P6 is an output port.
    pd7 = 0xff;             // P7 is an output port.
    p0  = rcv_data[0];        // Receice data 1st byte display.
    p1  = rcv_data[1];        // Receice data 2ndt byte display.
    p2  = rcv_data[2];        // Receice data 3rd byte display.
    p3  = rcv_data[3];        // Receice data 4th byte display.
    p4  = rcv_data[4];        // Receice data 5th byte display.
    p5  = rcv_data[5];        // Receice data 6th byte display.
    p6  = rcv_data[6];        // Receice data 7th byte display.
    p7  = rcv_data[7];        // Receice data 8th byte display.

    prc2 = 1;
    pd9  = 0xff;                // P9 is an output port.
    pd10 = 0xff;                // p10 is an output port.
    p9   = rcv_data[7];          // Receive data 8th byte display.
    p10  = (char)(rcv_data[7] >> 8);// Error flag display.

}
```

5. Reference

Renesas Technology Corporation Home Page

http://www.renesas.com/

E-mail Support

E-mail: csc@renesas.com

Hardware Manual

M16C/62P Group Hardware Manual Rev.2.30
(Use the latest version on the home page: http://www.renesas.com)

TECHNICAL UPDATE/TECHNICAL NEWS

(Use the latest information on the home page: http://www.renesas.com)

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		Page	Summary
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