82P338XX/9XX

Introduction

The IDT82P338XX/9XX **S**ynchronization **M**anagement **U**nit (SMU) for IEEE 1588 and Synchronous Ethernet (SyncE) provides tools to manage timing references. It has several different modes to align the output clocks, to control the skew, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks.

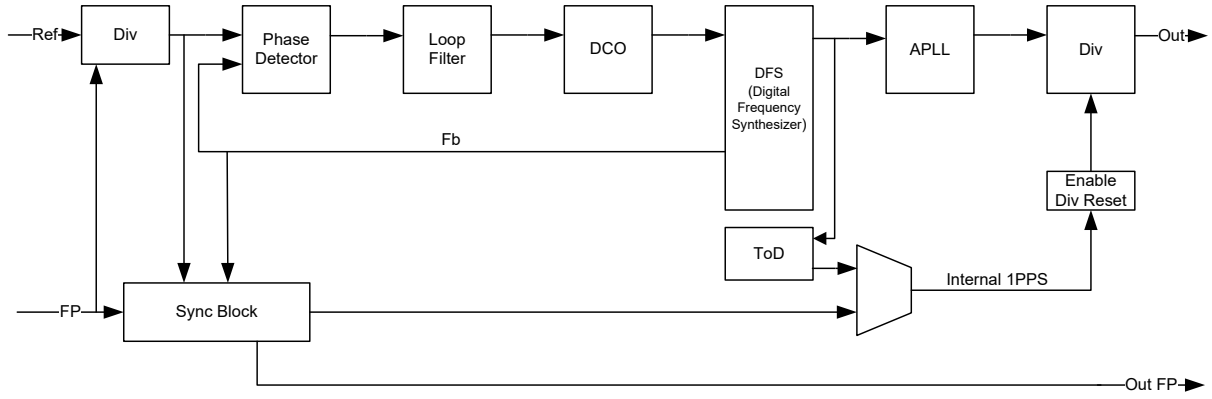

Figure 1: 82P338XX/9XX Block Diagram

Procedure to program clock phase skew

The 82P338XX/9XX enables the capability to manage phase skew of a physical clock at it's inputs, outputs and/or input-to-output. This application note describes the procedure to program the 82P338XX/9XX skews from its power-up default state; and it describes how to dynamically adjust skews needed for certain applications, such as 'snapping' a 1PPS clock representing a 1588 PTP clock. It also presents the measured skew offsets of 82P338XX/9XX for a typical configuration example.

Overview of clock skew capabilty

Per-Input skew control

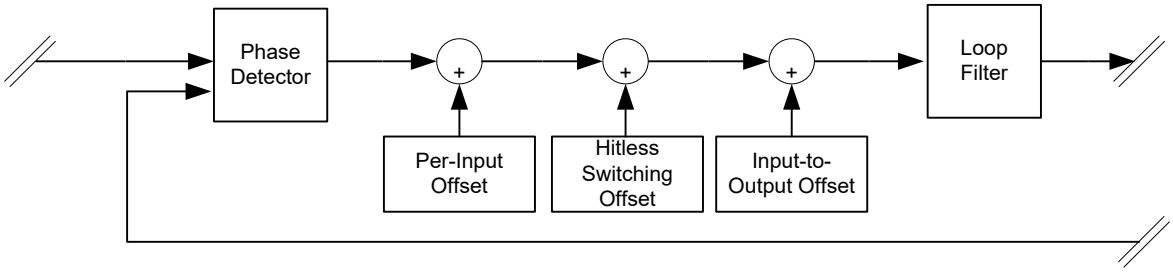

Figure 2: 82P338XX/9XX Input Clock & System Skew Block Diagram

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Each input provides a means to apply an independent phase skew offset to the reference clock. This skew is applied when the reference input is selected by the DPLL, after the phase detector. The value is a signed 7-bit digital value with units of 0.61ns, providing a range from [+77.5 ns,-78.1ns]of skew control.

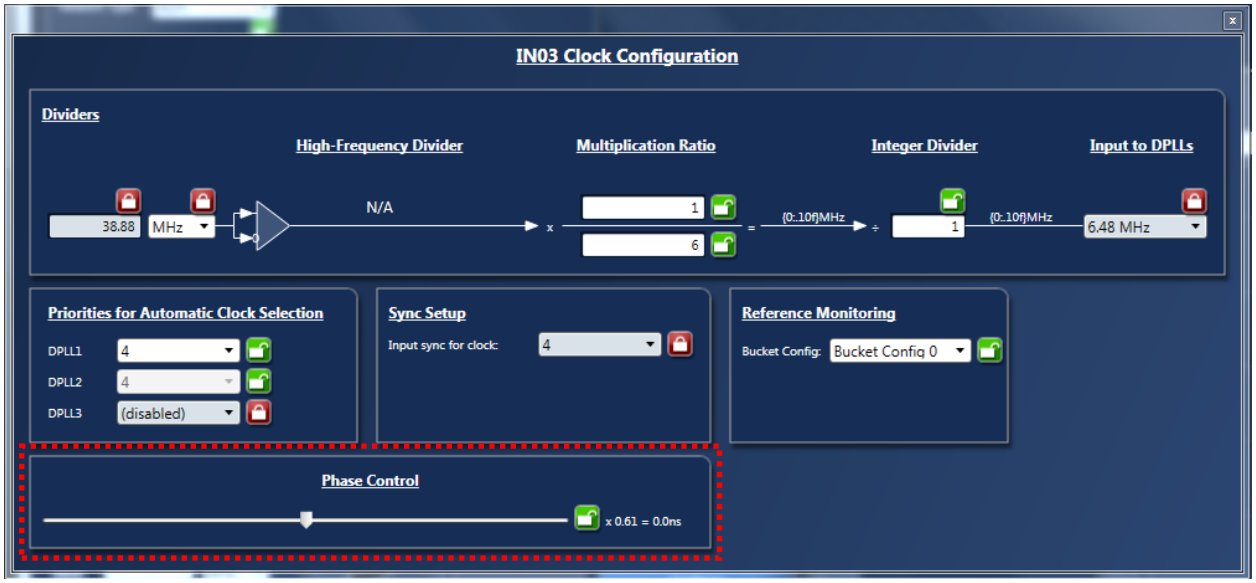

Figure 3: 82P33831 Timing Commander Input Clock Skew Settings

Since this offset is applied after the phase detector, any changes to the skew will be filter and phase limited by the DPLL.

Input-to-output skew control

Each DPLL provides a means to apply a system level phase skew offset to the clock. This skew is applied at the phase detector, and represents a phase offset of the feedback clock (internal or external) from the selected input reference clock. The value is a signed 28-bit digital value with units of 0.0745ps, providing a range from [+20µs,-20µs]of skew control.

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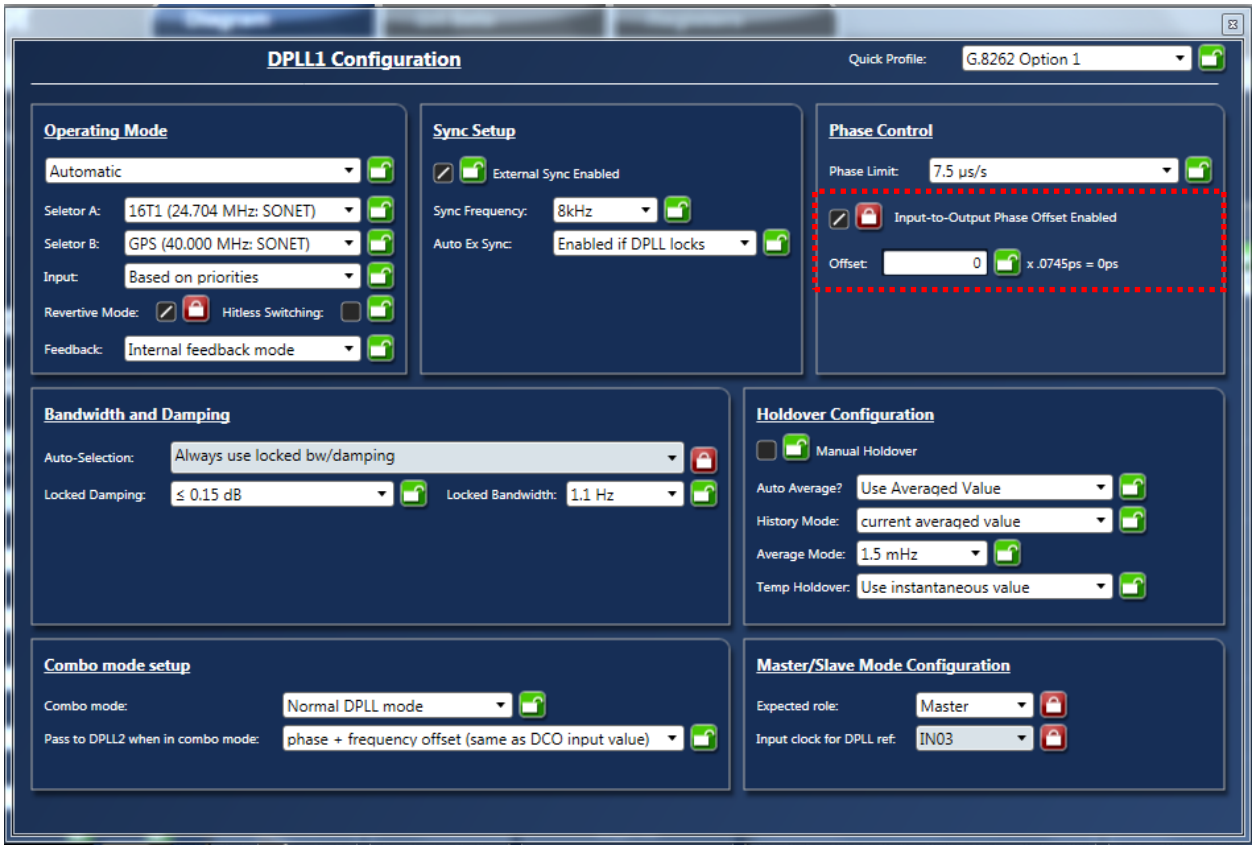

Figure 4: 82P33831 Timing Commander Input-to-Output Clock Skew Settings

Since this offset is applied after the phase detector, any changes to the skew will be filter and phase limited by the DPLL.

This 28-bit register is also used to apply the phase offset value when operating in Write Phase DCO mode.

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Per-Output skew control

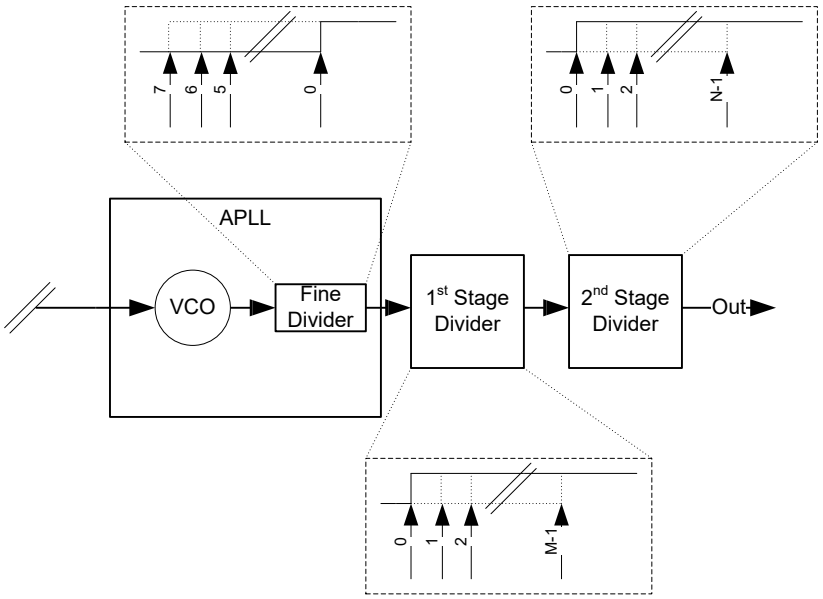

Figure 5: 82P338XX/9XX Output Clock Skew Block Diagram

Each output (OUT01~08[1]) provides a means to apply an independent phase skew offset of the synthesized clock. This skew represents a phase offset from the DPLL, which means any changes to the skew will cause a 'snap' of the output clock edge. There are three (3) adjustments available: up to two coarse adjustments in the positive direction, and one fine adjustment (APLL synthesized clock only) in the negative direction; which provides +/-180° of skew control.

The output skew adjustment is analogue based, providing very precise adjustments that are based on the APLL VCO or DFS engine clock edges.

[1] OUT08 for 82P33x10/x14, OUT07 for 82P33x31

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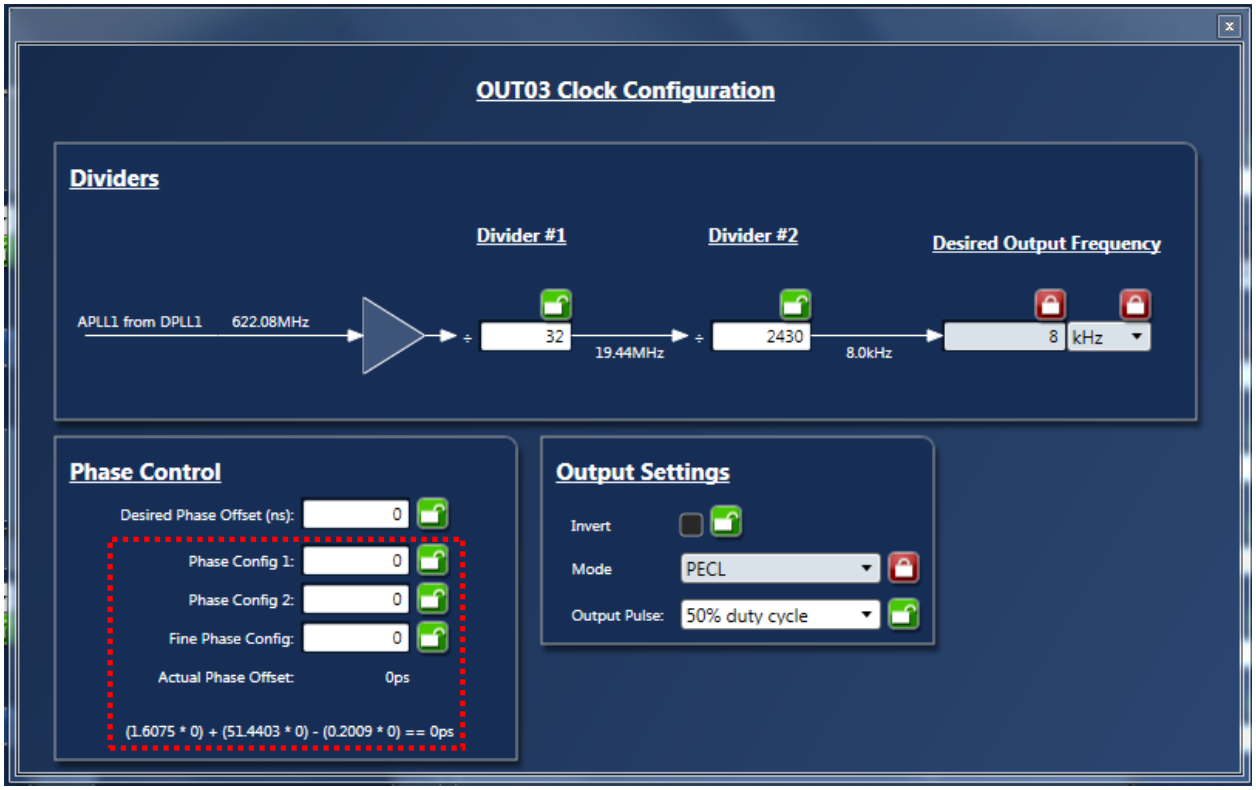

Figure 6: 82P33831 Timing Commander Output Clock Skew Settings

The first coarse value is a 5-bit value with units determined by either the APLL VCO frequency or the clock frequency from the DFS engine. For the example above using an APLL with VCO=622.08MHz, the unit would be 1/622.08M=1.6075ns. The max value that can be programmed is determined by the first stage divider value (M) minus 1. For the example above, the maximum value would be 31 for up to +49.8328ns of skew adjustment.

The second coarse value is a 27-bit value with units determined by the clock frequency from the first stage divider. For the example above using a /32 on the APLL clock (19.44MHz), the unit would be 1/19.44M= 51.4403ns. The max value that can be programmed is determined by the second stage divider value (N) minus 1. For the example above, the maximum value would be 2429 for up to + 124.9486µs of skew adjustment.

The total range with the two coarse adjustments would be [0,+124.9984]µs.

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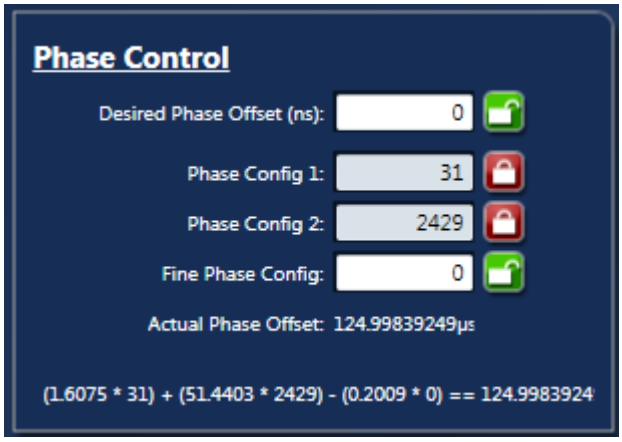

Figure 7: Output Clock Coarse Skew Setting Example

The fine value is a 3-bit value with units determined by the APLL VCO frequency * 8. Only a clock from the APLL has a fine skew adjustment. For the example above using an APLL with VCO=622.08MHz, the unit would be 1/(622.08M*8)= 200.9ps. The max value is 7 for a range of [0, -1.4066]ns of skew adjustment.

Figure 8: Output Clock Fine Skew Setting Example

Power-up Default State

Upon power-up, if there is no external EEPROM available, then the 82P338XX/9XX loads its register configurations from the metal defaults. With the qualification and locking to any input reference clock, the 82P338XX/9XX will exhibit typical delays as shown in Table 1.

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Output	Min (ns)	Max (ns)	Range (ns_{pp})
Any Input to Any APLL Output	10	19	9 (+/-4.5 around mean)
Any input to [M]FRSYNC Output	0	8	8
NOTES	1. The measurements in the above table takes into account any delays in the clock path from any input to any output; through either DPLL1 or DPLL2 and either APLL1 or APLL2. 2. The measurements in the above table are over operational temperature, varying power supply and repeated power on/off cycle. 3. Measurements are taken using an ideal REF input and an ideal System clock to account for only internal delays in the device.		

Table 1: Input-to-Output Delay for 82P338XX/9XX with Power-Up Default Configuration

Looking at a specific output clock, the 82P338XX/9XX will exhibit typical delays as shown in Table 2.

Output	Min (ns)	Max (ns)	Range (ns_{pp})
Any LVCMOS Input to any of OUT01, OUT02, OUT07, OUT08*	13	19	6 (+/-3 around mean)
Any LVPECL/LVDS Input to any of OUT03, OUT04, OUT05, OUT06	11.5	16.5	5 (+/-2.5 around mean)
NOTES	1. The measurements in the above table takes into account any delays in the clock path from any input to any output; through either DPLL1 or DPLL2 and either APLL1 or APLL2. 2. The measurements in the above table are over operational temperature, varying power supply and repeated power on/off cycle. 3. Measurements are taken using an ideal REF input and an ideal System clock to account for only internal delays in the device. * OUT08 for 82P33x10/x13/x14 only		

Table 2: Input-to-Output Delay for 82P338XX/9XX

For the associated output clock pair, the 82P338XX/9XX will exhibit delays as shown in Table 3.

Output	Min (ps)	Max (ps)
Output to Output, APLL LVCMOS (OUT01 to OUT02, OUT07 to OUT08*)	-110	110
Output to Output, LVPECL/LVDS (OUT03 to OUT04, OUT05 to OUT06)	-85	85

Table 3: Output-to-Output Delay for 82P338XX/9XX

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Programming Output Skew for SETS Application

For SETS applications, the input to output delay is typically not a factor as measurements are taken at the T0 output. However, a general rule is to try maintain a less than 10ns variation on the output in relationship to the input reference clock (excluding LPF response).

For this reason, Table 1 can be used to determine an initial skew offset by taking the Minimum number and writing an applicable coarse phase offset value. In this case, a value of 10ns would be used.

Programming Output Skew for T-GM(-P) Application

For T-GM(-P) applications, the input to output delay is critical to minimize any additional Time Error on the synthesized clocks in relationship to the PRTC. In this case, Table 2 should be used to determine an initial skew offset by taking the mean value and writing an applicable coarse & fine phase offset value. For example, if a 1PPS pulse is configured for OUT01 (LVCMOS), then a value of 16ns would be used. If a 125MHz clock is configured for OUT03 (LVPECL), then a value of 14ns would be used.

One note is if [M]FRSYNC is being used to represent the frame or sync pulse, in this case you may want to use the minimum value to make sure that the output clock never leads the [M]FRSYNC pulse.

Programming Output Skew for DCO (1588) Application

For DCO applications, the input to output delay is not applicable, as the "phase detector" is now at the timestamper; meaning that the synthesized clock from the 82P338XX/9XX now represents the "feedback" clock. However, when representing the PTP clock with a 1PPS output, there will be a need to snap the edge of the 1PPS clock to represent the nanosecond rollover (since pulling in +/-500ms via DCO would take too long).

For example, at start-up, all the clocks will be arbitrarily aligned to the internal 1PPS clock. This means that the 1PPS output may be up to +/-500ms off from the GM reference clock. To snap this phase, the output divider control may be used once the DCO has been syntonized to the GM clock (i.e. frequency locked).

For example, if a 1PPS pulse is to be moved by +125ms, then the following coarse & fine offsets can be used.

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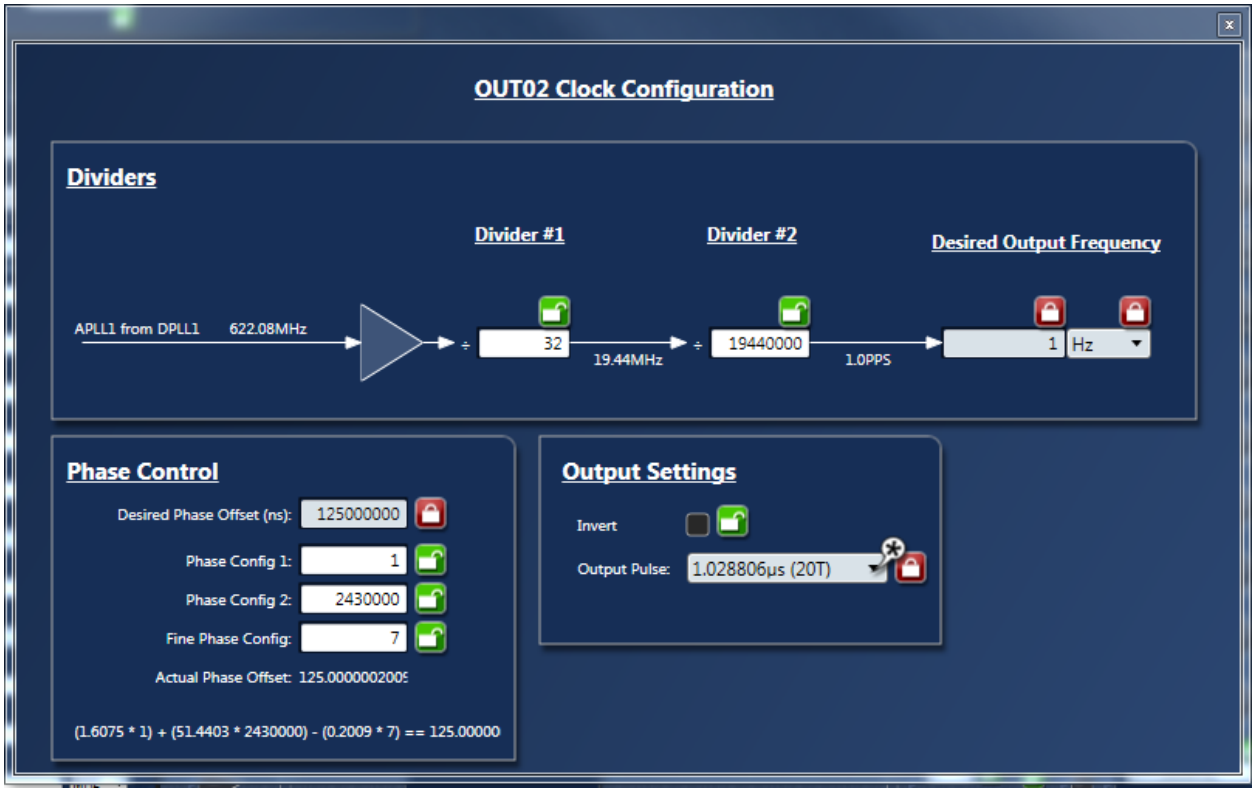

Figure 9: 1PPS Output Clock Snap Example

For questions related to device configurations, please contact IDT application support at support-sync@idt.com.

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