Power MOS FET

Structure and Features

R07ZZ0007EJ0200
(Previous: REJ27G0014-0100)
Rev.2.00
Aug 18, 2014

Renesas has two types of Power MOS FETs, D Series (vertical structure) and S Series (lateral structure), as shown in Figure 1 and Figure 2. Although there are some differences in their characteristics, both have the following advantages.

- Good frequency response and high switching speed due to absence of carrier storage effect.
- Free from current concentration, and hence have high resistance to destruction.
- Require a very low driving power as they are voltage controlled devices.

To understand the structure and features of Power MOS FETs, we would like to show the N-channel MOS FET.

Figure 3 shows the basic structure of the n-channel MOS FET. This is called a MOS (metal–oxide–semiconductor) structure because the metallic gate electrodes are covered by an oxide film. The source is so called because it is the source of the charged carriers (in this case, electrons), which flow out of the structure via the drain.

A positive voltage on the gate electrode drives inversion in the p layer directly under the gate, forming an n-channel through which current flows from drain to source. This is how the power MOS FET operates (the opposite is true of the p channel).

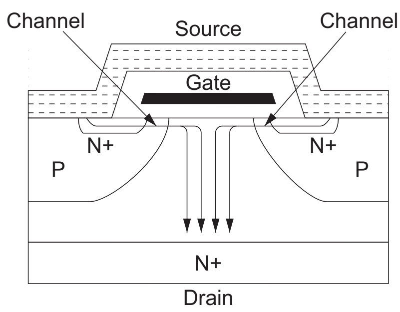

Figure 1 Structure of D Series (Vertical type) (N channel)

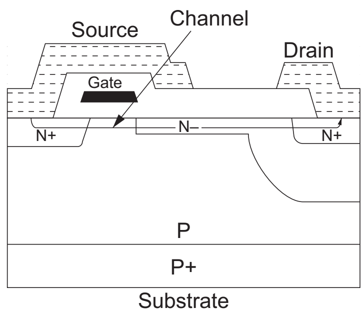

Figure 2 Structure of Series (Lateral type) (N channel)

When a voltage is applied between the drain and source, the electrons in the channel move in the direction of the drain, so a drain current flows.

There are two type of FETs, depletion type (normally ON type) and enhancement type (normally OFF type). In the case of depletion type FETs, drain current flows even if the gate voltage is 0 V, in contrast to enhancement type FETs. Renesas Power MOS FETs are all enhancement type (normally OFF type).

The gate voltage at which the drain current begins to flow is gate cut-off voltage $V_{GS(off)}$. (Figure 4).

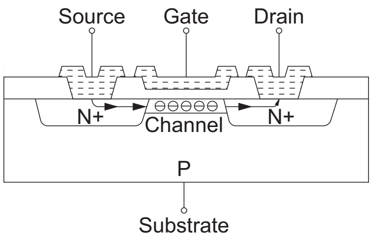

Figure 3 Basic structure of MOS FET (Lateral type)

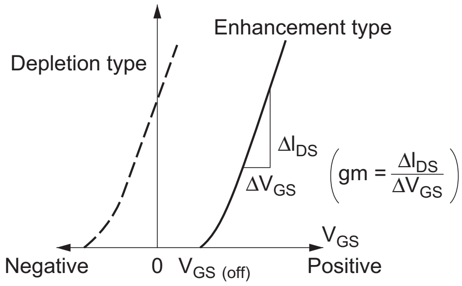

Figure 4 Transfer Characteristics

Normally, there is a quadratic correlation between I_{DS} and V_{GS}. The slope of its curve gives the mutual conductance

gm $\left(=\frac{\Delta I_{DS}}{\Delta V_{GS}}\right)$, that shows amplification factor.

Breakdown voltage of the drain varies with the structure between the N^+ region of the drain and the gate electrode, as shown in Figure 3. There is only a thin oxide film between the N^+ region and the gate electrode, so the field gradient will be high. This makes it difficult to achieve high drain to gate breakdown voltage, limited to 20 to 30 V in typical MOS FETs.

By widening the space between the N^+ region of the drain and the gate electrode, and easing the electric field concentration, we can make the breakdown voltage larger.

A power MOS FET is formed by multiple cells connected in parallel.

There are two types of power MOS FET structure: the vertical and the lateral structure. We refer to devices with the respective structures as D- and S-series. The structures are illustrated in figures 1 and 2. The features of each type are described below.

- D Series (vertical structure)

In D series the drain (N^+) is placed beneath the silicon substrate. The gate electrode covers over the N region between P channels, to ease the electric field concentration beneath the gate. The electrons flow out of the source and reach to the N region through the P channels horizontally. On the surface of the N region, there is an accumulation layer of N^+ produced by the positive voltage applied to the gate electrode. Therefore, the electrons are attracted to the accumulation layer, to flow to the drain through the N region vertically.

Consequently the D series is referred to as a vertical structure. In this structure, the case is connected to the drain.

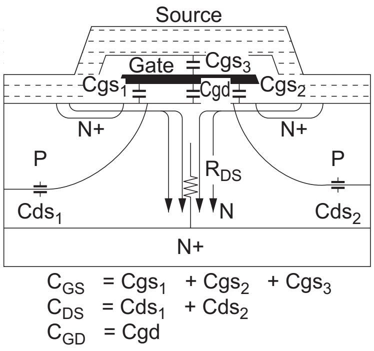

Figure 5 Structure of D Series (Vertical type) (N channel)

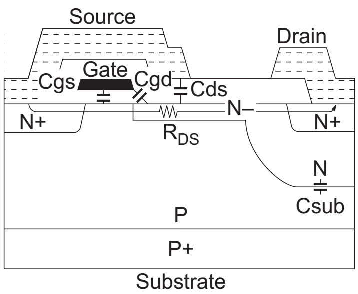

Figure 6 Structure of S Series (Lateral type) (N channel)

In the D series the channel (N region) is placed in the silicon, and the size of one unit can be smaller than that of S series. This enables the switching ON resistance of D series to be smaller than that of S series with the same voltage and the same chip size.

Electrostatic capacitances are the junction capacitances and the MOS capacitances as shown in Figure 5.

Here, the capacitance between the drain and the gate, C_{GD}, is relatively large, so in the source earth circuit, C_{GD}'s effects to the input capacitance (Ciss), to the output capacitance (Coss) and to the feedback capacitance (Crss) should be considered.

The gate electrode is made of polysilicon, which has long been used effectively in CMOS LSI. Polysilicon resistance is about 100 times larger than that of metals. When using it for the gate electrode, we lower the gate resistance by using a mesh gate pattern, and by connecting the polysilicon gate and the metal electrode effectively. To find the switching time of the vertical structure, more complicated operation analysis is required, because the feed back capacitance (Cgd) is large and the voltage dependence of the drain resistance is large. The input capacitance can't be determined simply by the time constant of the gate resistance. This will be further explained in the "Attention of Handling Semiconductor Devices".

- S Series (lateral structure)

In S series, the drain (N^+ region) is placed on the surface of the silicon. The region between the drain (N^+) and P channel is an N region produced by ion implantation, and it makes the strength of the electrostatic field even. Moreover, the source electrode is extended to cover a part of the N region, working as a field plate to prevent electrostatic field concentration around the gate. The electrons flow out of the source and reach to the drain through the P channel and the N region laterally. This is why the S series is called a lateral structure.

The substrate is connected to the source electrode, and the case to the source.

The feedback capacitance (Crss) is indicated as Cgd in Figure 6. The source field plate is extended above the N region, so the Cgd is shielded by the field plate and the capacitance of the N region (Cds). This results in a very small value of feedback capacitance (Crss).

From the view points of chip and package, the S series is very suitable for high frequency use, because the input and the output leads are separated electrically

Website and Support

Renesas Electronics Website

http://www.renesas.com/

Inquiries

http://www.renesas.com/contact/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 18, 2004	–	First edition issued
2.00	Aug. 18, 2014	–	The format was changed into the newest thing. The document number was changed.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141