To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

APPLICATION NOTE

Output of Three Complementary Pairs of PWM Signals

Introduction

Applies the complementary PWM mode of the H8/3687's timer Z block to output three complementary pairs (normal- and inverse-phase) of PWM waveforms that have the same period but individually controllable duty cycles.

Target Device

H8/300H Tiny Series H8/3687

Contents

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

1. Specifications

1. Applies the complementary PWM mode of the H8/3687's timer Z block to output three complementary pairs (normal- and inverse-phase) of PWM waveforms that have the same period but individually controllable duty cycles.
2. This sample task involves controlling the H8/3687 to produce outputs of the form shown in figure 1.1, that is, three complementary pairs of PWM waveforms, each of which has a controllable duty cycle but the same period. The level changes of the normal- and inverse-phase outputs are not simultaneous.
3. Any duty cycle from 0 to 100% is specifiable in registers.

$$\text{Duty cycle} = \frac{\text{High-level pulse width}}{\text{Period pulse}} \times 100\ (\%)$$

4. A toggled waveform with the same period is also output.

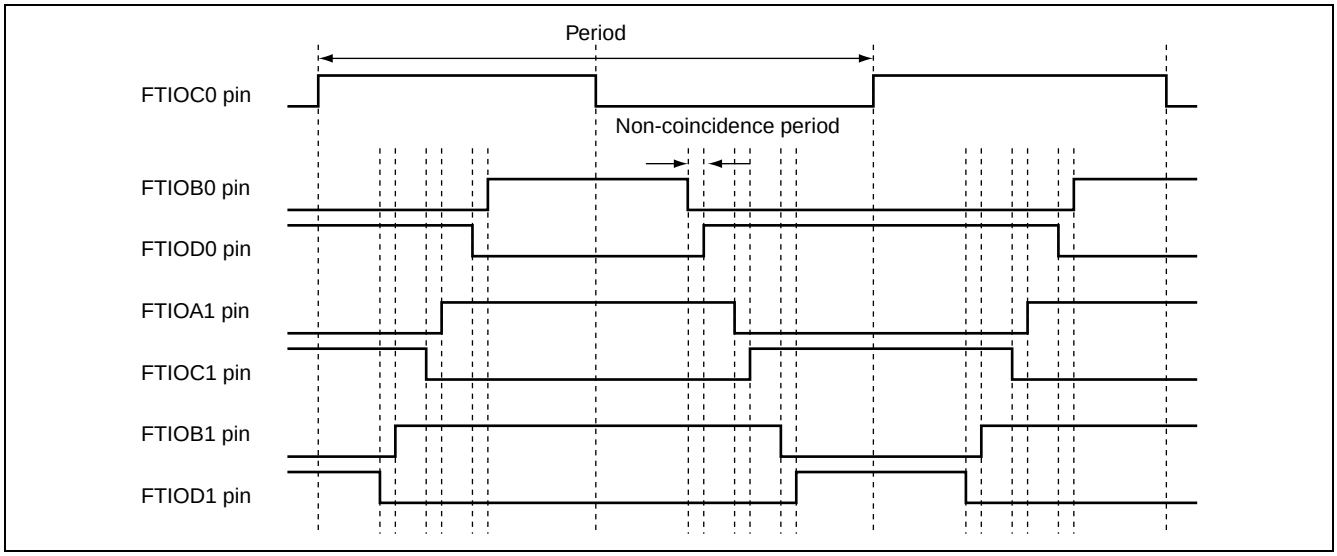


Figure 1.1 Output of Three Complementary (Normal and Inverse Phase) Pairs of PWM Signals

2. Functional Descriptions

1. In this sample task, the H8/3687 is controlled to produce three pairs of complementary PWM waveforms, i.e., waveforms in both normal and inverted phase. The level changes of the normal- and inverse-phase outputs are not simultaneous (there is a non-coincident period). This is achieved through the combination of channels 0 and 1 of timer Z. A toggled waveform with the same period as the PWM waveforms is also produced.
   1) Figure 2.1 is a block diagram of the way channels 0 and 1 of timer Z are used in this sample task.

      The following functions are used.

   — The complementary PWM mode, to output three pairs of inverse- and normal-phase PWM waveforms that do not change levels at the same time (complementary PWM period).

   — The transfer of buffer-register contents (GRC0/D0, GRC1/D1) to the comparison-value registers (GRA0/B0, GRA1/B1) when a compare-match occurs.

   — Production of a waveform that is toggled in synchronization with the PWM waveform cycle.

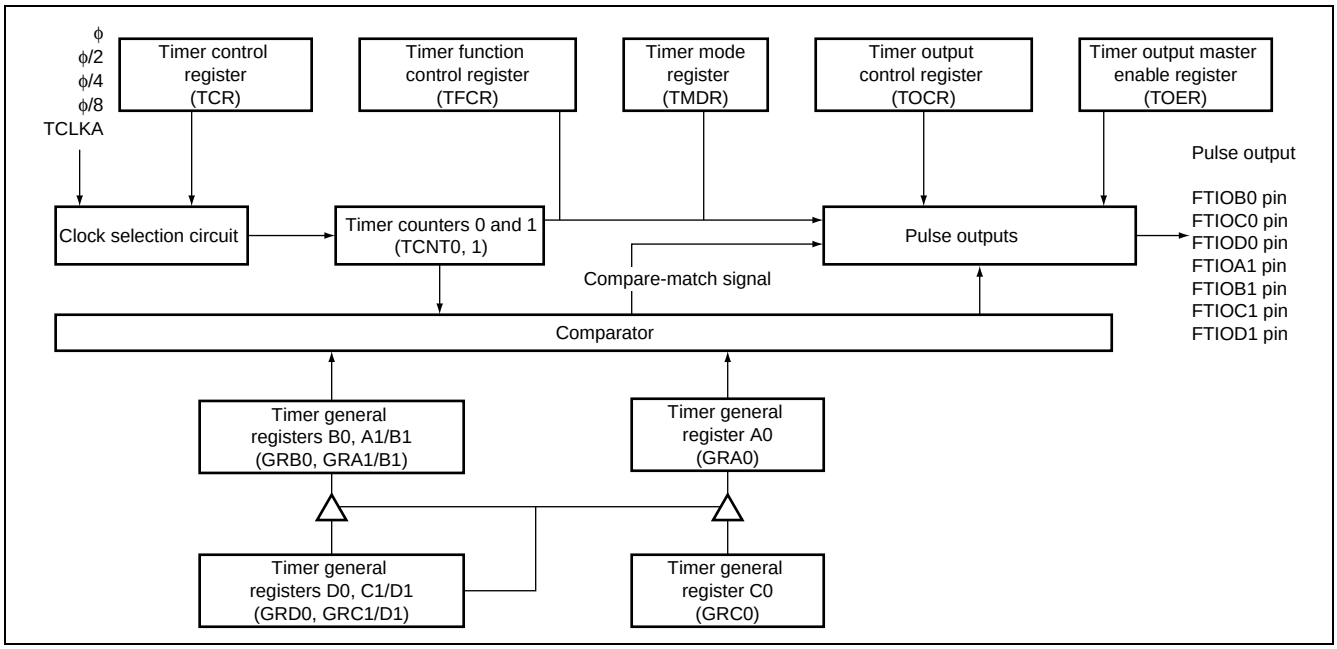


Figure 2.1 Timer Z Channels 0 and 1 in the Complementary PWM Mode

2) Table 2.1 shows the function assignments for this task. The three pairs of complementary-PWM signals are output by assigning the timer Z functions to the pins and registers indicated in table 2.1.

Table 2.1 Function Assignments

Pin or Register Name	Assigned Function
FTIOC0	Output toggled in synchronization with the PWM signal.
FTIOB0	PWM output 1
FTIOD0	Inverse-phase waveform which changes levels at slightly different times to PWM output 1.
FTIOA1	PWM output 2
FTIOB1	PWM output 3
FTIOC1	Inverse-phase waveform which changes levels at slightly different times to PWM output 2.
FTIOD1	Inverse-phase waveform which changes levels at slightly different times to PWM output 3.
TSTR	Enabling and disabling of TCNT0 and TCNT1 operation.
TOCR	Specification of the initial output level, i.e., the level before the first compare-match occurs.
TOER	Enabling and disabling of the signal output from the complementary PWM output pins.
TMDR	Specifies GRC0, GRD0, GRC1 and GRD1 as the buffer registers for GRA0, GRB0, GRA1 and GRB1, respectively.
TCR0 and TCR1	Select the input clock for and the condition that drives clearing of the channel 0 and 1 timer counters.
TFCR	Specifies the complementary PWM mode of timer Z.
GRA0	Specifies half of the PWM period.
GRC0	Buffer register for GRA0
GRD0	Buffer register for GRB0
GRB0, GRA1, GRB1	Specify the points where the levels of the output pulses change (comparison-value registers).
GRC1	Buffer register for GRA1
GRD1	Buffer register for GRB1

3. Description of Operation

Figure 3.1 shows the operational principle in the output of a single complementary pair of PWM waveforms. As the figure shows, the waveforms are output through a combination of hardware and software processing by the H8/3687. Note that, in this example, it is set up so that the data of waveform level-change timing is transferred from the buffer register to the compare register at the trough.

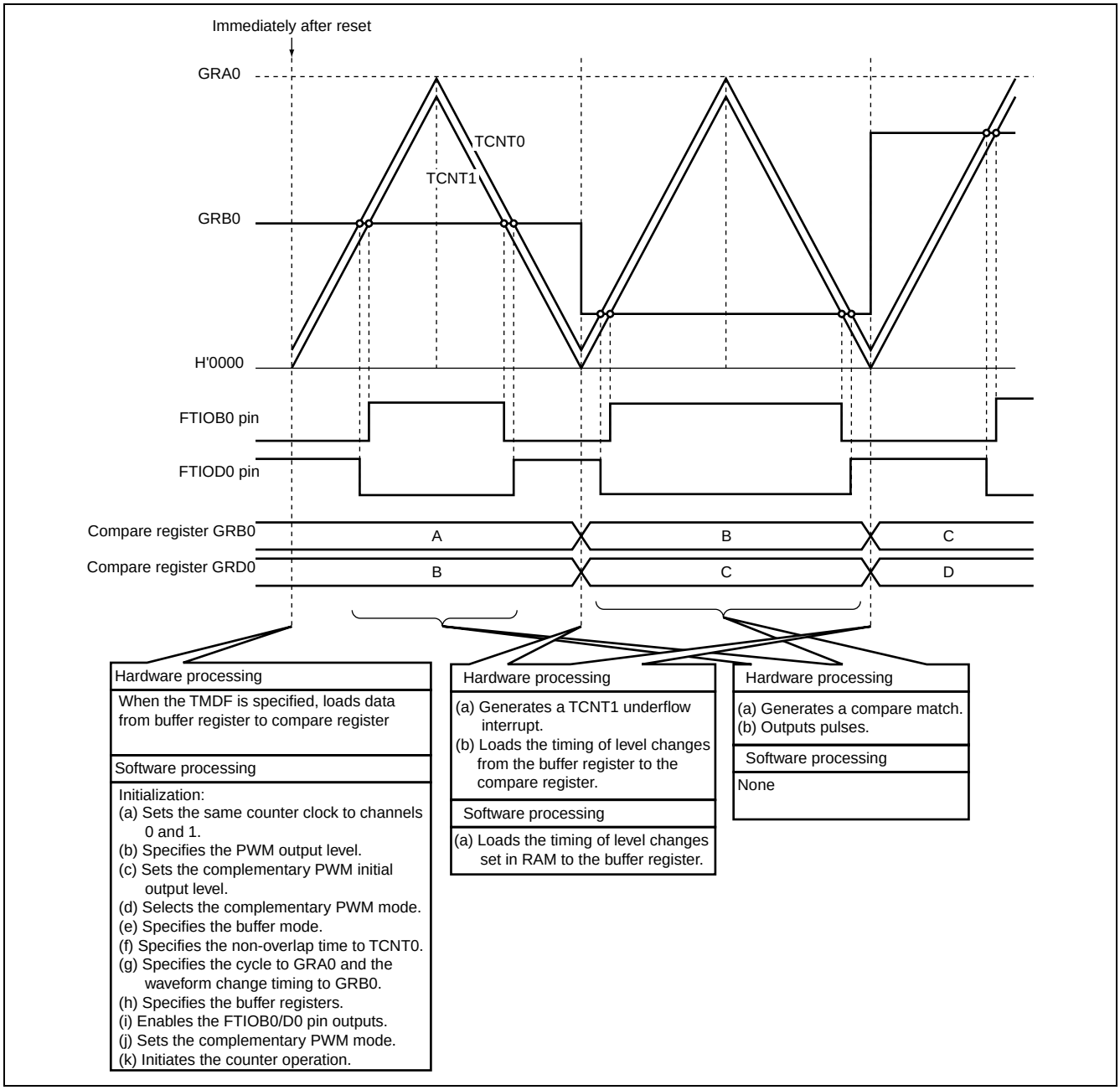


Figure 3.1 Operational Principle of Complementary PWM1-Phase Waveform Output

Figure 3.2 shows the principle of operation for the output of a waveform toggled in synchronization with the complementary PWM waveforms. As the figure shows, the waveforms are output through a combination of hardware and software processing by the H8/3687.

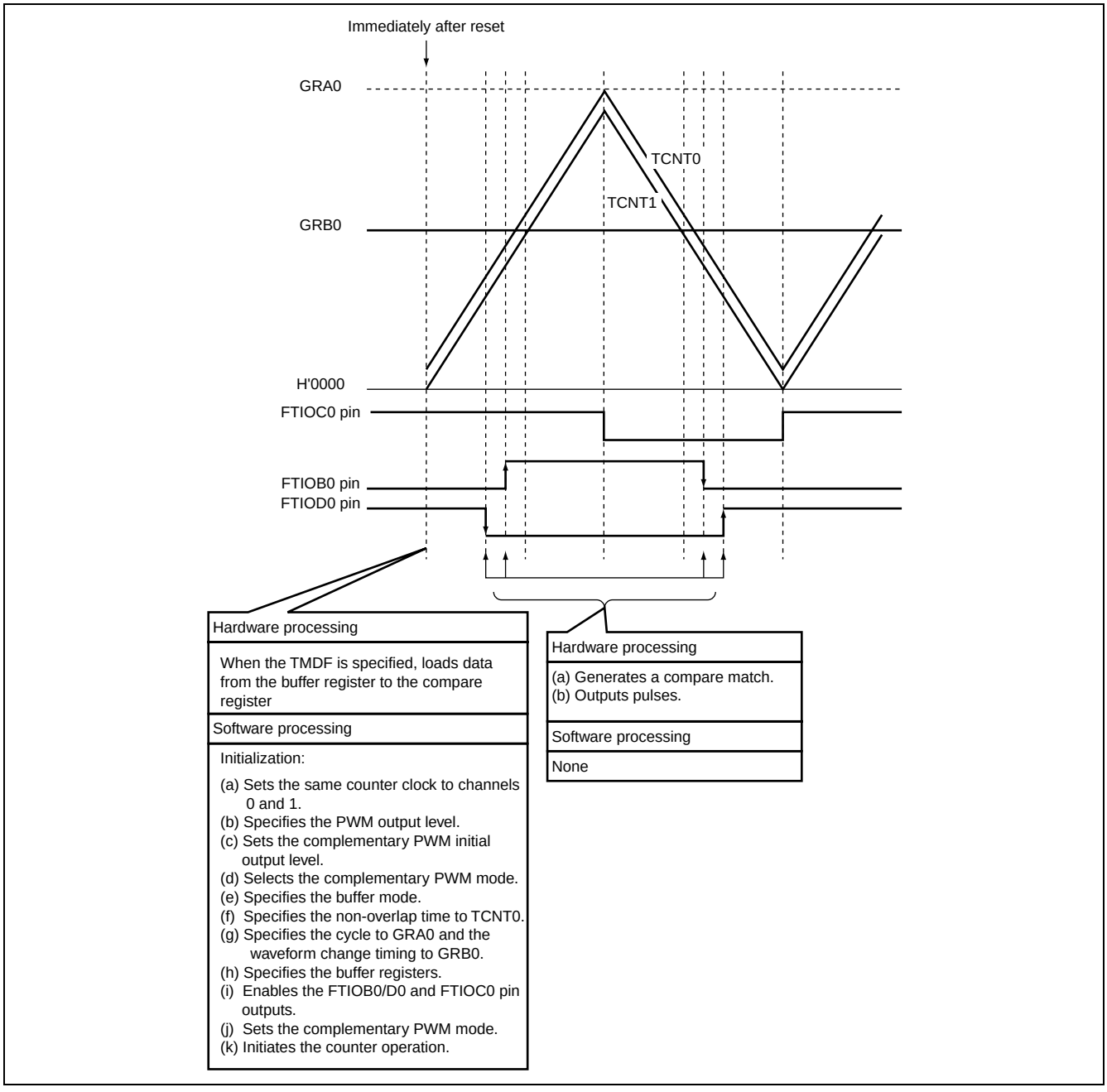


Figure 3.2 Operational Principle for the Output of a Waveform Toggled in Synchronization with the PWM Cycle

Figure 3.3 shows the principle of operation for the complementary-waveform output part of the sample task. As is shown in the figure, a combination of hardware and software processing by the H8/3687 is used to produce the three complementary pairs of PWM waveforms on the PWM output pins (FTIOB0/D0, FTIOA1/B1/C1/D1) of channels 0 and 1. Note that, in this example below, it is set up so that the data of PWM waveforms' level-change timing are transferred from the buffer registers to respective compare registers at the crest.

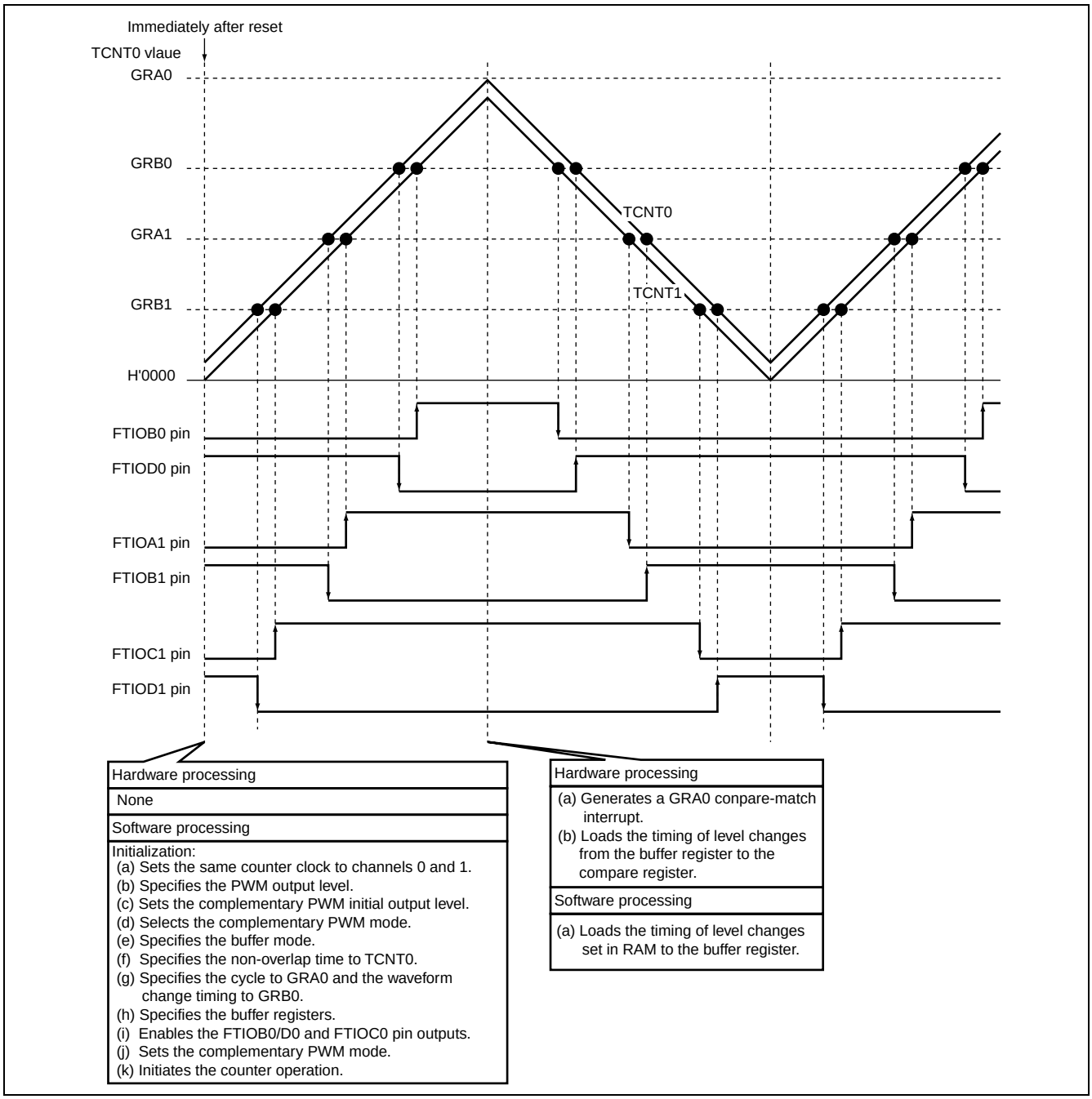


Figure 3.3 Operational Principle of PWM Waveform Output

4. Software Descriptions

4.1 Modules

Module Name	Label Name	Function
Main routine	main	Sets up the complementary PWM waveform output.
Data specification	setdata	Sets the buffer-register values that control the timing of waveform changes.

4.2 Arguments

Label Names	Assigned Function	Data Size	Used in	Input/ Output
pul_cyc	Specifies half of the period for the pulses. The following formula is used to calculate the pulse period: period (ns) = timer value × ϕ (=62.5 ns in 16-MHz operation)	1 word	Main routine	Input
duty_1	Specifies the timings of the level changes in the waveforms output on the FTIO pins.			
duty_2				
duty_3				
dead_time	Specifies the non-coincidence period.		Main routine Data specification	

4.3 Internal registers used

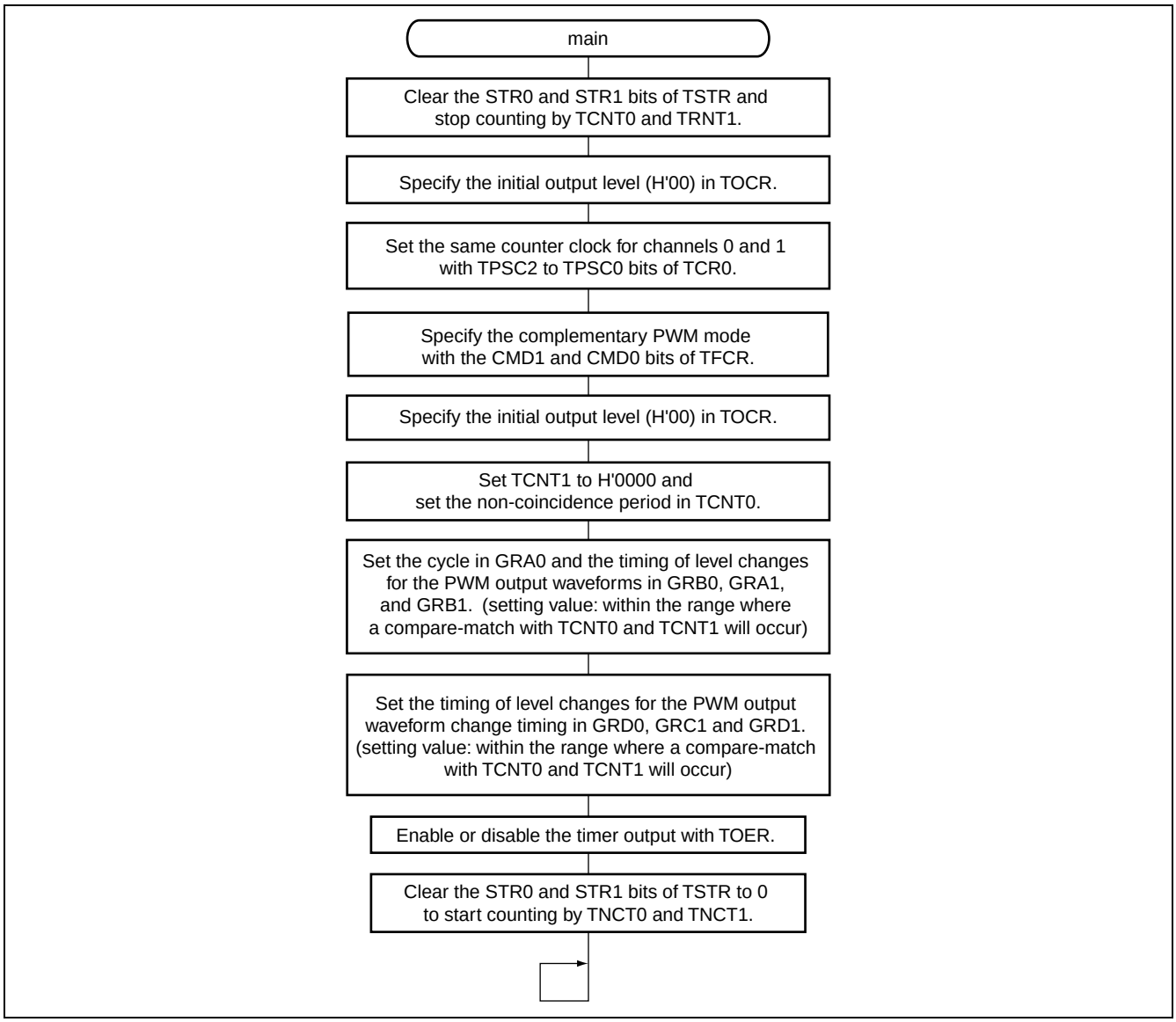
Register Names	Assigned Function	Used in (Module Name)
TSTR	Starts counting by the timer.	Main routine
TOCR	Specifies the initial output until the first compare-match occurs.	
TCR0	Selects the input clock (the same signal as is selected by TCR1).	
TCR1	Selects the input clock (the same signal as is selected by TCR0).	
TFCR	Specifies the complementary PWM mode.	
TMDR	Specifies GRC0, GRD0, GRC1 and GRD1 as the buffer registers for GRA0, GRB0, GRA1 and GRB1, respectively.	
TCNT0	Channel 0 timer counter	
TCNT1	Channel 1 timer counter	
GRA0	Specifies half of the period	Main routine Data specification
GRB0	Specifies the timer-counter value that gives level-change timing of the PWM waveforms output on FTIOB0 and FTIOD0	
GRC0	Buffer register for GRA0	Main routine Interrupt routine Data specification
GRD0	Buffer register for GRB0	
GRA1	Specifies the timer-counter value that gives level-change timing of the PWM waveforms output on FTIOA1 and FTIOC1.	Main routine Data specification
GRB1	Specifies the timer-counter value that gives level-change timing of the PWM waveforms output on FTIOB1 and FTIOD1.	
GRC1	Buffer register of GRA1	Main routine Interrupt routine Data specification
GRD1	Buffer register of GRB1	
TOER	Enables the timer output.	Main routine
TIER0	Enables the GRA0 interrupt.	

4.4 RAM usage

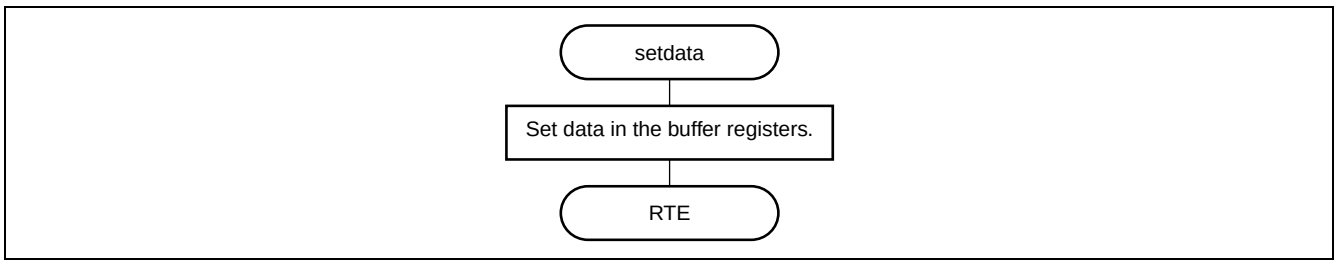
This task example uses no RAM other than the arguments (listed above).

5. Flowcharts

1. Main routine



2. Interrupt routine



6. Program Listing

```
/*********************************************************************/
/*                                                                   */
/*    H8/300HN Series -H8/3687-                                      */
/*    Application Note                                               */
/*                                                                   */
/*    'Complementry PMW Mode function'                               */
/*                                                                   */
/*    Function                                                       */
/*    :Timer Z Complementary PWM Mode                                */
/*                                                                   */
/*    External Clock:     16MHz                                      */
/*    Internal Clock:     16MHz                                      */
/*    Sub-clock:       32.768kHz                                     */
/*                                                                   */
/*********************************************************************/
#include    <C:\ch38\include\machine.h>

/*********************************************************************/
/*    Symbol Definition                                              */
/*********************************************************************/

struct BIT {
    unsigned char    b7:1;                                  /* bit7                    */
    unsigned char    b6:1;                                  /* bit6                    */
    unsigned char    b5:1;                                  /* bit5                    */
    unsigned char    b4:1;                                  /* bit4                    */
    unsigned char    b3:1;                                  /* bit3                    */
    unsigned char    b2:1;                                  /* bit2                    */
    unsigned char    b1:1;                                  /* bit1                    */
    unsigned char    b0:1;                                  /* bit0                    */
};
```

```
#define        TCR0        *(volatile unsigned char *)0xF700       /* Timer Control Register 0            */
#define        TIORA0      *(volatile unsigned char *)0xF701       /* Timer I/O Control Register A0       */
#define        TIORC0      *(volatile unsigned char *)0xF702       /* Timer I/O Control Register C0       */
#define        TSR0        *(volatile unsigned char *)0xF703       /* Timer Status Register 0             */
#define        TSR0_BIT    (*(struct BIT *)0xF703)                 /* Timer Status Register 0             */
#define        IMIFA_0     TSR0_BIT.b0                             /* Input Capture/Compare match Flag A  */
#define        TIER0       *(volatile unsigned char *)0xF704       /* Timer Interrupt Enable Register 0   */
#define        POCR0       *(volatile unsigned char *)0xF705       /* Port Output Level Control Register  */
#define        TCNT0       *(volatile unsigned short *)0xF706      /* Timer Counter 0                     */
#define        GRA0        *(volatile unsigned short *)0xF708      /* General Register A0                 */
#define        GRB0        *(volatile unsigned short *)0xF70A      /* General Register B0                 */
#define        GRC0        *(volatile unsigned short *)0xF70C      /* General Register C0                 */
#define        GRD0        *(volatile unsigned short *)0xF70E      /* General Register D0                 */

#define        TCR1        *(volatile unsigned char *)0xF710       /* Timer Control Register 1            */
#define        TIORA1      *(volatile unsigned char *)0xF711       /* Timer I/O Control Register A1       */
#define        TIORC1      *(volatile unsigned char *)0xF712       /* Timer I/O Control Register C1       */
#define        TSR1        *(volatile unsigned char *)0xF713       /* Timer Status Register 1             */
#define        TIER1       *(volatile unsigned char *)0xF714       /* Timer Interrupt Enable Register 0   */
#define        POCR1       *(volatile unsigned char *)0xF715       /* Port Output Level Control Register  */
#define        TCNT1       *(volatile unsigned short *)0xF716      /* Timer Counter 1                     */
#define        GRA1        *(volatile unsigned short *)0xF718      /* General Register A1                 */
#define        GRB1        *(volatile unsigned short *)0xF71A      /* General Register B1                 */
#define        GRC1        *(volatile unsigned short *)0xF71C      /* General Register C1                 */
#define        GRD1        *(volatile unsigned short *)0xF71E      /* General Register D1                 */

#define        TSTR        *(volatile unsigned char *)0xF720       /* Timer Start Register                */
#define        TMDR        *(volatile unsigned char *)0xF721       /* Timer Mode Register                 */
#define        TPMR        *(volatile unsigned char *)0xF722       /* Timer PWM Mode Register             */
#define        TFCR        *(volatile unsigned char *)0xF723       /* Timer Function Control Register     */
#define        TOER        *(volatile unsigned char *)0xF724       /* Timer Output Master Enable Register */
#define        TOCR        *(volatile unsigned char *)0xF725       /* Timer Output Master Enable Register */
}
#pragma        interrupt    (setdata)
/************************************************************************/
/* Function definition                                                  */
/************************************************************************/
extern    void    INIT ( void );                                    /* SP Set                              */
void      main      ( void );
void      setdata    ( void );
```

```
/*********************************************************************/
/*    RAM define                                                     */
/*********************************************************************/
unsigned char    duty_1;                                    /* Duty Setting Buffer 1              */
unsigned char    duty_2;                                    /* Duty Setting Buffer 2              */
unsigned char    duty_3;                                    /* Duty Setting Buffer 3              */
unsigned short   pul_cyc;                                   /* PWM cycle Data Set                 */
unsigned short   dead_time;                                 /* Dead Time Data Set                 */

extern void _INITSCT();

/*********************************************************************/
/*    Vector Address                                                 */
/*********************************************************************/
#pragma    section        V1                                /* VECTOR SECTION SET                 */
void (*const VEC_TBL1[])(void) = {                          /* 0x00 - 0x0f                        */
    INIT                                                    /* 00 Reset                           */
};

#pragma    section        V2                                /* VECTOR SECTION SET                 */
void (*const VEC_TBL2[])(void) = {
    setdata                                                 /* 34 Timer z(CH0) Interrupt          */
};

#pragma    section                                          /* P                                  */
/*********************************************************************/
/*    Main Program                                                   */
/*********************************************************************/
void main ( void )
{
   _INITSCT();

    set_imask_ccr(1);                                       /* Interrupt Disable                  */

     TSTR = 0xFC;                                           /* Timer Stop                         */
    TOCR = 0x00;                                            /* PWM initial output "0"             */

    TCR0 = 0x00;                                            /* No-clear mode                      */
    TCR1 = 0x00;                                            /* No-clear mode                      */
    TFCR = 0x0A;                                            /* Complementary PWM mode             */
    TMDR = 0xEE;                                            /* GRB0,GRA1,GRB1 buffered mode       */
```

```
    dead_time = 0x0000;

    TCNT0 = dead_time;                          /* No dead time                          */
    TCNT1 = 0x0000;

    pul_cyc = 0x190;                            /* Pulse period 50 us                    */
    duty_1 = 0x78;                              /* Duty cycle 30%                        */
    duty_2 = 0xC8;                              /* Duty cycle 50%                        */
    duty_3 = 0x140;                             /* Duty cycle 80%                        */
GRA0 = pul_cyc;                                 /* Pulse period 50 us                    */
    GRB0 = duty_1;                              /* Duty cycle 30%                        */
    GRA1 = duty_2;                              /* Duty cycle 50%                        */
    GRB1 = duty_3;                              /* Duty cycle 80%                        */

    GRD0 = duty_1;                              /* Duty cycle 30%                        */
    GRC1 = duty_2;                              /* Duty cycle 50%                        */
    GRD1 = duty_3;                              /* Duty cycle 80%                        */

    TOER = 0x00;                                /* FTIOB0,FTIO00,FTIOA1,FTIOB1,FTIOC1    */
                                                /* FTIOD1 Output Enable                  */

    TIER0 = 0x01;                               /* Interrupt Enable Disable              */

    TSTR = 0xFF;                                /* TCNT0,TCNT1 Start                     */

    set_imask_ccr(0);                           /* Interrupt Enable                      */

    while(1){
        ;
        }
}
```

```
/*********************************************************************/
/*    Timerz Interrupt                                               */
/*********************************************************************/
void setdata ( void )
{

     TSR = (TSR & 0xF7);                                    /* Clear IMIFA_0 to 0                */

     GRD0 = duty_1;
     GRC1 = duty_2;
     GRD1 = duty_3;

}
```

INIT.SRC (Program Listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

Link address specification:

Section Name	Address
CV1	H'0000
P	H'0100
B	H'FB80