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H8SX Family

Output of Long-Period Pulses by Cascade Connection of 16-Bit Timers

Introduction

Two 16-bit counters (channels 4 and 5) of the 16-bit timer pulse unit (TPU) are cascade-connected for operation as a 32-bit counter, which is used to output long-period pulses.

Target Devices

H8SX/1653 and H8SX/1638 Groups

Preface

Although the writing of this application note is in accord with the hardware manual for the H8SX/1653 Group, the program covered in this application note can be run on the target devices indicated above.

However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device.

Contents

1. Specifications

Figure 1 shows an example of long-period pulse output. Long-period pulses are output by employing PWM mode 1 and cascade connection.

With the cascade-connection function, the 16-bit counters of channels 4 and 5 are cascade-connected for operation as a 32-bit counter; that is, the channel-4 counter clock counts overflows of the channel-5 counter clock. Pulse output is obtained by placing channel 4 in PWM mode 1 and having two compare matches controls the output of 0 and 1.

The output pulse waveform has a period of 2.8 s with a width at low-level of 0.7 s.

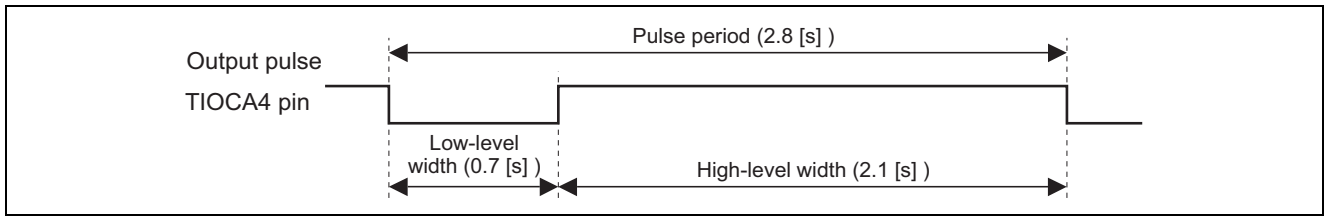


Figure 1 Example of Long-Period Pulse Output

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock	: 12 MHz
	System clock (Iϕ)	: 48 MHz (input clock frequency × 4)
	Peripheral module clock (Pϕ)	: 24 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 48 MHz (input clock frequency × 4)
Operating mode	Mode 7 (single-chip mode) Setting of mode pins: MD2 = 1, MD1 = 1, MD0 = 1, MD_CLK = 0	
Development tool	High-performance Embedded Workshop Ver.4.04.01	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Ver.6.02.00 (from Renesas Technology Corp.)	
	Option settings -cpu=h8sxa:24:md, -code=machinecode, -optimize=1, -regparam=3, -speed=(register,shift,struct,expression)	
Optimizing linkage editor	Optimizing Linkage Editor Ver.9.03.00 (from Renesas Technology Corp.)	
	Option setting -start=P/01000	

3. Description of Module Used

3.1 16-Bit Timer Pulse Unit (TPU)

Figure 2 shows a block diagram of the 16-bit timer pulse unit (TPU)

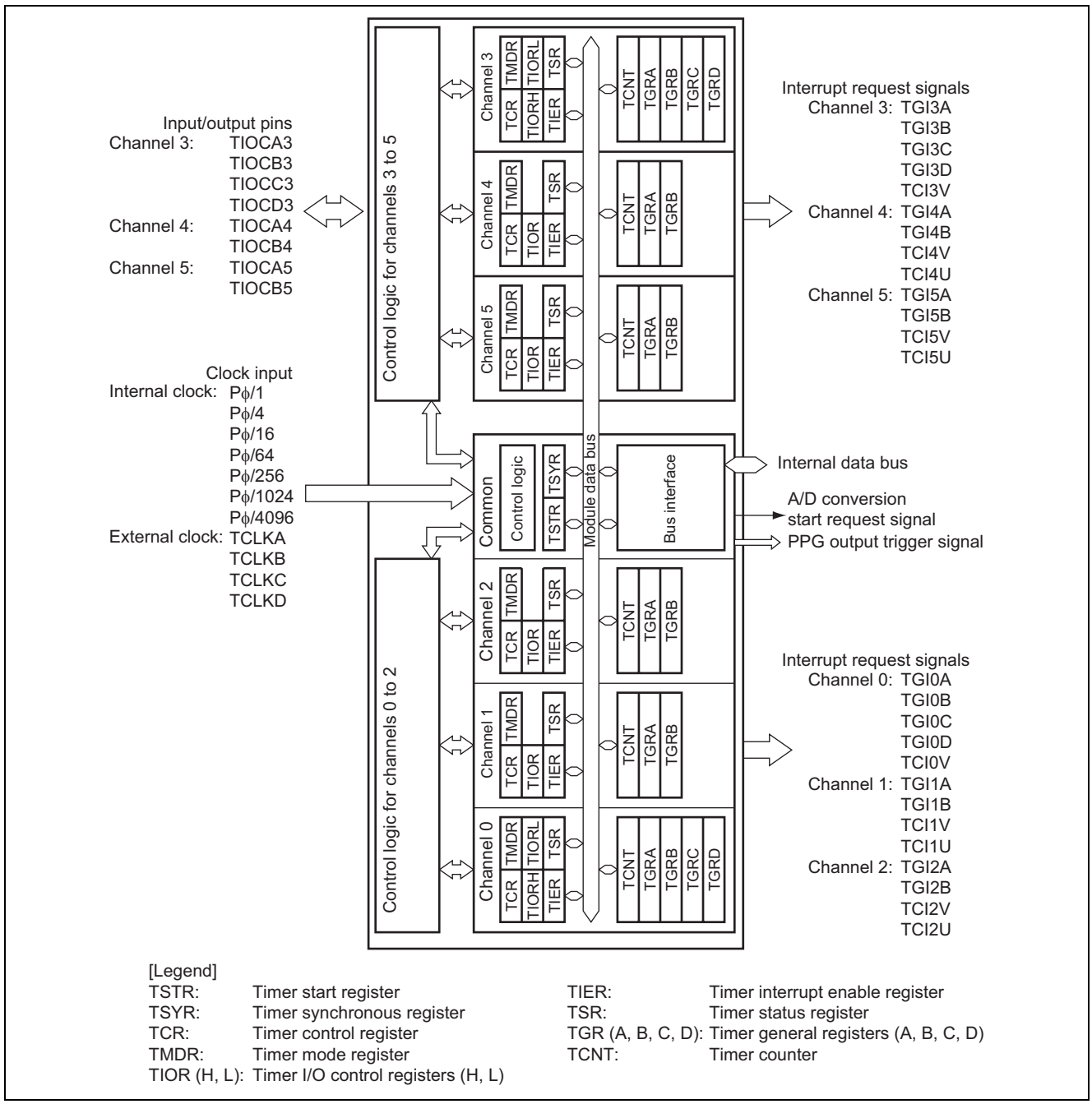


Figure 2 Block Diagram of the TPU

3.2 Cascade-Connected Operation

In the cascade-connected operation of 16-bit timer, two 16-bit counters for different channels are used together as a 32-bit counter. In this function, the channel-1 (channel-4) counter clock counts overflows/underflows of TCNT_2 (TCNT_5) as set in bits TPSC2 to TPSC0 in TCR.

Underflows only occur when the lower-order 16-bit TCNT is in phase-counting mode.

Table 2 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for channel 1 or 4, the counter clock setting is invalid and the counter operates independently in phase counting mode.

Table 2 Combinations for Cascade Connection

Combination	Upper 16 Bits	Lower 16 Bits
Channels 1 and 2	TCNT_1	TCNT_2
Channels 4 and 5	TCNT_4	TCNT_5

3.2.1 Example of Procedure for Setting Cascade-Connected Operation

Figure 3 shows an example of procedure for setting cascade-connected operation.

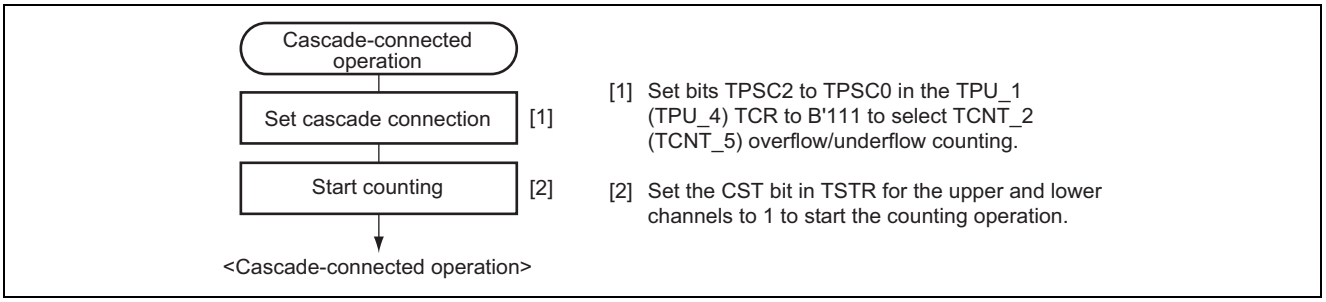


Figure 3 Example of Procedure for Setting Cascade-Connected Operation

3.3 PWM Modes

In PWM mode, PWM waveforms are output from the output pins. The output of 0 or 1, or toggling of the output, can be selected as the response to a compare match with each of the TGRs.

Settings of TGR registers can output a PWM waveform in the range of 0 to 100% duty cycle.

Designating TGR compare match as the counter clearing source enables the cycle to be set in that register. All channels can be designated for PWM mode independently. Synchronous operation is also possible.

There are two PWM modes, as described below.

1. PWM mode 1
   PWM output is generated from the TIOCA and TIOCC pins by pairing TGRA with TGRB and TGRC with TGRD. The outputs specified by bits IOA3 to IOA0 and IOC3 to IOC0 in TIOR are output from the TIOCA and TIOCC pins at compare matches A and C, respectively. The outputs specified by bits IOB3 to IOB0 and IOD3 to IOD0 in TIOR are output at compare matches B and D, respectively. The initial output value is the value set in TGRA or TGRC. If the set values of paired TGRs are identical, the output value does not change when a compare match occurs.
   In PWM mode 1, a maximum 4-phase PWM output is possible.
2. PWM mode 2
   PWM output is generated using one TGR as the cycle register and the others as duty cycle registers. The output specified in TIOR is performed by means of compare matches. Upon counter clearing by a synchronous register compare match, the output value of each pin is the initial value set in TIOR. If the set values of the cycle and duty cycle registers are identical, the output value does not change when a compare match occurs.
   In PWM mode 2, a maximum 7-phase PWM output is possible by combined use with synchronous operation.

Table 3 gives the correspondence between PWM output pins and registers.

Table 3 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Registers**	**PWM Mode 1**	**PWM Mode 2**
0	TGRA_0	—	—
	TGRB_0		
	TGRC_0		
	TGRD_0		
1	TGRA_1		
	TGRB_1		
2	TGRA_2		
	TGRB_2		
3	TGRA_3	TIOCA3	TIOCA3
	TGRB_3		TIOCB3
	TGRC_3	TIOCC3	TIOCC3
	TGRD_3		TIOCD3
4	TGRA_4	TIOCA4	TIOCA4
	TGRB_4		TIOCB4
5	TGRA_5	TIOCA5	TIOCA5
	TGRB_5		TIOCB5

Note: In PWM mode 2, PWM output is not possible for the TGR register in which the cycle is set.

3.3.1 Example of Procedure for Setting PWM Mode

Figure 4 shows an example of procedure for setting the PWM mode.

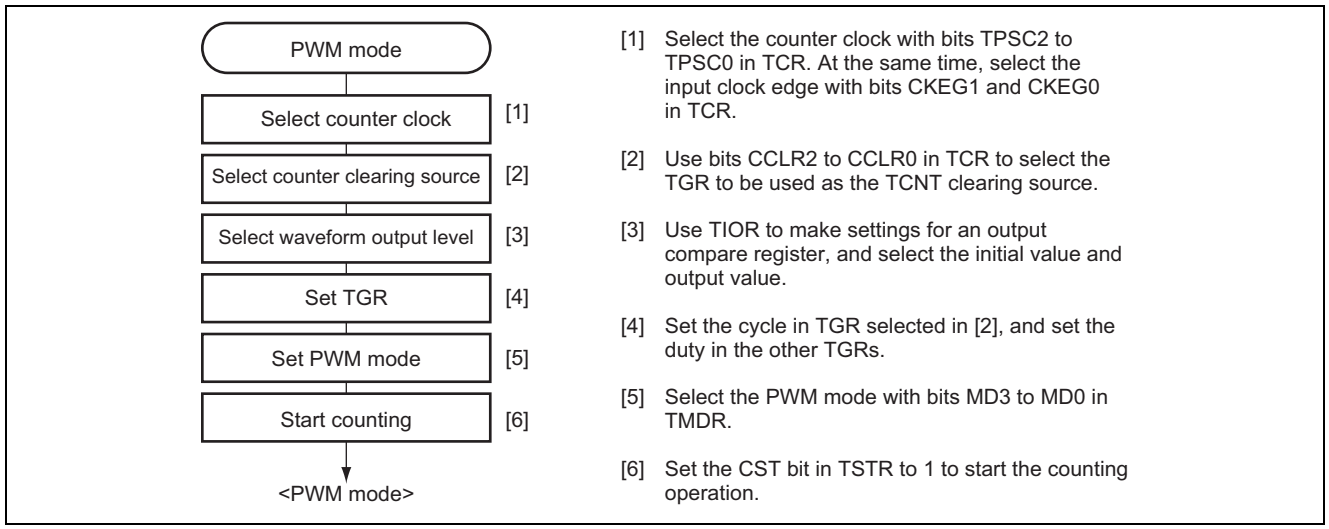


Figure 4 Example of Procedure for Setting PWM Mode

3.3.2 Examples of PWM Mode Operation

Figure 5 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the cycle, and the value set in TGRB register as the duty cycle.

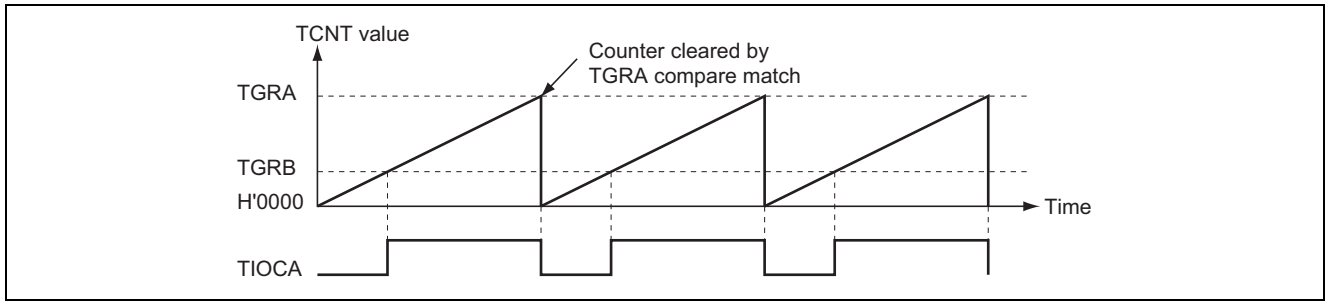


Figure 5 Example of PWM Mode Operation (1)

Figure 6 shows an example of PWM mode 2 operation.

In this example, synchronous operation is designated for channels 3 and 4, TGRB_4 compare match is set as the TCNT clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGR registers (TGRA_3 to TGRD_3, TGRA_4), to output a 5-phase PWM waveform.

In this case, the value set in TGRB_4 is used as the cycle, and the values set in the other TGRs as the duty cycle.

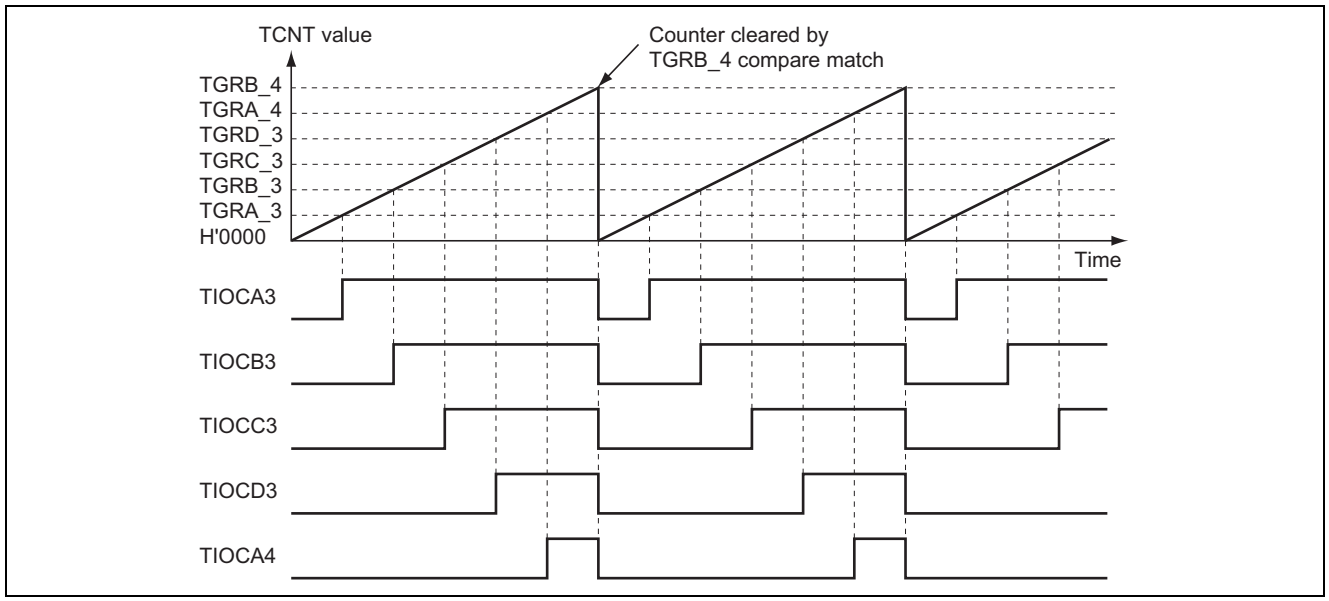


Figure 6 Example of PWM Mode Operation (2)

4. Description of Operation

4.1 Description of Output of Long-Period Pulses

The output of long-period pulses is obtained by cascade-connecting the channel-4 and channel-5 counters and placing channel 4 in PWM mode 1. When the counters are cascade-connected, TCNT_4 counts overflows of TCNT_5.

The output from the TIOCA4 pin turns to 1 on a compare match with TGRA_4 and to 0 on a compare match with TGRB_4. Additionally, TCNT_4 is cleared to H'0000 on a compare match with TGRB_4.

Figure 7 shows the timing of operations for the output of long-period pulses.

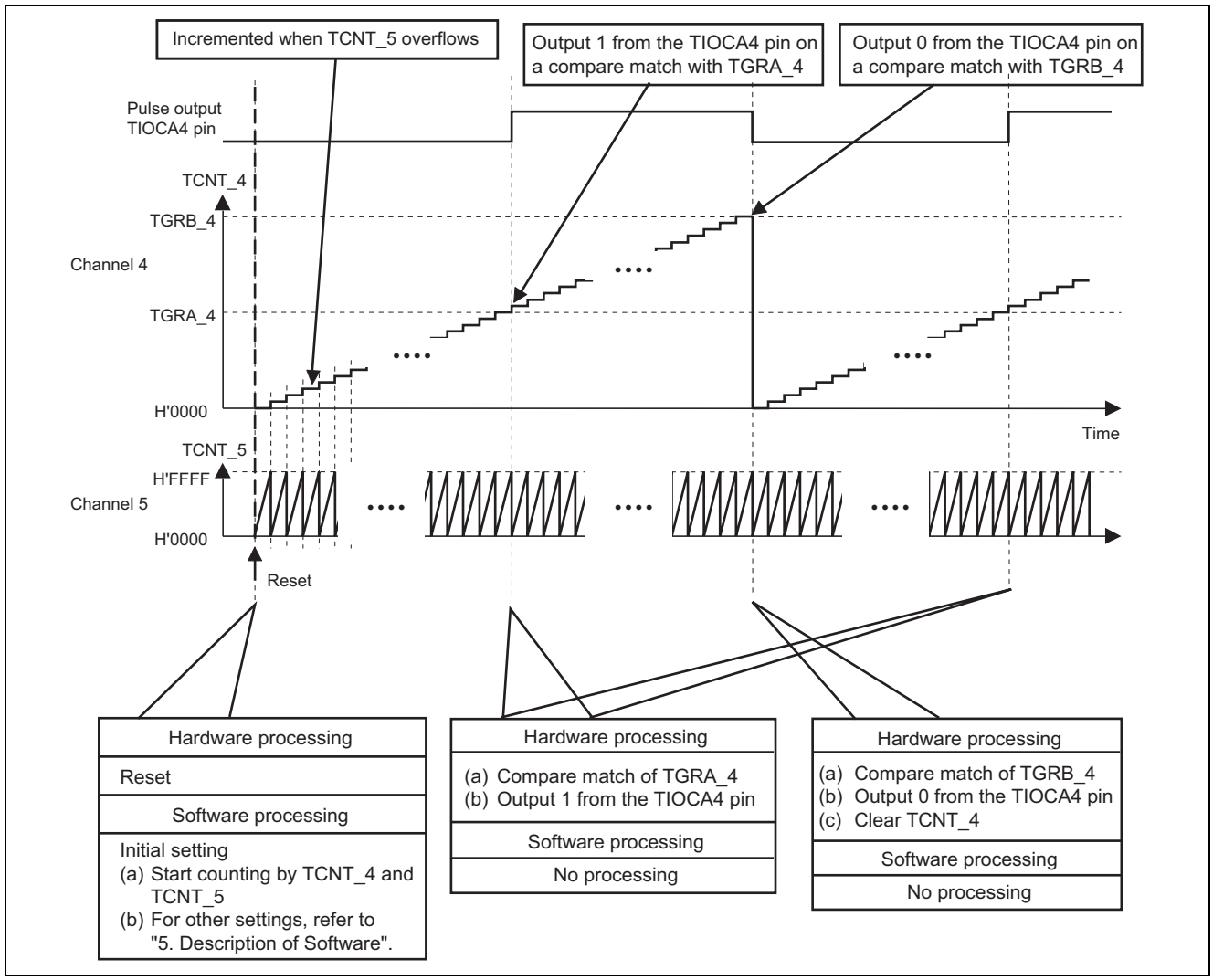


Figure 7 Timing of Operation to Output Long-Period Pulses

4.2 Formulas for Calculation of Pulse Output Values

The pulse period and low-level width of the pulse are calculated by the formulas below.

When Pϕ = 24 MHz and TGRB_4 = H'03FF,

$$\text{Pulse period} = \frac{(\text{TGRB\_4} + 1) \times \text{TCNT\_5 overflow count}}{P\phi}$$

$$= \frac{(\text{H'3FF} + 1) \times \text{H'10000}}{24\ \text{MHz}}$$

= 2.79 …… ≈ 2.8 s

When Pϕ = 24 MHz and TGRA_4 = H'00FF,

$$\text{Low-level width} = \frac{(\text{TGRA\_4} + 1) \times \text{TCNT\_5 overflow count}}{P\phi}$$

$$= \frac{(\text{H'FF} + 1) \times \text{H'10000}}{24\ \text{MHz}}$$

= 0.69 …… ≈ 0.7 s

5. Description of Software

5.1 Vector Table

Table 4 Vector Table for Interrupt Exception Handling

Exception Handling Source	Vector Number	Address in Vector Table	Destination Interrupt Processing Function
Reset	0	H'000000	init

5.2 List of Functions

Table 5 List of Functions

Name Functions	Description
init	Initialization routine Release the module from the module stop mode, configures the clocks and calls the main function.
main	Main routine Obtain long-period pulse output on the TIOCA4 pin by cascade-connecting channel-4 and channel-5 counters and setting channel 4 to PWM mode 1.

5.3 Description of Functions

5.3.1 init Function

1. Functional overview
   Initialization routine releases the module from the module stop mode, sets up the clocks, and calls the main function.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which
8	ICK0	0	R/W	is supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable The ACSE bit enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

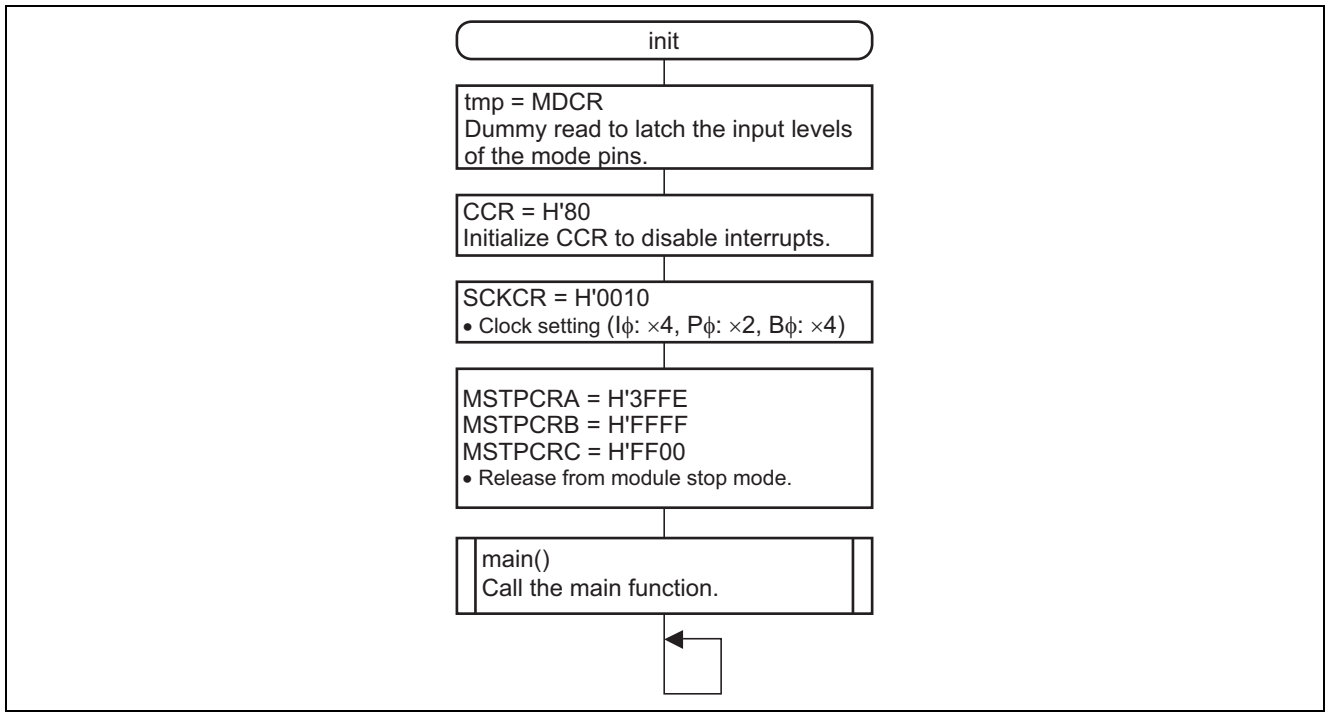
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.3.2 main Function

1. Functional overview
   Main routine obtains long-period pulse output on the TIOCA4 pin by cascade-connecting channel-4 and channel-5 counters and setting channel 4 to PWM mode 1.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port function control register 9 (PFCR9) Number of bits: 8 Address: H'FFFBC9

Bit	Bit Name	Setting	R/W	Function
6	TPUMS4A	0	R/W	TPU I/O Pin Multiplex Function Select This bit selects the TIOCA4 function. 0: Specifies P25 as the output compare output or input capture input pin 1: Specifies P24 as the input capture input pin and P25 as the output compare output pin

- Timer control register_4 (TCR_4) Number of bits: 8 Address: H'FFFEE0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	1	R/W	These bits select the TCNT_4 counter clearing condition.
5	CCLR0	0	R/W	010: TCNT_4 is cleared by TGRB compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	1	R/W	Timer Prescaler 2 to 0
1	TPSC1	1	R/W	These bits select the TCNT_4 counter clock.
0	TPSC0	1	R/W	111: TCNT_5 overflow/underflow signal

- Timer mode register_4 (TMDR_4) Number of bits: 8 Address: H'FFFEE1

Bit	Bit Name	Setting	R/W	Function
3	MD3	0	R/W	Modes 3 to 0
2	MD2	0	R/W	These bits set the timer operating mode.
1	MD1	1	R/W	0010: PWM mode 1
0	MD0	0	R/W	Note: When channel 4 is set in PWM mode 1, TGRA_4 and TGRB_4 are used in pair to generate PWM output on the TIOCA4 pin.

- Timer I/O control register_4 (TIOR_4) Number of bits: 8 Address: H'FFFEE2

Bit	Bit Name	Setting	R/W	Function
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	1	R/W	These bits specify the TGRB_4 function.
5	IOB1	0	R/W	0101: TGRB_4 functions as an output compare register.
4	IOB0	1	R/W	In PWM mode 1, the TIOCA4 pin outputs 0 as the initial output and 0 on compare match.
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the TGRA_4 function.
1	IOA1	1	R/W	0010: TGRA_4 functions as an output compare register.
0	IOA0	0	R/W	The TIOCA4 pin outputs 0 as the initial output and outputs 1 on compare match.

- Timer counter_4 (TCNT_4) Number of bits: 16 Address: H'FFFEE6
  Function: 16-bit readable/writable counter
  Setting: H'0000

- Timer general register A_4 (TGRA_4) Number of bits: 16 Address: H'FFFEE8
  Function: Used as an output compare register.
  Setting: H'00FF

- Timer general register B_4 (TGRB_4) Number of bits: 16 Address: H'FFFEEA
  Function: Used as an output compare register.
  Setting: H'03FF

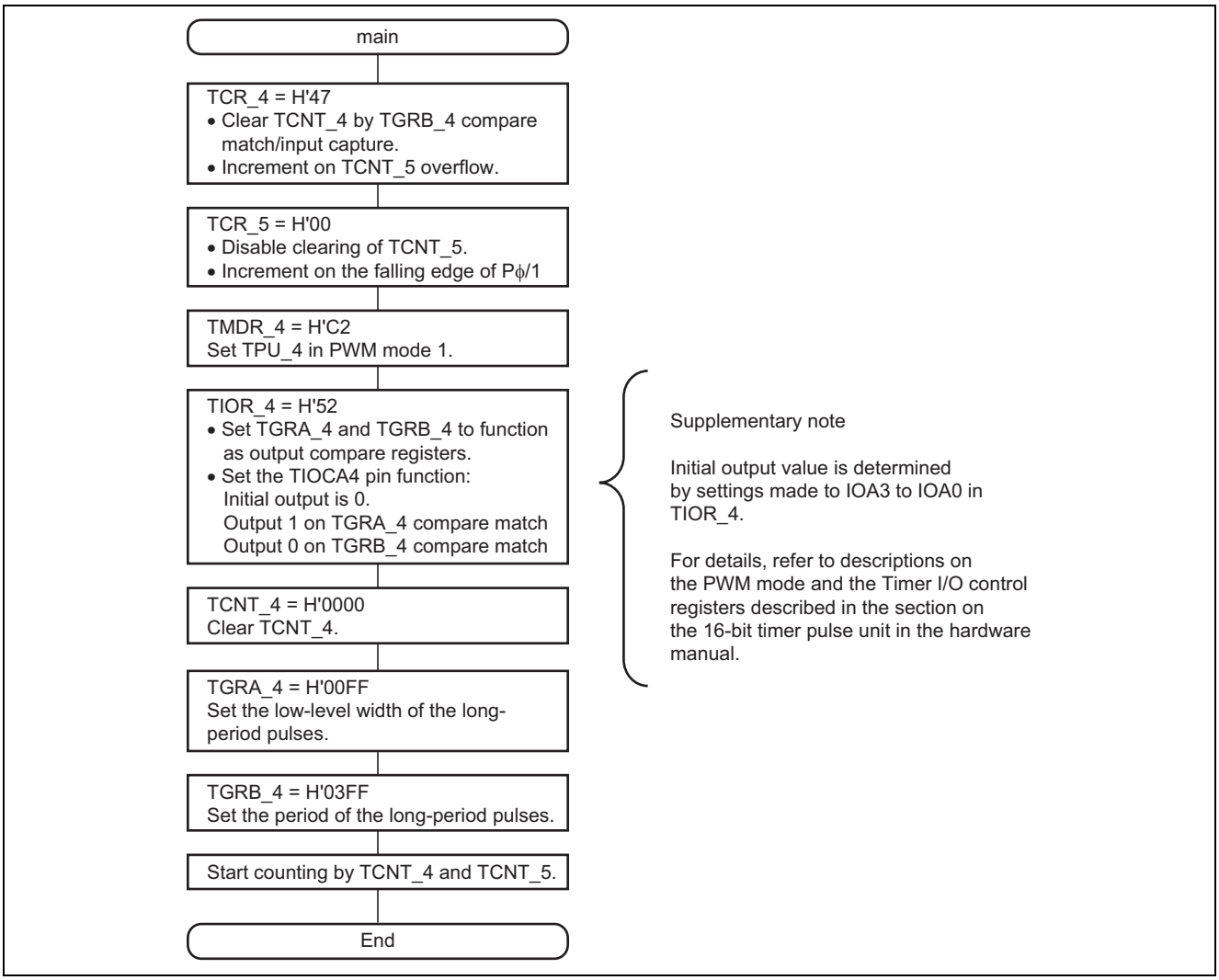
- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	1	R/W	Counter Start 5 to 0
4	CST4	1	R/W	These bits start or stop the operation of the corresponding TCNT.
3	CST3	0	R/W	0: Stops counting by TCNT_5 to TCNT_0
2	CST2	0	R/W	1: Starts counting by TCNT_5 to TCNT_0
1	CST1	0	R/W	
0	CST0	0	R/W	

- Timer control register_5 (TCR_5) Number of bits: 8 Address: H'FFEA41

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT_5 counter clearing condition.
5	CCLR0	0	R/W	000: Clearing of TCNT_5 is disabled
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT_5 counter clock.
0	TPSC0	0	R/W	000: Internal clock Pϕ/1

5. Flowchart


main
TCR_4 = H'47
• Clear TCNT_4 by TGRB_4 compare match/input capture.
• Increment on TCNT_5 overflow.
TCR_5 = H'00
• Disable clearing of TCNT_5.
• Increment on the falling edge of Pϕ/1
TMDR_4 = H'C2
Set TPU_4 in PWM mode 1.
TIOR_4 = H'52
• Set TGRA_4 and TGRB_4 to function as output compare registers.
• Set the TIOCA4 pin function:
Initial output is 0.
Output 1 on TGRA_4 compare match
Output 0 on TGRB_4 compare match
TCNT_4 = H'0000
Clear TCNT_4.
TGRA_4 = H'00FF
Set the low-level width of the long-period pulses.
TGRB_4 = H'03FF
Set the period of the long-period pulses.
Start counting by TCNT_4 and TCNT_5.
End
Supplementary note
Initial output value is determined by settings made to IOA3 to IOA0 in TIOR_4.
For details, refer to descriptions on the PWM mode and the Timer I/O control registers described in the section on the 16-bit timer pulse unit in the hardware manual.

6. Documents for Reference

- Hardware Manuals
  H8SX/1653 Group Hardware Manual
  H8SX/1638 Group Hardware Manual
  The most up-to-date versions of the documents are available on the Renesas Technology Website.

- Technical News/Technical Update
  The most up-to-date version of this document is available on the Renesas Technology Website.

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Inquiries
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csc@renesas.com

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.19.08	—	First edition issued

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