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M16C/64 Group

Operation of serial I/O (transmission in UART mode)

1. Abstract

In transmitting data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up		Item	Set-up	
Transfer clock source	O	Internal clock (f_{1SIO}/f_{2SIO}/f_{8SIO}/f_{32SIO})	Data logic select function	O	No reverse
		External clock (CLKi pin)			Reverse
$\overline{CTS}$ function	O	$\overline{CTS}$ function enabled	TXD, RXD I/O polarity reverse bit	O	No reverse
		$\overline{CTS}$ function disable			Reverse
Transmission interrupt factor		Transmission buffer empty	Bus collision detection function	O	Not selected
	O	Transmission complete			Selected

4. Operation

(1) Setting the transmit enable bit to “1” and writing transmission data to the UARTi transmit buffer register readies the data transmissible status.

(2) When input to the $\overline{CTSi}$ pin goes to “L”, transmission starts (the $\overline{CTSi}$ pin needs to be controlled on the reception side).

(3) Transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the TxDi pin. Then, data is transmitted, bit by bit, in sequence: LSB, ····, MSB, parity bit, and stop bit(s).

(4) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to “1”, which indicates that transmission is completed. At this time, the UARTi transmit interrupt request bit goes to “1”. The transfer clock stops at “H” level.

(5) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.

Figure 1 shows the operation timing.

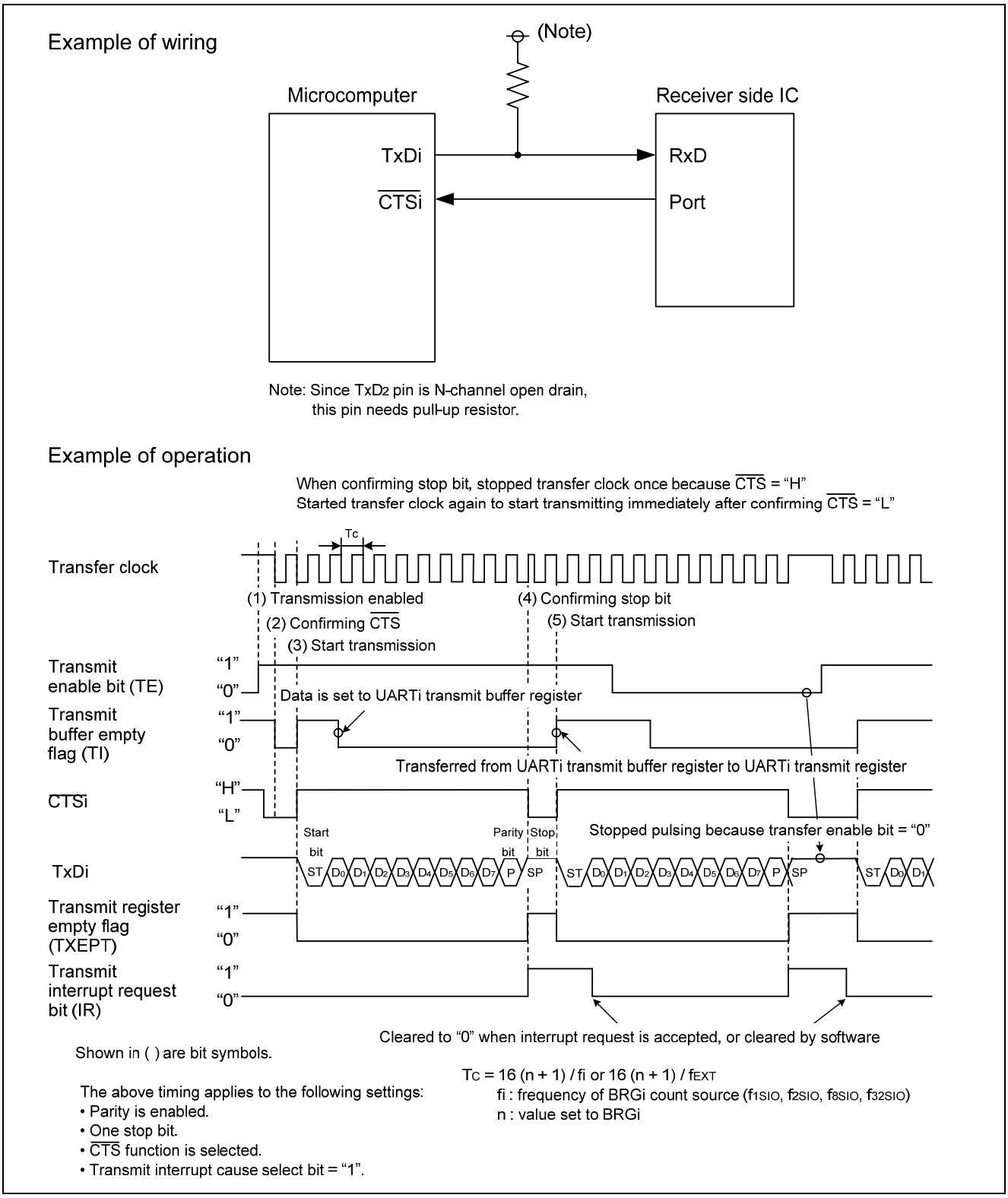
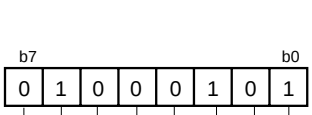


Figure 1. Operation timing of transmission in UART mode

5. Set-up procedure

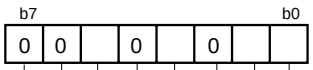
Setting UARTi transmit/receive mode register (i = 0 to 2, 5 to 7)



UART0 transmit/receive mode register [Address 0248h] U0MR
UART1 transmit/receive mode register [Address 0258h] U1MR
UART2 transmit/receive mode register [Address 0268h] U2MR
UART5 transmit/receive mode register [Address 0288h] U5MR
UART6 transmit/receive mode register [Address 0298h] U6MR
UART7 transmit/receive mode register [Address 02A8h] U7MR

Serial I/O mode select bit
b2 b1 b0
1 0 1 : Transfer data 8 bits long
Internal/external clock select bit
0 : Internal clock
Stop bit length select bit
0 : One stop bit
Odd/even parity select bit (Valid when bit 6 = “1”)
0 : Odd parity
Parity enabled bit
1 : Parity enabled
TxD, RxD I/O polarity reverse bit
Usually set to “0”

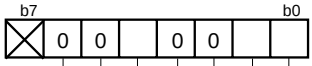
Setting UARTi transmit/receive control register (i = 0 to 2, 5 to 7)



UART0 transmit/receive control register [Address 024Ch] U0C0
UART1 transmit/receive control register [Address 025Ch] U1C0
UART2 transmit/receive control register [Address 026Ch] U2C0
UART5 transmit/receive control register [Address 028Ch] U5C0
UART6 transmit/receive control register [Address 029Ch] U6C0
UART7 transmit/receive control register [Address 02ACh] U7C0

UiBRG count source select bit
b1 b0
0 0 : f_{1SIO} or f_{2SIO} is selected
0 1 : f_{8SIO} is selected
1 0 : f_{32SIO} is selected
1 1 : Do not set to this value
$\overline{CTS}/\overline{RTS}$ function select bit (Valid when bit4 = “0”)
0 : $\overline{CTS}$ function is selected
Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (transmission completed)
$\overline{CTS}/\overline{RTS}$ disable bit
0 : $\overline{CTS}/\overline{RTS}$ function enabled
Data output select bit
0 : Pins TxDi/SDAi and SCLi are CMOS output
1 : Pins TxDi/SDAi and SCLi are N-channel open-drain output
Must always be “0” in UART mode
Transfer format select bit
0 : LSB first

Setting UART transmit/receive control register 2



UART transmit/receive control register 2 [Address 0250h] UCON

UART0 transmit Interrupt cause select bit
1 : Transmission completed (TXEPT = 1)

UART1 transmit Interrupt cause select bit
1 : Transmission completed (TXEPT = 1)

Must always be “0” in UART mode

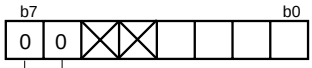
Must always be “0” in UART mode

Invalid in UART mode

Must always be “0” in UART mode

Separate UART0 $\overline{\text{CTS}}/\overline{\text{RTS}}$ bit
0 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ shared pin

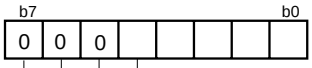
Setting UARTi transmit/receive control register 1 (i = 0 to 2, 5 to 7)



UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Data logic select bit
0 : No reverse

Error signal output enable bit
0 : Output disable



UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

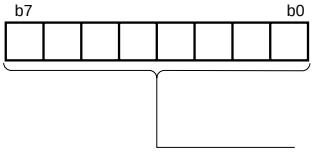
UARTi transmit Interrupt cause select bit
1 : Transmission completed (TXEPT = 1)

Must always be “0” in UART mode

Data logic select bit
0 : No reverse

Error signal output enable bit
0 : Output disable

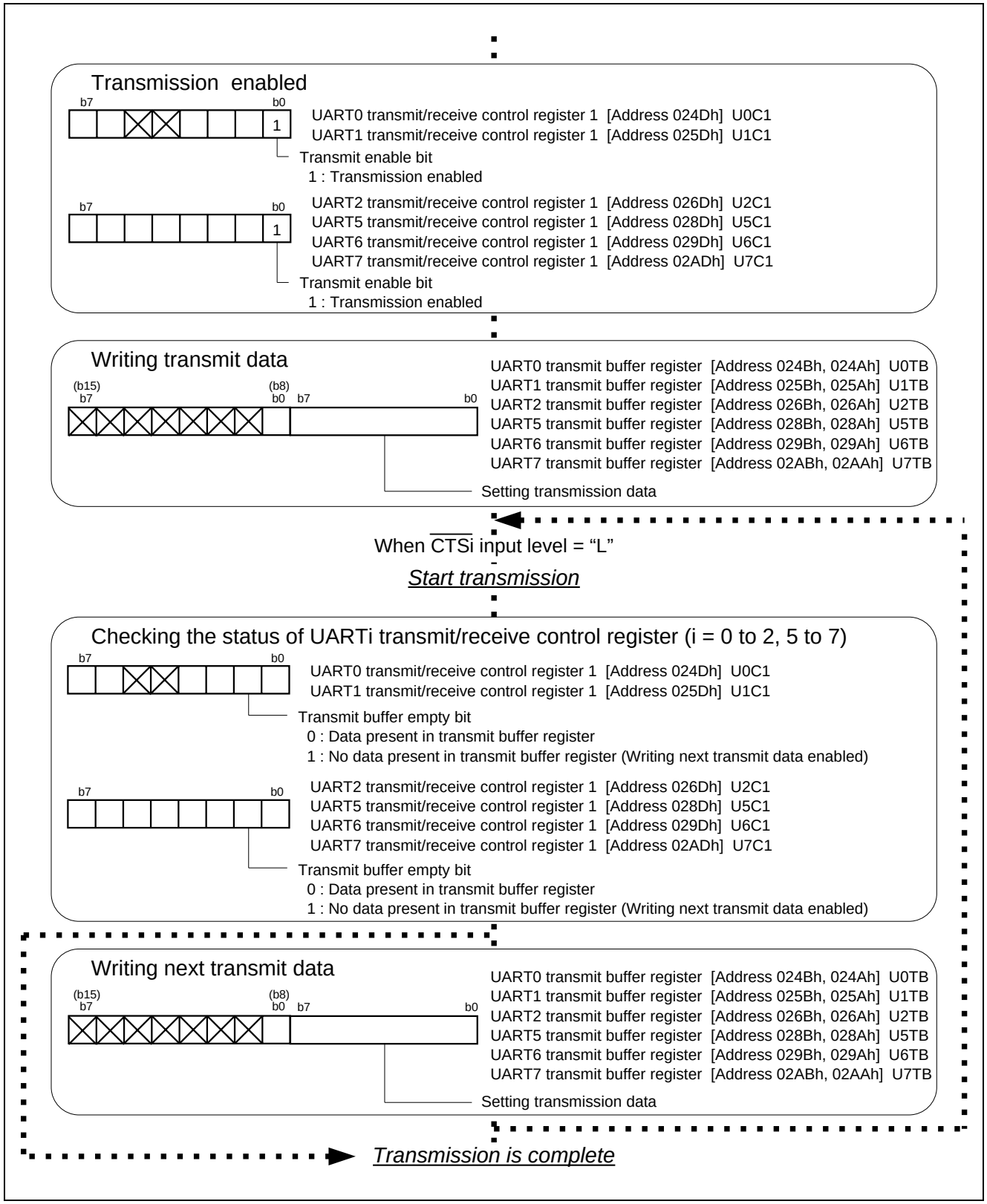
Setting UARTi bit rate register (i = 0 to 2, 5 to 7)



UART0 bit rate register [Address 0249h] U0BRG
UART1 bit rate register [Address 0259h] U1BRG
UART2 bit rate register [Address 0269h] U2BRG
UART5 bit rate register [Address 0289h] U5BRG
UART6 bit rate register [Address 0299h] U6BRG
UART7 bit rate register [Address 02A9h] U7BRG

Can be set to 00h to FFh (Note)

Note : Write to UARTi bit rate register when transmission/reception is halted.


Transmission enabled
b7
b0
1
UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1
Transmit enable bit
1 : Transmission enabled
b7
b0
1
UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1
Transmit enable bit
1 : Transmission enabled
Writing transmit data
(b15)
(b8)
b7
b0
b7
b0
UART0 transmit buffer register [Address 024Bh, 024Ah] U0TB
UART1 transmit buffer register [Address 025Bh, 025Ah] U1TB
UART2 transmit buffer register [Address 026Bh, 026Ah] U2TB
UART5 transmit buffer register [Address 028Bh, 028Ah] U5TB
UART6 transmit buffer register [Address 029Bh, 029Ah] U6TB
UART7 transmit buffer register [Address 02ABh, 02AAh] U7TB
Setting transmission data
When CTSi input level = "L"
Start transmission
Checking the status of UARTi transmit/receive control register (i = 0 to 2, 5 to 7)
b7
b0
UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1
Transmit buffer empty bit
0 : Data present in transmit buffer register
1 : No data present in transmit buffer register (Writing next transmit data enabled)
b7
b0
UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1
Transmit buffer empty bit
0 : Data present in transmit buffer register
1 : No data present in transmit buffer register (Writing next transmit data enabled)
Writing next transmit data
(b15)
(b8)
b7
b0
b7
b0
UART0 transmit buffer register [Address 024Bh, 024Ah] U0TB
UART1 transmit buffer register [Address 025Bh, 025Ah] U1TB
UART2 transmit buffer register [Address 026Bh, 026Ah] U2TB
UART5 transmit buffer register [Address 028Bh, 028Ah] U5TB
UART6 transmit buffer register [Address 029Bh, 029Ah] U6TB
UART7 transmit buffer register [Address 02ABh, 02AAh] U7TB
Setting transmission data
Transmission is complete

6. Reference

Hardware manual

M16C/64 Group Hardware Manual

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