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M16C/65 Group

Operation of serial I/O (transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up		Item	Set-up	
Clock prior to division select	O	f1	Transfer format	O	LSB first
		foco-F			MSB first
Peripheral clock	O	f_{1SIO}	Transmission interrupt factor		Transmission buffer empty
		f_{2SIO}		O	Transmission complete
Transfer clock source	O	Internal clock (f_{1SIO}/f_{2SIO}/f_{8SIO}/f_{32SIO})	Output transfer clock to multiple pins (Note 1)		Not selected
		External clock (CLKi pin)		O	Selected
$\overline{CTS}$ function		$\overline{CTS}$ function enabled	Serial data logic	O	No reverse
	O	$\overline{CTS}$ function disable			Reverse
CLK polarity	O	Output transmission data at the falling edge of the transfer clock			
		Output transmission data at the rising edge of the transfer clock			

Note 1: This can be selected only when UART1 is used in combination with the internal clock.

4. Operation

(1) Setting the transmit enable bit to “1” makes data transmissible status ready.

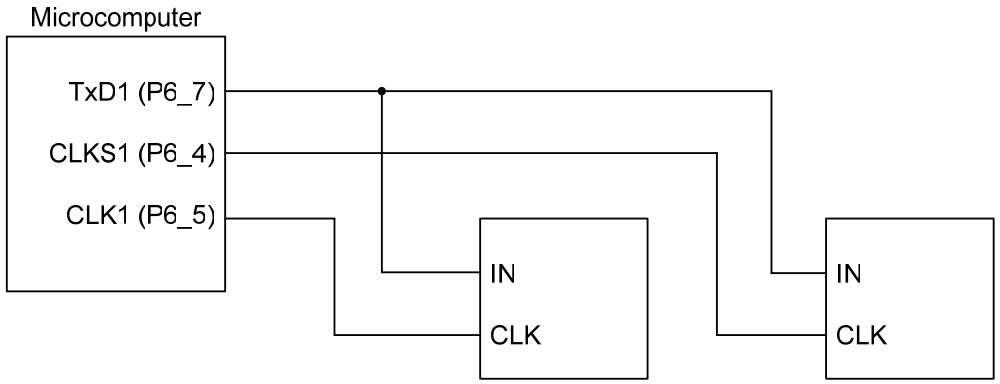
(2) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.

(3) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that the transmission is completed. The transfer clock stops at “H” level. At this time, the UART1 transmit interrupt request bit goes to “1”.

(4) Setting CLK/CLKS select bit 1 to “1” and setting CLK/CLKS select bit 0 to “1” causes the CLKS1 pin to go to the transfer clock output pin. Change the transfer clock output pin when transmission is halted.

Figure 1 shows the operation timing.

Example of wiring



Note: This applies when performing only transmission with an internal clock selected in the clock synchronous serial I/O mode.

Example of operation

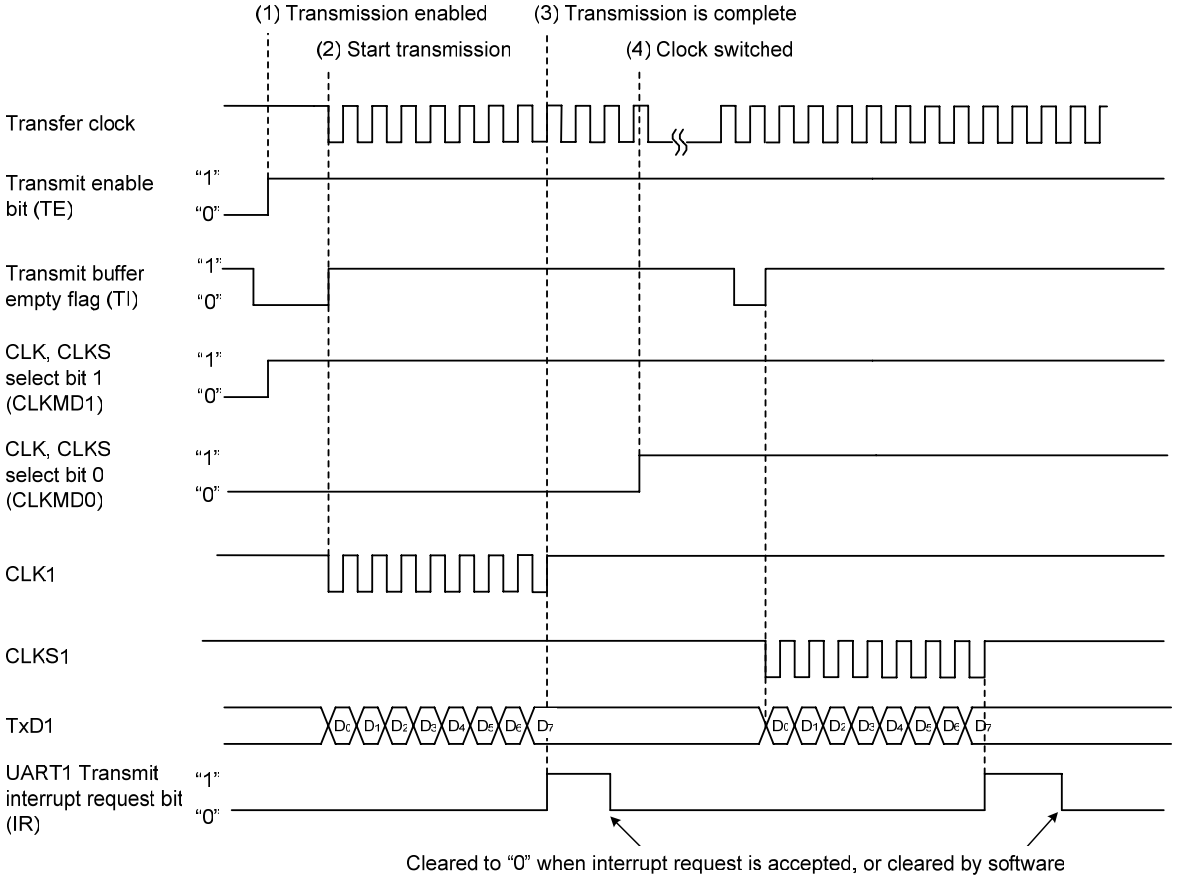
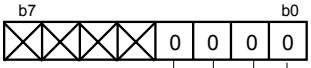


Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected

5. Set-up procedure

Setting UART clock select register

(Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.)



UART clock select register [Address 0252h] UCLKSEL0

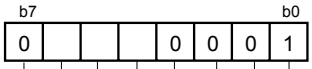
Set to "0"

UART0 to UART2 clock prior to division select bit
0 : f_1

UART5 to UART7 clock prior to division select bit
0 : f_1

Note: Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.

Setting UART1 transmit/receive mode register



UART1 transmit/receive mode register [Address 0258h]
U1MR

Must be fixed to "001"

Internal/external clock select bit
0 : Internal clock

Invalid in clock synchronous I/O mode

Invalid in clock synchronous I/O mode

Invalid in clock synchronous I/O mode

TxD, RxD I/O polarity reverse bit
Usually set to "0"

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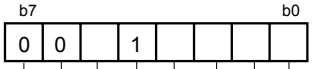
Setting UART1 transmit/receive control register 0



UART1 transmit/receive control register [Address 025Ch] U1C0

UiBRG count source select bit
b1 b0
0 0 : f_{1SIO} or f_{2SIO} is selected (Note1)
0 1 : f_{8SIO} is selected
1 0 : f_{32SIO} is selected
1 1 : Do not set to this value

$\overline{CTS}/\overline{RTS}$ function select bit (Valid when bit4 = "0")

Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (transmission completed)

$\overline{CTS}/\overline{RTS}$ disable bit
1 : $\overline{CTS}/\overline{RTS}$ function disabled

Data output select bit
0 : Pins TxDi/SDAi and SCLi are CMOS output
1 : Pins TxDi/SDAi and SCLi are N-channel open-drain output

CLK polarity select bit
0 : Transmission data is output at falling edge of transfer clock and reception data is input at rising edge

Transfer format select bit
0 : LSB first

Note 1: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f_{1SIO}. When the PCLK0 bit is "0", the selected clock source is f_{2SIO}.

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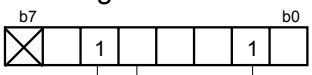
Setting UART transmit/receive control register 2



UART transmit/receive control register 2 [Address 0250h]
UCON

UART1 transmit interrupt cause select bit
0 : Transmit buffer empty (TI = 1)

CLK/CLKS select bit 0
0 : Clock output to CLK1
1 : Clock output to CLKS1

UART1 CLK/CLKS select bit 1
1 : Transfer clock output from multiple pins function selected

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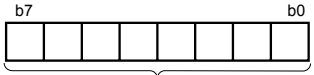
▪

Setting UART1 bit rate register



UART1 bit rate register [Address 0259h]
U1BRG

Can be set to 00h to FFh (Note)

Note : Write to the UiBRG register while serial interface is neither transmitting nor receiving. Use MOV instruction to write to the UiBRG register. Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.

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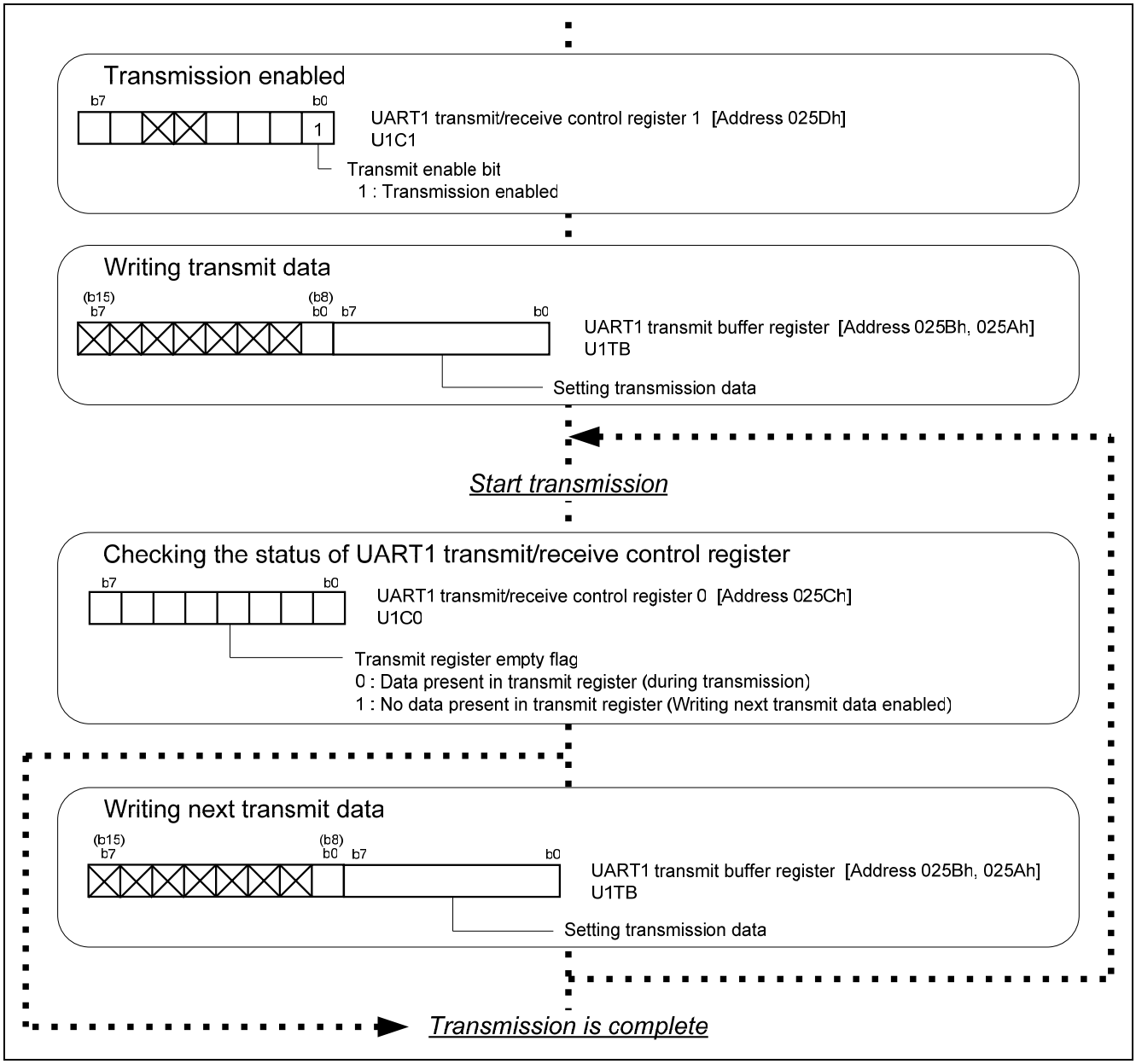
Transmission enabled
b7
b0
1
UART1 transmit/receive control register 1 [Address 025Dh]
U1C1
Transmit enable bit
1 : Transmission enabled
Writing transmit data
(b15)
(b8)
b7
b0
b7
b0
UART1 transmit buffer register [Address 025Bh, 025Ah]
U1TB
Setting transmission data
Start transmission
Checking the status of UART1 transmit/receive control register
b7
b0
UART1 transmit/receive control register 0 [Address 025Ch]
U1C0
Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (Writing next transmit data enabled)
Writing next transmit data
(b15)
(b8)
b7
b0
b7
b0
UART1 transmit buffer register [Address 025Bh, 025Ah]
U1TB
Setting transmission data
Transmission is complete

6. Reference

Hardware manual

M16C/65 Group Hardware Manual
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