

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## M16C/62A Group

Operation of Serial I/O (transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

### 1.0 Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

**Table 1. Chosed functions**

Item	Set-up		Item	Set-up	
Transfer clock source	<input type="radio"/>	Internal clock (f <sub>1</sub> / f <sub>8</sub> / f <sub>32</sub> )	Transmission interrupt factor		Transmission buffer empty
		External clock (CLKi pin)		<input type="radio"/>	Transmission complete
CTS function		CTS function enabled	Output transfer clock to multiple pins (Note 1)		Not selected
	<input type="radio"/>	CTS function disabled		<input type="radio"/>	Selected
CLK polarity	<input type="radio"/>	Output transmission data at the falling edge of the transfer clock	Data logic select function (Note 2)	<input type="radio"/>	No reverse
		Output transmission data at the rising edge of the transfer clock			Reverse
Transfer clock	<input type="radio"/>	LSB first	TxD, RxD I/O polarity reverse bit (Note 2)	<input type="radio"/>	No reverse
		MSB first			Reverse

**Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 CTS/RTS function can not be utilized. Set the UART1 CTS/RTS disable bit to "1".**

**Note 2: UART2 only.**

### 2.0 Introduction

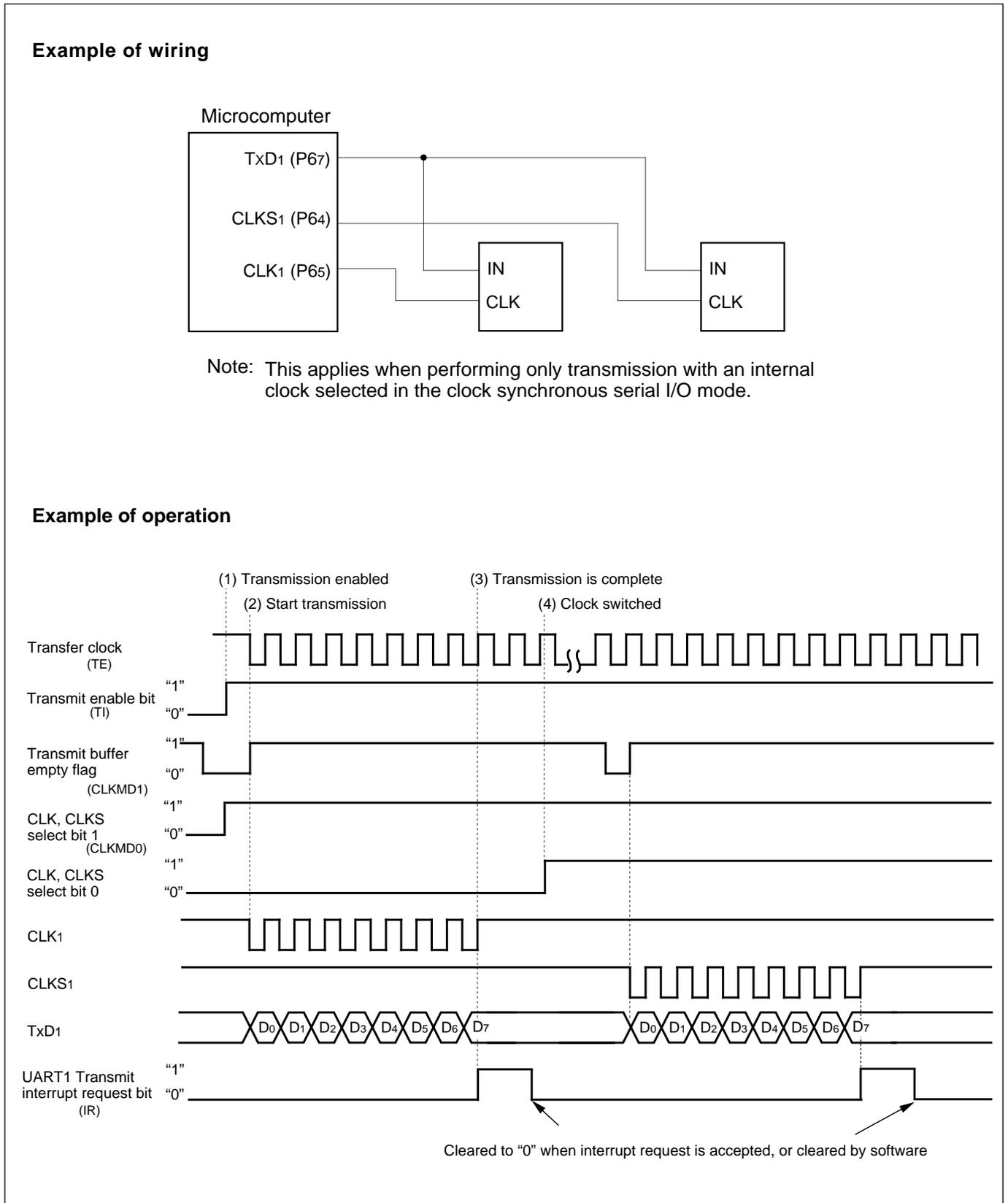
Operation (1) Setting the transmit enable bit to "1" makes data transmissible status ready.

(2) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.

(3) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that the transmission is completed. The transfer clock stops at "H" level. At this time, the UART1 transmit interrupt request bit goes to "1".

(4) Setting CLK/CLKS select bit 1 to "1" and setting CLK/CLKS select bit 0 to "1" causes the CLKs1 pin to go to the transfer clock output pin. Change the transfer clock output pin when transmission is halted.

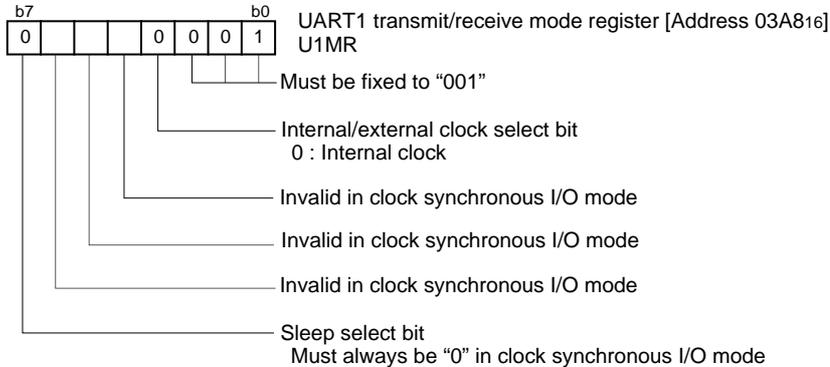
Figure 1 shows the operation timing



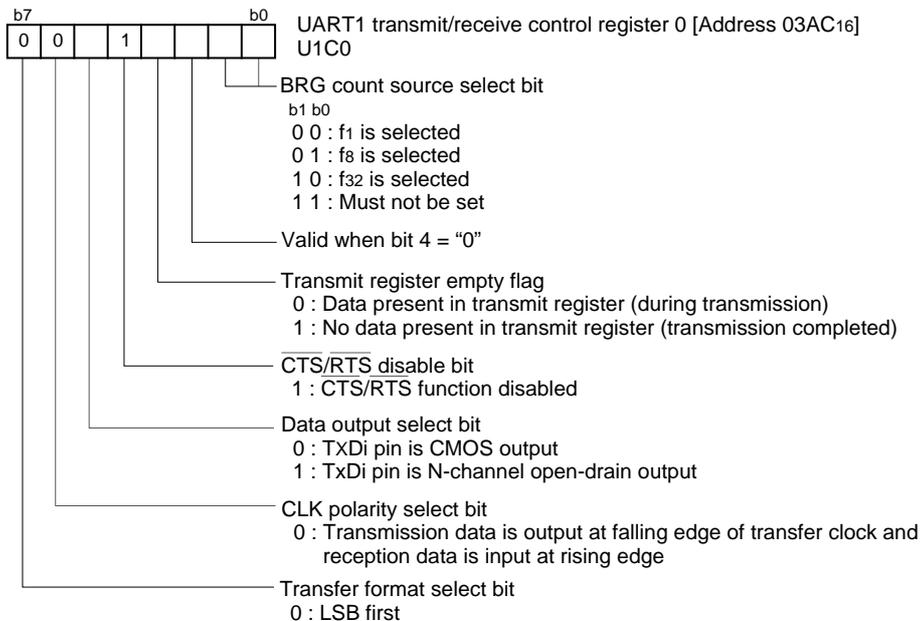
**Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected**

### 3.0 Set-up procedure

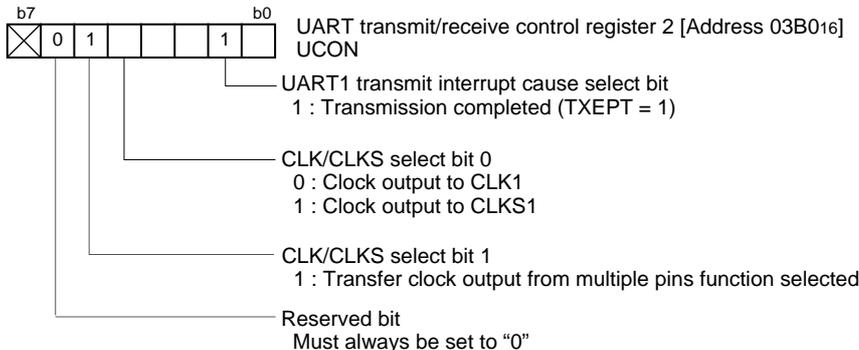
#### Setting UART1 transmit/receive mode register



#### Setting UART1 transmit/receive control register 0



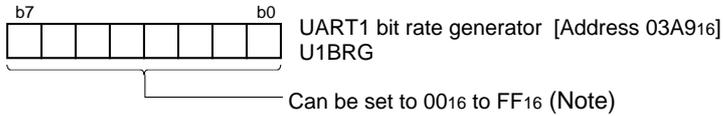
#### Setting UART transmit/receive control register 2



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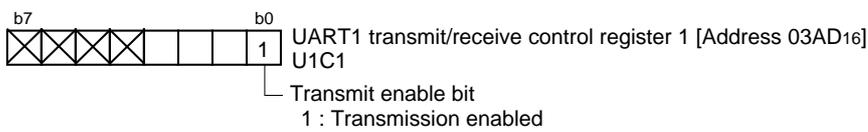
Continued from the previous page

### Setting UART1 bit rate generator

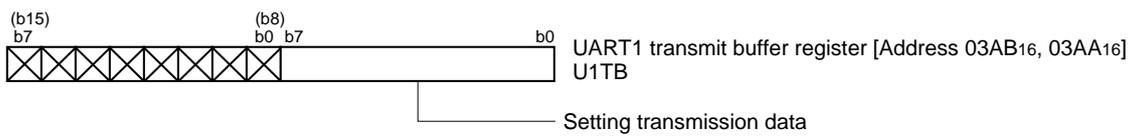


Note: Write to UART1 bit rate generator when transmission/reception is halted.

### Transmission enabled

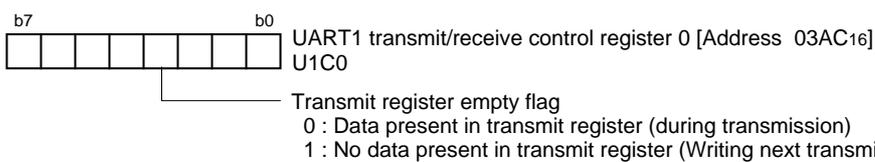


### Writing transmit data

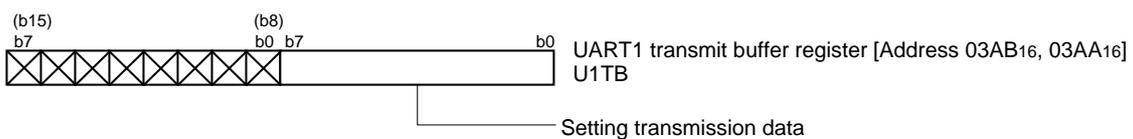


Start transmission

### Checking the status of UART1 transmit/receive control register



### Writing next transmit data



Transmission is complete



```

; Clears WORKRAM area
MOV.W #0, R0
MOV.W #(RAM_END-RAM_TOP)/2, R3
MOV.W #WORKRAM_TOP, A1
SSTR.W

; Makes transmission data for sample ( 1 to C_DATA_SIZE )
MOV.B #1, R0L ;1st data
MOV.W #0, A0 ;Initialize offset address
MAKE_DATA:
;
MOV.B R0L, v_Trans_data[A0] ;
ADD.B #1, R0L ;
ADD.W #1, A0 ;
CMP.W #C_DATA_SIZE, A0 ;
JLTU MAKE_DATA ;
;
;=====
; Serial I/O (transmission in clock-synchronous serial I/O mode,
; transfer clock output from multiple pins function selected)
;=====
MOV.B #00000001B, ulmr ;Setting UART1 transmit/receive mode register
;
; ||| |+++-----;Must be fixed to "001"
;
; ||| |+-----;Internal/external clock select bit (0:Internal clock)
;
; |+++-----;Invalid in clock synchronous I/O mode
;
; +-----;Sleep select bit
;
; (Must always be "0" in clock synchronous I/O mode)
MOV.B #00011000B, ulc0 ;Setting UART1 transmit/receive control register 0
;
; ||| | |+++-----;BRG count source select bit (00:f1 is selected)
;
; ||| | |+-----;(Valid when bit 4="0")
;
; ||| |+-----;Transmit register empty flag
;
; || |+-----;CTS/RTS disable bit (1:CTS/RTS function disabled)
;
; | +-----;Data output select bit (0:TxDi pin is CMOS output)
;
; | +-----;CLK polarity select bit
;
; | (0:Transmission data is output at falling edge of
; | transfer clock and
; | reception data is input at rising edge)
;
; | +-----;Transfer format select bit (0:LSB first)
;
MOV.B #00100010B, ucon ;Setting UART transmit/receive control register 2
;
; ||| +-----;UART1 transmit interrupt cause select
;
; ||| (1:Transmission completed(TXEPT=1))
;
; || +-----;CLK/CLKS select bit 0 (0:Clock output to CLK1)
;
; || (1:Clock output to CLKS1)
;
; | +-----;CLK/CLKS select bit 1
;
; | (1:Transfer clock output from multiple pins function
; | selected)
;
; | +-----;Reserved bit (Must always be set to "0")
;
MOV.B #07H, ulbrg ;Setting UART1 bit rate generator (1MHz, @16MHz f1)
MOV.B #00000001B, ulc1 ;Transmission enabled
;
; +-----;Transmission enabled
;
;

```

```

=====
;
;   Main program
=====
      MOV.W   #0, A0           ;Initialize offset
WRITE_DATA:
      MOV.B   v_Trans_data[A0], ultbl  ;Writing transmit data
                                           ;Start transmission
;
WAIT_TRANS:
      BTST   txept_ulc0           ;Checking the status of transmit register
      JNC    WAIT_TRANS
      ; Transmission complete.

      ; Change the transfer clock output pin when transmission and reception have completed
      ; if it is necessary.
      ; Writing next transmit data is enabled.
;
PREPARE_NEXT_DATA:
      ADD.W   #1, A0
      AND.W   #(C_DATA_SIZE-1), A0
      JNZ    WRITE_DATA
;
COMPLETE_TRANS:
      JMP     COMPLETE_TRANS
;
=====
;
;   Dummy interrupt processing program
=====
dummy:
      REIT
;
;*****
;   Setting of fixed vector
;*****
      .SECTION   F_VECT, ROMDATA
      .ORG       FIXED_VECT_TOP
;
      .LWORD    dummy      ;Undefined instruction interrupt vector
      .LWORD    dummy      ;Overflow (INT0 instruction) interrupt vector
      .LWORD    dummy      ;BRK instruction interrupt vector
      .LWORD    dummy      ;Address match interrupt vector
      .LWORD    dummy      ;Single-step interrupt vector
      .LWORD    dummy      ;Watchdog timer interrupt vector
      .LWORD    dummy      ;DBC interrupt vector
      .LWORD    dummy      ;NMI interrupt vector
      .LWORD    RESET      ;Sets reset vector
;
      .END

```

**5.0 Reference****Renesas Technology Corporation Semiconductor Home page**

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**Data Sheet**

M16C/62A group Rev. C.1

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M16C/62A group Rev. 1.0

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