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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of Serial I/O (transmission in clock-synchronous serial I/O mode)

1.0 Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosen functions

Item	Set-up	Item	Set-up
Transfer clock source	○ Internal clock (f ₁ / f ₈ / f ₃₂)	Transmission interrupt factor	○ Transmission buffer empty
	External clock (CLKi pin)		Transmission complete
CTS function	○ CTS function enabled	Output transfer clock to multiple pins (Note 1)	○ Not selected
	CTS function disabled		Selected
CLK polarity	○ Output transmission data at the falling edge of the transfer clock	CTS / RTS separation function (Note 2)	○ Pin shared by CTS and RTS
	Output transmission data at the rising edge of the transfer clock		CTS and RTS separated
Transfer clock	○ LSB first	Data logic select function (Note 3)	○ No reverse
	MSB first		Reverse
		Tx/D, Rx/D I/O polarity reverse bit (Note 3)	○ No reverse
			Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, neither UART1 CTS/RTS function, nor UART0 CTS/RTS separation function can be utilized. Set the UART1 CTS/RTS disable bit to "1".

Note 2: UART0 only. (UART1 CTS/RTS function cannot be used when this function is selected.)

Note 3: UART2 to UART4 only.

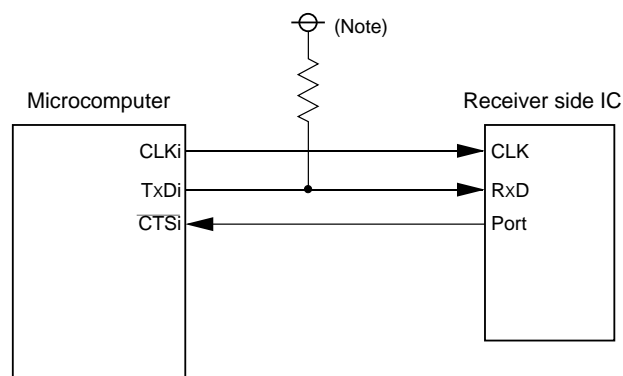
2.0 Introduction

- Operation
- (1) Setting the transmit enable bit to "1" and writing transmission data to the UARTi transmit buffer register makes data transmissible status ready.
 - (2) When input to the CTSi pin goes to "L" level, transmission starts (the CTSi pin must be controlled on the reception side).
 - (3) In synchronization with the first falling edge of the transfer clock, transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the UARTi transmit interrupt request bit goes to "1". Also, the first bit of the transmission data is transmitted from the TxDi pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.
 - (4) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that transmission is completed. The transfer clock stops at "H" level.
 - (5) If the next transmission data is set in the UARTi transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.

- Note
- Select CLKi and TxDi outputs with the function select register A, B and C.
 - Set CTSi pin's function select register A to I/O port and port direction register to "0".
 - When setting the function select registers A, B, and C, sets the function select registers B and/or C first, and then sets the function select register A.

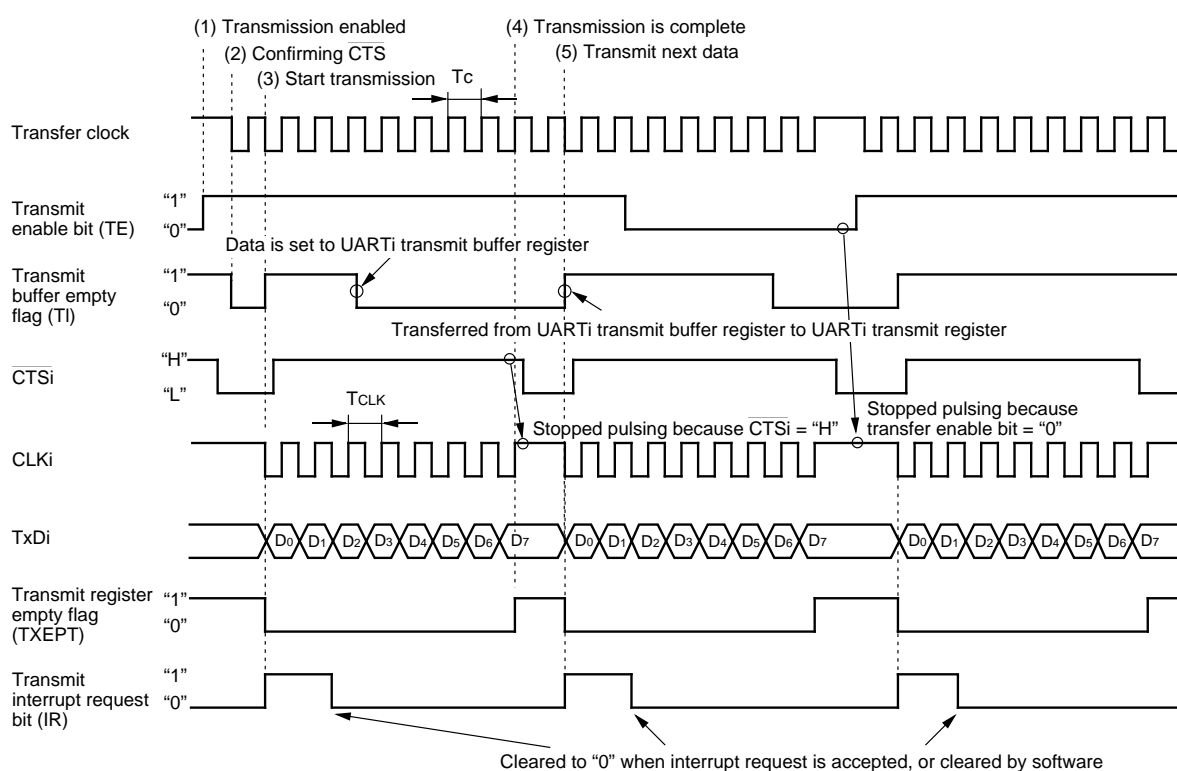
Figure 1 shows the operation timing

Example of wiring



Note : Since TxD2 pin is N-channel open drain, this pin needs pull-up resistance.

Example of operation



Shown in () are bit symbols.
The above timing applies to the following settings:

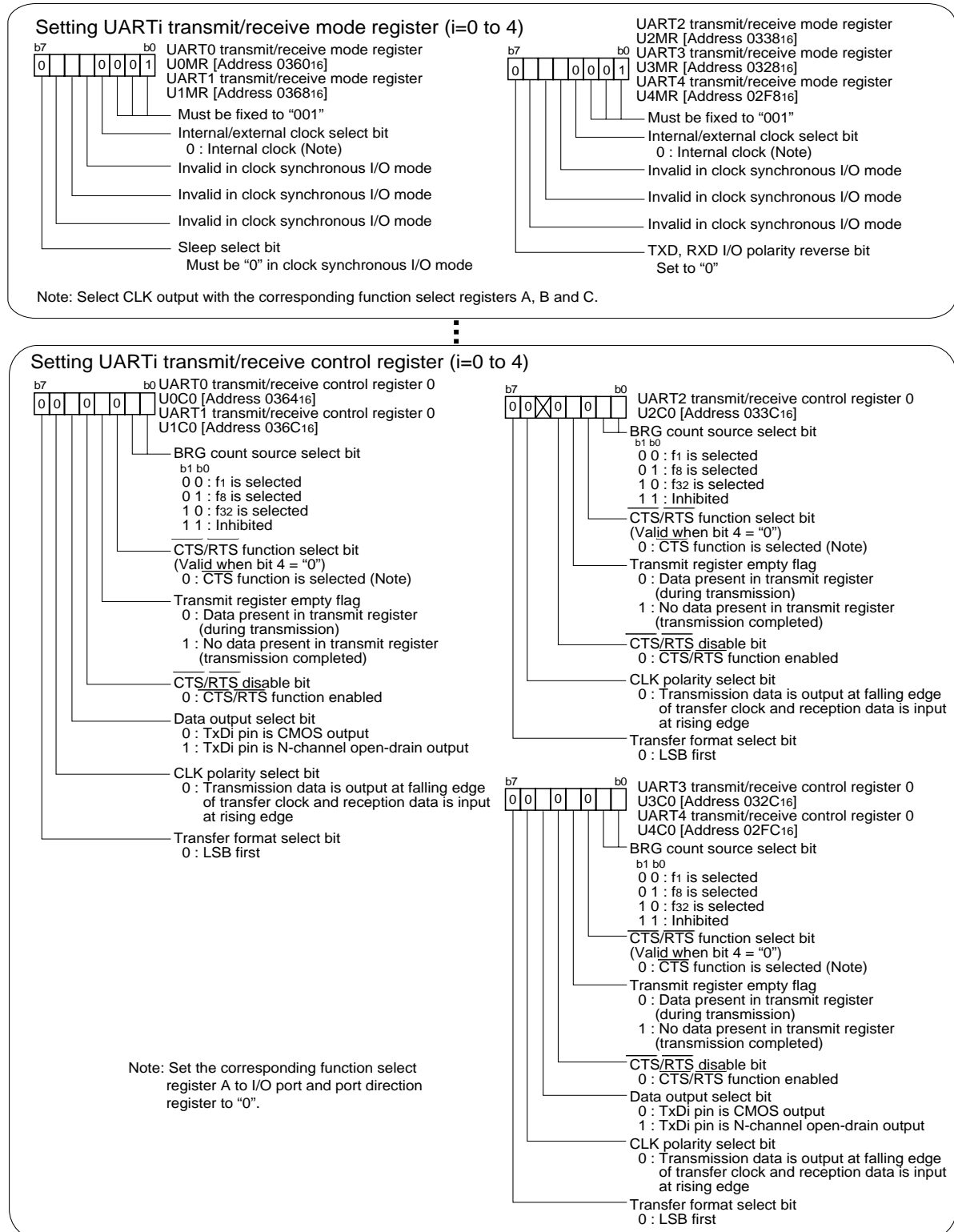
- Internal clock is selected.
- CTS function is selected.
- CLK polarity select bit = "0".
- Transmit interrupt cause select bit = "0".

$$T_c = T_{CLK} = 2(n + 1) / f_i$$

f_i : frequency of BRGi count source (f_1, f_8, f_{32})
 n : value set to BRGi

Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode

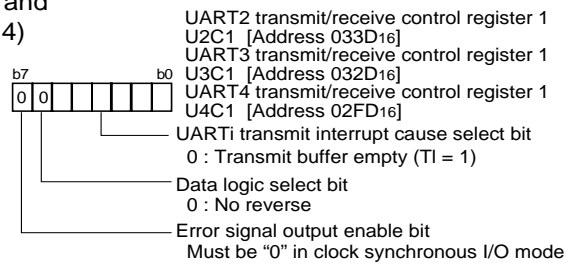
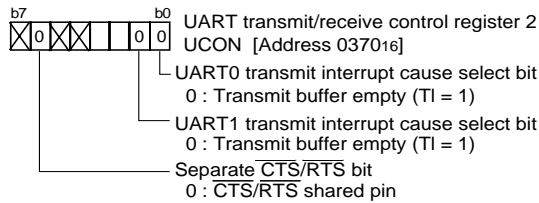
3.0 Set-up procedure



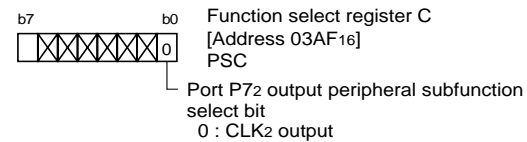
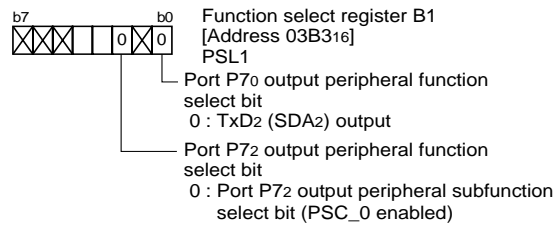
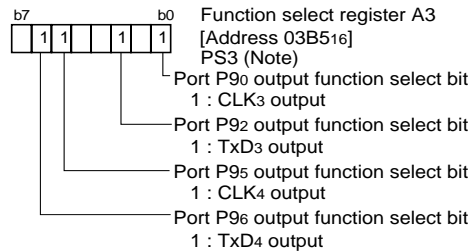
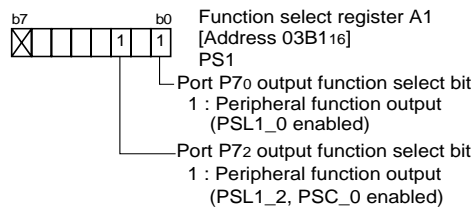
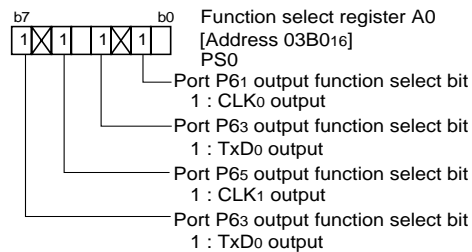
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Setting UART transmit/receive control register 2 and UARTi transmit/receive control register 1 (i=2 to 4)

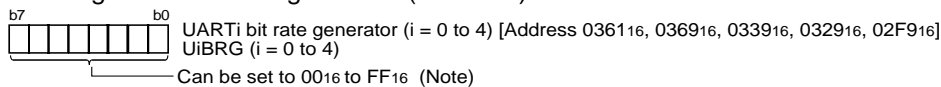


Setting function select register



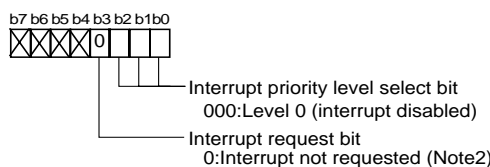
Note: Set bit 2 of the protect register (address 000A₁₆) to "1" when writing new value to this register.

Setting UARTi bit rate generator (i = 0 to 4)



Note: Write to UARTi bit rate generator when transmission/reception is halted.

Clearing UARTi transmit interrupt request bit (i=0 to 4)

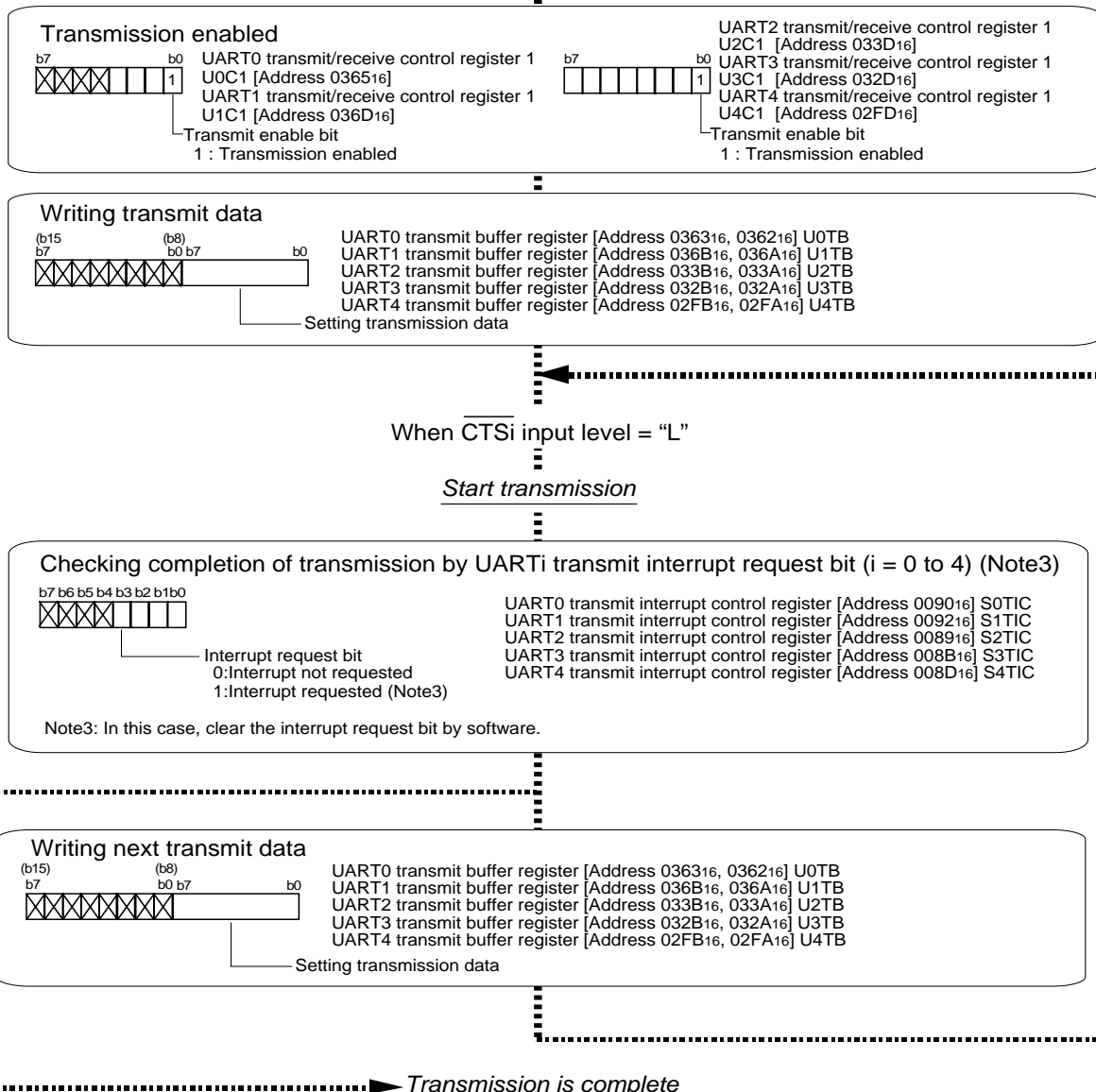


UART0 transmit interrupt control register [Address 0090₁₆] S0TIC
UART1 transmit interrupt control register [Address 0092₁₆] S1TIC
UART2 transmit interrupt control register [Address 0089₁₆] S2TIC
UART3 transmit interrupt control register [Address 008B₁₆] S3TIC
UART4 transmit interrupt control register [Address 008D₁₆] S4TIC

Note2: This bit can only be accessed for reset (=0), but cannot be accessed for set (=1).

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4.0 Programming Code

```

;*****
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0138_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of Serial I/O
;               (transmission in clock-synchronous serial I/O mode)
;   HISTORY   : 2004.02.16 Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;*****
;*****
;   Include
;*****
;*****
;   .LIST      OFF          ;Stops outputting lines to the assembler list file
;   .INCLUDE   sfr80100.inc ;Reads the file that defined SFR
;   .LIST      ON           ;Starts outputting lines to the assembler list file
;
;*****
;   Symbol definition
;*****
RAM_TOP      .EQU    000400H ;Start address of RAM
RAM_END      .EQU    002BFFH ;End address of RAM
ROM_TOP      .EQU    0FFC000H ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFFDCH ;Start address of fixed vector
;
;*****
;   Allocation of work RAM area
;*****
;*****
;   .SECTION    WORKRAM, DATA
;   .ORG        RAM_TOP
WORKRAM_TOP:
C_POWER      .EQU    3
C_DATA_SIZE  .EQU    (1<< C_POWER) ;Data size
v_Trans_data: .BLKB   C_DATA_SIZE   ;Area of send data for sample
WORKRAM_END:
;
;*****
;   Program area
;*****
;*****
;=====
;   Start up
;=====
;*****
;   .SECTION    PROGRAM, CODE ;Declares section name and section type
;   .ORG        ROM_TOP      ;Declares start address
RESET:
;   Sets Processor mode, System clock and Main clock division
MOV.B        #03H, prcr      ;Removes protect
MOV.B        #10000000B, pm0 ; Single-chip mode
MOV.B        #11000000B, pm1 ; Flash memory version
MOV.B        #00001000B, cm0 ; Xcin-Xcout High
MOV.B        #00100000B, cm1 ; Xin-Xout High
MOV.B        #00010010B, mcd ; No division mode
MOV.B        #00H, prcr      ;Protects all registers
;

```


Operation of Serial I/O (transmission in clock-synchronous serial I/O mode)

```

; Clears WORKRAM area
MOV.W    #0, R0
MOV.W    #(RAM_END-RAM_TOP)/2, R3
MOV.W    #WORKRAM_TOP, A1
SSTR.W
; Makes transmission data for sample ( 1 to C_DATA_SIZE )
MOV.B    #1, R0L                ;1st data
MOV.W    #0, A0                ;Initialize offset address
MAKE_DATA:
MOV.B    R0L, v_Trans_data[A0] ;
ADD.B    #1, R0L                ;
ADD.W    #1, A0                ;
CMP.W    #C_DATA_SIZE, A0      ;
JLTU     MAKE_DATA             ;
;
;=====
;      Serial I/O (transmission in clock-synchronous serial I/O mode)
;=====
; Setting UART0 transmit/receive mode register
MOV.B    #00000001B, u0mr
;      ||| |++-----;Must be fixed to "001"
;      ||| |+-----;Internal/external clock select bit (0:Internal clock)
;      |++-----;Invalid in clock synchronous I/O mode
;      +-----;Sleep select bit
;      (Must always be "0" in clock synchronous I/O mode)
; Setting UART0 transmit/receive control register 0
MOV.B    #00001000B, u0c0
;      ||| |++-----;BRG count source select bit (00:f1 is selected)
;      ||| |+-----;CTS function is selected (Valid when bit 4="0") (Note)
;      ||| +-----;Transmit register empty flag (Written value is invalid)
;      ||+-----;CTS/RTS disable bit (0:CTS/RTS function enabled)
;      |+-----;Data output select bit (0:TxDi pin is CMOS output)
;      +-----;CLK polarity select bit
;      (0:Transmission data is output at falling edge of
;      transfer clock and
;      reception data is input at rising edge)
;      +-----;Transfer format select bit (0:LSB first)
; Setting UART transmit/receive control register 2
MOV.B    #00000000B, ucon
;      ||| |++-----;UART0 transmit interrupt cause select bit
;      ||| |         (0:Transmit buffer empty (TI=1) )
;      ||| |++-----;UART1 transmit interrupt cause select bit
;      ||| |++-----;UART0 continuous receive mode enable bit
;      ||| |++-----;UART1 continuous receive mode enable bit
;      ||++-----;Nothing is assigned (When write, set "0")
;      |+-----;Separate CTS/RTS bit (0:CTS/RTS shared pin)
;      +-----;Nothing is assigned (When write, set "0")
; (Note) Set the corresponding function select register A to I/O port
; and port direction register to "0"
BCLR     pd6_0                ;Port P60 is input direction
BCLR     ps0_0                ;CTS0[P60] is I/O port
; Setting function select register
BSET     ps0_1                ;Port P61 output function select bit (1:CLK0 output)
BSET     ps0_3                ;Port P63 output function select bit (1:TxD0 output)
; Setting UART0 bit rate generator (1MHz, @20MHz f1)
MOV.B    #9, u0brg
; Clear UART0 transmit interrupt request bit
MOV.B    #00000000B, s0tic
;      |++-----;Interrupt priority level select bit
;      |         (000:Level 0, interrupt disabled)
;      +-----;Interrupt request bit (0:Interrupt not requested)
; Transmission enabled
MOV.B    #00000001B, u0c1 ;UART0 transmit/receive control register 1
;      +-----;(1:Transmission enabled)
;

```

Operation of Serial I/O (transmission in clock-synchronous serial I/O mode)

```

=====
;      Main program
=====
      MOV.W    #0, A0          ;Initialize offset
WRITE_DATA:
      ; Writing transmit data
      MOV.B    v_Trans_data[A0], u0tb
      ; When CTS0 input level = "L", Start transmission
;
WAIT_TRANS:
      ; Checking completion of transmission by UART0 transmit interrupt request bit
      BTST     ir_s0tic
      JNC      WAIT_TRANS
      MOV.B    #00H, s0tic     ; Clear UART0 transmit interrupt request bit
;
PREPARE_NEXT_DATA:
      ADD.W    #1, A0
      AND.W    #(C_DATA_SIZE-1), A0
      JNZ      WRITE_DATA
;
COMPLETE_TRANS:
      ; Transmission is complete
      JMP      COMPLETE_TRANS
;
=====
;      Dummy interrupt processing program
=====
dummy:
      REIT
;
;*****
;      Setting of fixed vector
;*****
      .SECTION  F_VECT, ROMDATA
      .ORG      FIXED_VECT_TOP
;
      .LWORD    dummy      ;Undefined instruction
      .LWORD    dummy      ;Overflow
      .LWORD    dummy      ;BRK instruction execution
      .LWORD    dummy      ;Address match
      .LWORD    dummy      ;
      .LWORD    dummy      ;Watchdog timer
      .LWORD    dummy      ;
      .LWORD    dummy      ;NMI
      .LWORD    RESET      ;Reset
;
      .END

```

5.0 Reference

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M16C/80 group Rev. E3

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